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Effect of CuPc and PEDOT:PSS as hole transport layers in planar heterojunction CdS/CdTe solar cell

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Keywords: heterojunction, photovoltaic, electronic structure, hole transport

Abstract

This paper presents the fabrication and photovoltaic performance of new architecture based planar heterojunction CdS/CdTe thin film solar cells which were employed with two hole transport layers (PEDOT:PSS as HTL1 and CuPc as HTL2). The reported solar cells were fabricated through various deposition techniques such as sputtering, thermal evaporation, spin coating and characterized by FESEM, AFM, XPS, UPS and AM 1.5 solar simulator. The interfacial layer growth and chemical state identification of the deposited thin films were studied by cross-sectional FESEM and XPS techniques. The band bending occurs between absorbing and transporting layer helps to inject the excited charge carriers effectively into electrode that was explained using UPS analysis. The present work intends to explain the role of additional window layer (TiO_2), buffer layer (CdS) and hole transporting layers (PEDOT:PSS and CuPc) in the novel device architecture. Further, these findings will offer new research directions to address the double hole transport (back contact) layers selection concept in CdS/CdTe heterojunction based solar cells.

1. Introduction

In recent years, due to world population growth and techno economic energy requirements, there has been an over dependence on sustainable energy sources. To fulfill this energy demand, renewable energy sources are found to be an alternative for the conventional non-renewable energy resources. Solar energy is considered as one of the most important renewable energy, due to its abundance, being pollution-free and also possessing wide energy distribution. The amount of solar energy received in one hour alone on the surface of earth is sufficient to provide world energy consumption for one year [1]. Moreover to harvest the solar energy, solar cell is one direct way to exploit and convert it into electricity. In recent years, thin film (second generation) solar cells have been extensively studied due to its lower material cost and less energy consumption during production [2, 3]. Cadmium telluride (CdTe) a binary (II–VI) chalcogenide based thin film solar cells were shown to produce high power conversion efficiency (PCE) solar cells, due to its direct band gap (1.45 eV at 300 K) and higher optical absorbance coefficient ($\alpha > 10^4 \, \mathrm{cm}^{-1}$) [4–6]. In general, a typical superstrate CdTe thin film solar cells have been constructed by: (i) transparent conducting oxide (TCO) layered substrate as front electrode, (ii) commonly employed heterojunction partner n-type cadmium sulfide (CdS) as buffer layer, (iii) p-type CdTe as an absorbing layer and iv) metal over the CdTe layer as bottom electrode.

At the interface of thin CdS/CdTe, the fact that CdTe and CdS are miscible to form a highly intermixed layer ($CdS_{1-x}Te_x$), which facilitates to reduce the interfacial defect density [7]. According to Shockley–Queisser limit, theoretically calculated PCE of CdS/CdTe heterojunction thin film solar cell is 33% and at present achieved a record efficiency (on lab scale) of 22.1% [8–10]. However, to achieve high quality polycrystalline CdTe thin film (without pinhole formation), the required absorbing layer thickness is to be around ∼2–5 μm. At the same time, when CdTe layer thickness exceeds 1 μm, the performance of solar cell decreases due to local shunting. In

addition, according to the absorption co-efficient of CdTe, 1 μm thick layer is well enough to absorb 90% of the solar energy spectrum [11–14].

In recent years to enhance the efficiency of CdTe solar cells, the research efforts are continued in various aspects, especially to find a suitable material for back contact and also design a novel CdTe device architectures [15, 16]. Hence, the CdTe solar cells have been demonstrated by introducing different front and back charge transport contact (electron/hole) layers to collect and transport the charge carrier towards the bottom and top electrodes [7, 16–20]. In other words, in order to provide a suitable driving force to transfer the photogenerated charge carriers effectively; conduction band (CB) of the absorbing layer should be significantly higher than CB of electron transport layer (ETL) and as well as the valance band (VB) of absorbing layer should be lower than the VB of hole transport layer's (HTL) [21].

To date, CdTe solar cells have been extensively studied using different ETL like CdS, zinc sulfide (ZnS), $Zn_xCd_{1-x}S$, zinc selenide (ZnSe), titanium dioxide (TiO_2) [7, 22–24]. Amurtha *et al*, have reported that, in CdS/CdTe heterojunction thin film solar cell an addition of TiO_2 window layer inserted between FTO substrate and CdS layer helps to reduce the device leakage current [25]. Also Hernandez *et al*, have reported that the sputtered TiO_2 thin film (15 nm) can be used as high resistance buffer layer to achieve higher conversion efficiency (12%) in CdS/CdTe solar cells [26]. On the other hand, Khrypunov *et al* have reported that, at the metal interface (CdTe/metal) high WF CdTe interns to forms Schottky barrier (back diode behavior) instead of ohmic contact [15].

To avoid such issues in CdTe solar cells, inorganic molybdenum oxide (MoO_3), organic SPIRO OMeTAD (N2, N2, N2′, N2′, N7, N7, N7′, N7′-octakis(4-methoxyphenyl)-9, 9′-spirobi [9H-fluorene]-2, 2′, 7, 7′-tetramine), PEDOT:PSS (poly (3, 4-ethylenedioxythiophene) polystyrene sulfonate) and poly(3-hexythiophene-2, 5-diyl) (P3HT) have been extensively used as HTL [15, 16, 19, 20, 27, 28]. Among them, PEDOT:PSS having the advantage of high work function (WF) which helps reduce the barrier height, especially to prevent the metal diffusion into the absorbing CdTe layer [23]. Moreover, the lower interfacing defects at the inorganic/polymer interface facilitate to decrease charge carrier trapping and recombination in the device architecture [29]. The properties of PEDOT:PSS (as back contact) in CdTe solar cells has been extensively investigated and reported [19, 20]. Similarly, in bulk heterojunction based solar cells to improve the cell efficiency an oligomer copper phthalocyanine (CuPc) is often employed as HTL. This may due to its suitable highest occupied molecular orbital (HOMO) energy level to enhance carrier mobility, excellent thermal and chemical stability, and low cost [30–32]. Moreover, the combination of CuPc along with PEDOT:PSS were extensively studied and reported in organic heterojunction solar cells [33–35]. In our present work an attempt has been made to fabricate and study the photovoltaic performance of new architecture based planar heterojunction CdS/CdTe thin film solar cells by introducing two hole transport layers (PEDOT:PSS as HTL1 and oligomer phthalocyanine (CuPc) as HTL2). The fabrication details, characterizations of the developed structure, photovoltaic behavior of the devices and relevant discussions are reported in the subsequent sections.

2. Experimental section

2.1. Device fabrication

The CdS/CdTe planar heterojunction solar cells described in this work were used SnO_2:F over thin glass plate as substrates. Prior to thin film deposition, the FTO substrates were cleaned using 1:1:1 ratio of acetone, 2-propanol, and de-ionized (DI) water, later the substrates were blow dried under nitrogen (N_2) gas. The window layer of TiO_2 (100 nm) on top of FTO and the buffer layer of CdS (50 nm) over the TiO_2/FTO were deposited using RF magnetron sputtering. Each deposited layer was annealed at suitable condition before depositing consecutive layers. The coated TiO_2/FTO substrates were air annealed at 450 °C for 30 min, whereas the CdS/TiO_2/FTO films were annealed at 350 °C for 5 min under N_2 atmosphere. On top of the CdS/TiO_2/FTO film ~1 μm thick absorbing layer of CdTe was deposited by thermal evaporation. The coated CdTe/CdS/TiO_2/FTO films were annealed at 450 °C for 20 min in N_2 atmosphere for improving the crystallinity and the junction formation. The solar cells were fabricated with two different architectures, device A: FTO/TiO_2/CdS/CdTe/PEDOT:PSS/Au, and device B: FTO/TiO_2/CdS/CdTe/PEDOT:PSS/CuPc/Au. On both devices A and B, 150 nm and 100 nm thick HTL1 of PEDOT:PSS were spin coated respectively at 3000 rpm under room temperature and later the films were air baked at 100 °C for 20 min. In case of the novel architecture device B, a layer of 50 nm HTL2 of CuPc was additionally deposited over the surface of PEDOT:PSS/CdTe/CdS/TiO_2/FTO using thermal evaporation. Finally a 100 nm top electrode Au was deposited over the both device architectures by thermal evaporation. Experiments are conducted on five optimized planar heterojunction samples and the best results are presented here.
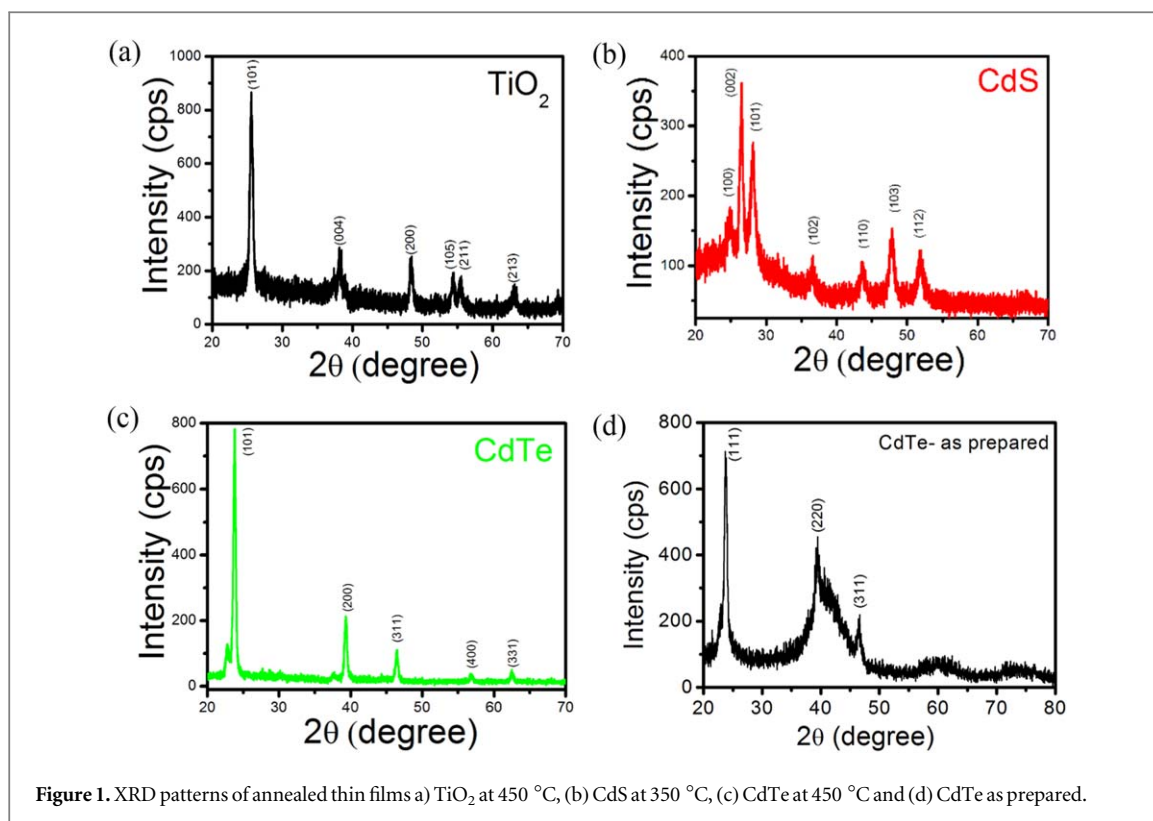
Figure 1. XRD patterns of annealed thin films a) TiO_2 at 450 °C, (b) CdS at 350 °C, (c) CdTe at 450 °C and (d) CdTe as prepared.

2.2. Characterization

The surface morphology and topographical information of the fabricated films were studied using a high-resolution field emission scanning electron microscope (Carl ZEISS-ULTRA 55 FE-SEM) and tapping mode atomic force microscopy (AFM) (Bruker dimension ICON). Chemical oxidation states of deposited films were obtained by x-ray photoelectron spectroscopy (XPS) (Kratos Axis Ultra DLD) under the condition of 13 mA emission current and 12 kV as accelerating voltage (156 W). Before recording the XPS spectra of TiO_2, CdS and CdTe films were sputtered using Argon ion source (4 kV, area of 3×3 mm^2) to remove the surface contaminations. The electronic structures (valence band maximum and work function) of deposited TiO_2, CdS, CdTe, PEDOT: PSS and CuPc films were characterized using ultra-violet photoelectron spectroscopy (UPS) using He I source energy (21.22 eV). The current-voltage (I-V) performances of the devices were measured using Keithley 2420 with the light source of 1000 W m^{-2} (Newport) oriel solar simulator under the condition of AM 1.5.

3. Results and discussion

The GI-XRD and Raman spectroscopy techniques were used to observe the crystallinity and phase identification of annealed TiO_2, CdS and CdTe thin films. The GI-XRD geometry is particularly useful for thin films to increase the path length of the beam into the layer, leading to achieving a better signal-to-noise ratio. Figure 1(a) represents the relative intensity peaks of TiO_2 film presented at the diffraction angles of 25.3°, 37.9°, 48.2°, 54.1°, 55.1° and 61.9° which corresponds to the orientation of (101), (004), (200), (105), (211) and (213) respectively (JCPDS: 84–1285) [36]. It reveals that the deposited TiO_2 thin films were in dominant anatase polycrystalline structure without any impurity peaks. The planes of CdS thin film (figure 1(b)) were oriented at (100), (002), (101), (102), (110), (103) and (112) which correspond to the diffraction angles of 25.0°, 26.6°, 28.3°, 36.6°, 43.6°, 47.8° and 51.8°. The calculation indicated standard hexagonal wurtzite structure (JCPDS: 41–1049) [26]. The CdTe diffraction pattern displays five diffraction peaks at 2θ values of 23.7°, 39.5°, 47.2° and 63.1° which correspond to the diffraction produced by the (111), (220), (311), (400) and (331) planes which indicates the preferential crystallographic growth of CdTe, respectively. The diffraction intensity of CdTe film showed an increase, due to the improved crystallinity compared to the as prepared thin film (see figures 1(c) and (d)). The intense peak values of annealed CdTe thin film was in good agreement with a cubic zinc blende structure (JCPDS:15–0770) [37].

Figure 2 represents the Raman bands of TiO_2, CdS and CdTe thin films. As seen from the figure 2, the crystal phases are well separated in frequency and thus offer accurate information about the presence of different crystal
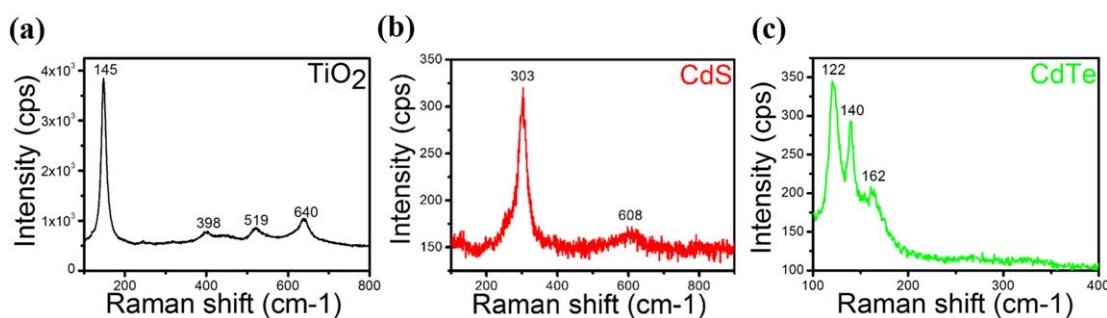
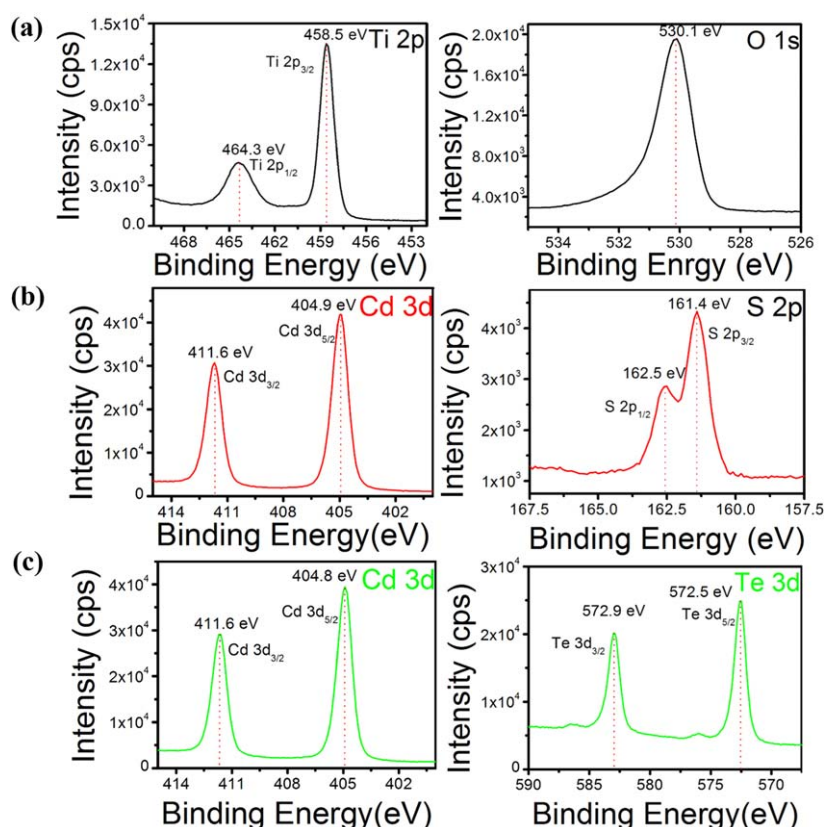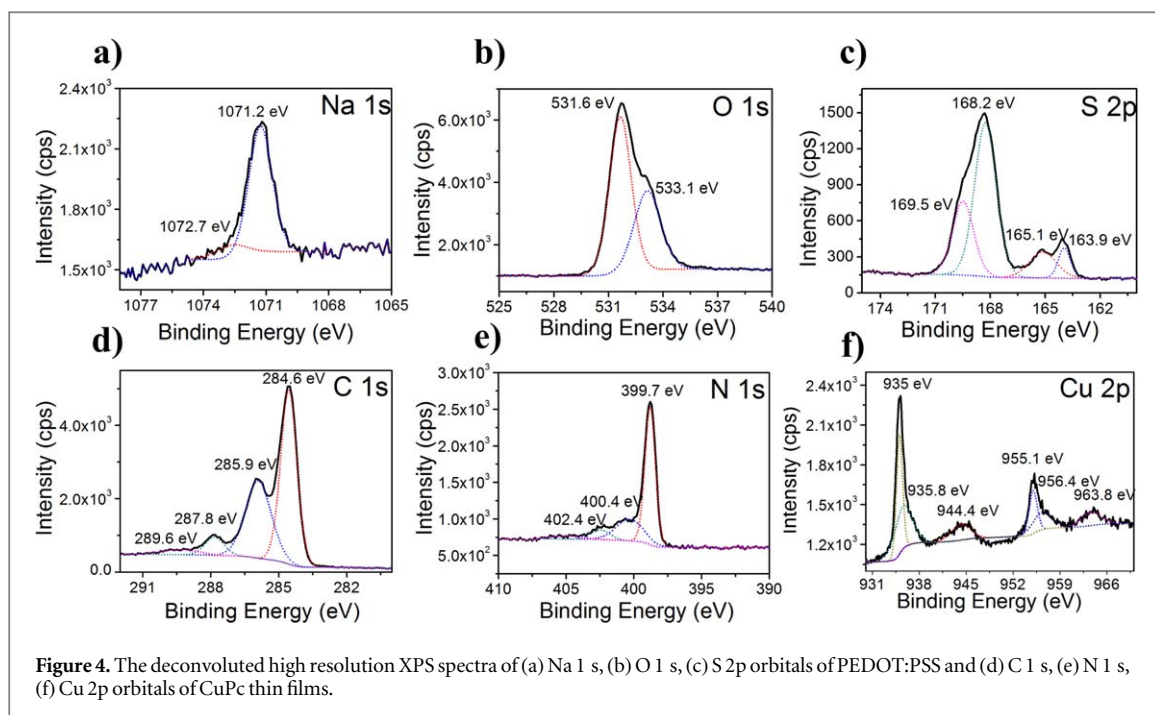**Figure 2.** Raman analysis of annealed films (a) TiO_2 at 450 °C (b) CdS at 350 °C (c) CdTe at 450 °C.

Figure 3. XPS spectra of annealed (a) TiO_2 (b) CdS (c) CdTe thin films.

phases in the films. In general, the anatase phase of TiO_2 has six Raman active modes: $A_{1g} + 2B_{1g} + 3E_g$. Figure 2(a) shows the Raman spectrum of the TiO_2 thin film, with peaks located at 145 cm^{-1}, 398 cm^{-1}, 519 cm^{-1}, and 640 cm^{-1} confirming the anatase phase of TiO_2, which consisted with XRD data. The prominently intense E_g (low-frequency) mode at 145 cm^{-1} and 640 cm^{-1} and bending vibrations B_{1g} mode (O–Ti–O) peaks at 398 cm^{-1} and 519 cm^{-1} were correspond to anatase TiO_2 [38]. Also, The peaks at 303 cm^{-1} and 608 cm^{-1} correspond to the fundamental optical phonon Longitudinal modes (LO) and the first over tone mode (2LO) of annealed CdS film as shown in figure 2(b) [39]. The position rules for transverse (TO), LO and A_1 (Te) optical phonon modes of CdTe films were found to be at 140 cm^{-1}, 162 cm^{-1} and 122 cm^{-1} respectively [22].

Further to confirm the surface level oxidation state (before the heterojunction layer interface formation), XPS analysis was carried out on the deposited films. Figure 3 shows the chemical state of surface etched XPS spectra of TiO_2, CdS, and CdTe thin films. The Ti $2p_{3/2}$ and Ti $2p_{5/2}$ peaks of TiO_2 films were observed at the binding energies of 458.5 eV and 464.3 eV respectively, which confirms the deposited films are in TiO_2 chemical state (figure 3(a)) [40]. The peaks located at the binding energies of 404.9 eV and 411.6 eV are observed for CdS thin film, which is consistent with Cd^{2+} state. The S 2p core level spectrum of CdS centered at 161.4 eV and 162.5 eV is attributed to the S $2p_{3/2}$ and S $2p_{5/2}$ of S^{2-} states respectively (figure 3(b)) [41]. The peaks at the

Figure 4. The deconvoluted high resolution XPS spectra of (a) Na 1 s, (b) O 1 s, (c) S 2p orbitals of PEDOT:PSS and (d) C 1 s, (e) N 1 s, (f) Cu 2p orbitals of CuPc thin films.

binding energies of 404.8 eV and 411.6 eV are related to Cd $3d_{5/2}$ and Cd $3d_{3/2}$ emissions of CdTe respectively. Figure 3 shows Te 3d region of the same XPS spectrum where observed peaks at binding energies of 572.5 eV and 582.9 eV are related to Te $3d_{5/2}$ and Te $3d_{3/2}$ (figure 3(c)) [37].

The O 1 s spectra of spin coated HTL1 PEDOT: PSS film has two major peaks at 531.8 eV and 533.2 eV, are assigned to S=O and O–H bonds respectively (figures 4(a)–(f)). Moreover, O–H bond of PEDOT and PSS chains help to minimize the surface oxidation of CdTe at the interface, resulting decrease in the device leakage current. Also, the presence of those bonds are to assist to enhance the hole transportation property (figures 4(a) and (b)). The sulfur (S 2p) peaks from the PSS and PEDOT chains correspond to doublet at the binding energies of 169.5 eV and 165.1 eV, 168.2 eV and 163.9 eV respectively (figure 4(c)) [42]. The high-resolution XPS spectrum of N 1 s of HTL2 CuPc as shown in figure 4(e) comprises the groups of nitrogen atoms in N–N, C–N and Cu–N bonding in the CuPc molecule. The corresponding electronic states of Cu $2p_{3/2}$ and $2p_{1/2}$ peaks were located at 935.2 eV and 955.1 eV respectively. The presence of Cu (II) state in CuPc molecule clearly exhibits a ∼9 eV binding energy (BE) difference between the major Cu peak and satellite peak at 944.4 eV (figure 4(f)) [43].

The UPS spectra of TiO_2, CdS, CdTe, PEDOT:PSS and CuPc thin films are shown in figure 5. The surface WF (ϕ) of the films were determined by the energy difference between the incident photon (hυ = 21.22 eV) and the mid-point of respective secondary onset from UPS spectrum. The measured BE of the TiO_2, CdS and CdTe films (from figures 5(a)–(c)) are 17.12 eV, 17.46 eV and 16.63 eV, which correspond to the WF of 4.1 eV, 3.76 eV and 4.59 eV respectively. The valence band maximum (V_{bm}) was measured by the linearly fitting leading edge of the valence band and extrapolating the fitted line to the *X*-axis of the spectrum. The measured V_{bm} of TiO_2, CdS and CdTe films were 3.39 eV, 2.94 eV and 0.46 eV and its calculated valence band position (VB = V_{bm} + ϕ) of 7.49 eV, 6.7 eV and 5.05 eV respectively.

The band gap (E_g) of TiO_2 (3.2 eV) and CdS (2.43 eV) were measured from the UV-visible spectroscopy (figures 6(a) and (b)), the calculated conduction band (CB) positions (VB-E_g) are 4.29 eV and 4.27 eV respectively. Therefore, the Fermi levels (E_f) of TiO_2 and CdS (4.1 eV and 3.76 eV) falls below the CB, which clearly reveals that both are consisted with n-type semiconductors. Similarly from figure 6(c), the CdTe (4.59 eV) shows p-type semiconductor behavior, due to its E_f value which is closer to the valence band (5.05 eV) with respect to the calculated CB position of 3.58 eV (E_g = 1.47 eV). Figure 6(d) and (e) shows the WF of PEDOT:PSS and highest occupied molecular orbital (HOMO) level of CuPc were 5.01 eV and 4.83 eV respectively. Figure 6(f) explains the schematic band diagram of fabricated devices.

Figures 7(a)–(f) shows the cross-section and planar view FESEM images of FTO substrate and the deposited TiO_2, CdS, CdTe, PEDOT:PSS and CuPc films. Note that the CdS/CdTe solar cells shown in figures 7(a)–(f) are a superstrate configuration. Figure 7(a) shows the lateral view of transparent conducting oxide FTO (500 nm) coated over the glass substrate with granular surface morphology (inset Figure 7(a)). The uniform deposition of TiO_2 window layer (figure 7(b)) helps to prevent the formation of shunt resistance in the device, which arises from the CdTe absorbing layer making contact with the bottom electrode (FTO) through CdS pinholes.
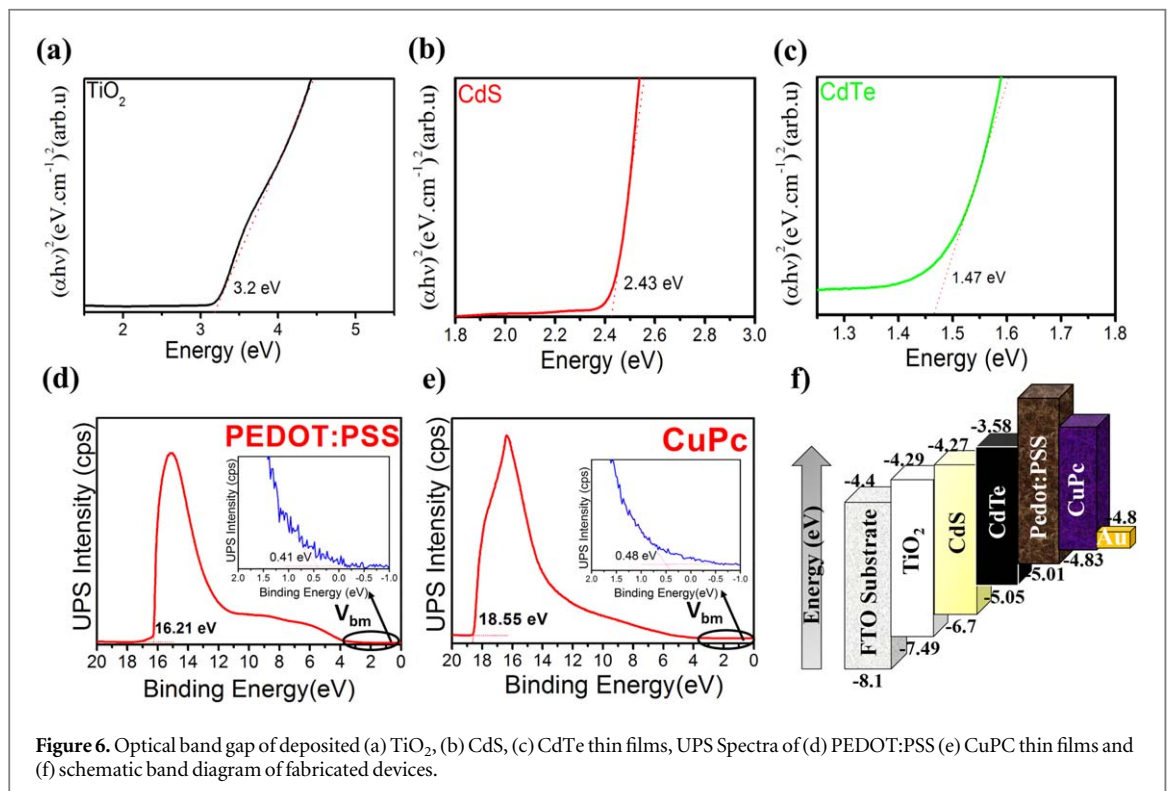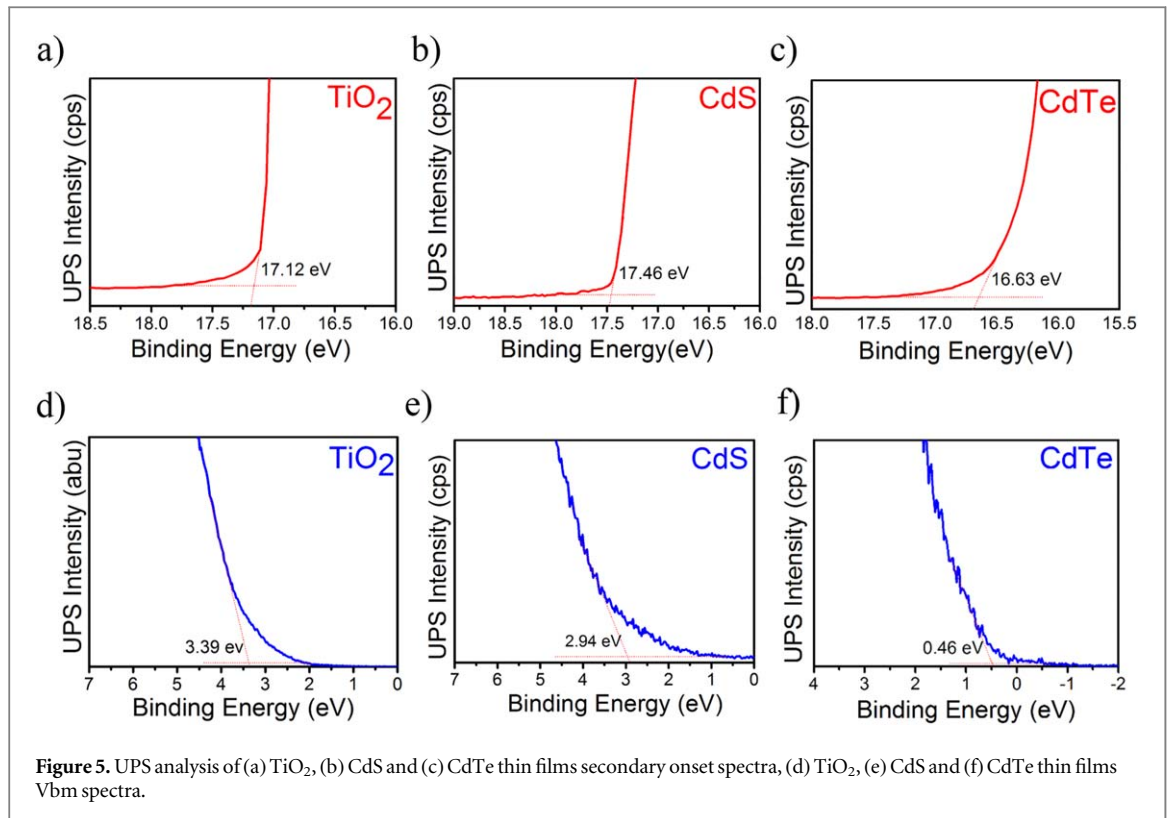
Figure 5. UPS analysis of (a) TiO$_2$, (b) CdS and (c) CdTe thin films secondary onset spectra, (d) TiO$_2$, (e) CdS and (f) CdTe thin films Vbm spectra.

Figure 6. Optical band gap of deposited (a) TiO$_2$, (b) CdS, (c) CdTe thin films, UPS Spectra of (d) PEDOT:PSS (e) CuPC thin films and (f) schematic band diagram of fabricated devices.

Figure 7(c) shows the cross sectional view of CdS buffer layer deposited over the n-type TiO$_2$/FTO. Figure 7(c) in set shows the morphology of highly dense, pinhole free CdS buffer layer with an average grain size of ~30 nm. It is noted that an absorbing layer of polycrystalline CdTe film (figure 7(d)) was densely compact and had good coverage over CdS/TiO$_2$/FTO. Figures 7(e) and (f) show cross sectional and surface view of spin coated and thermal evaporated HTL1 and HTL2 on top of CdTe/CdS/TiO$_2$ layers respectively. It clearly reveals that the HTL1 and HTL2 layers were uniformly deposited consecutively, which helps to transport the charge carriers from the granular CdTe layer. Additionally, AFM analysis was used to carry out to study topographical
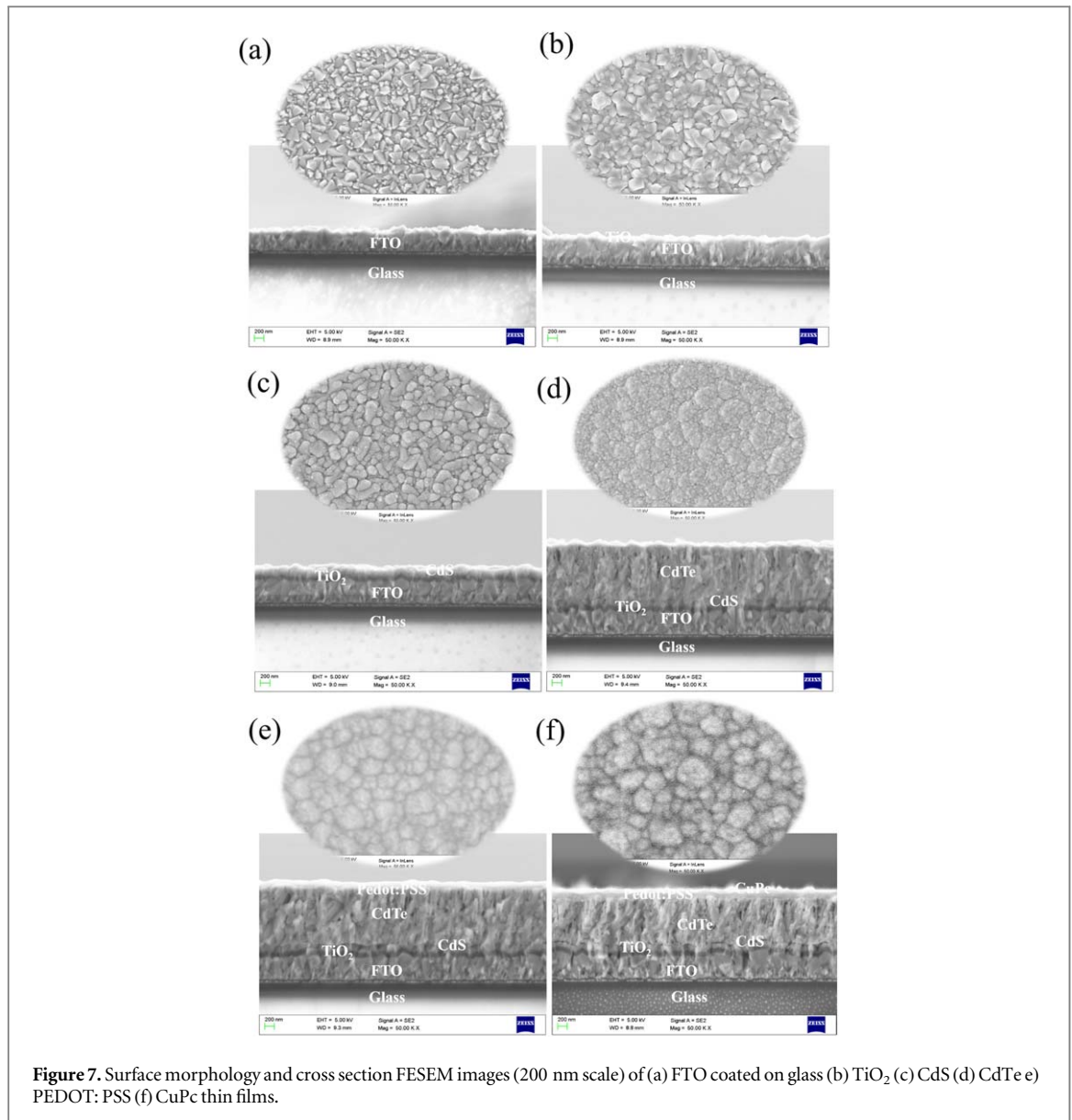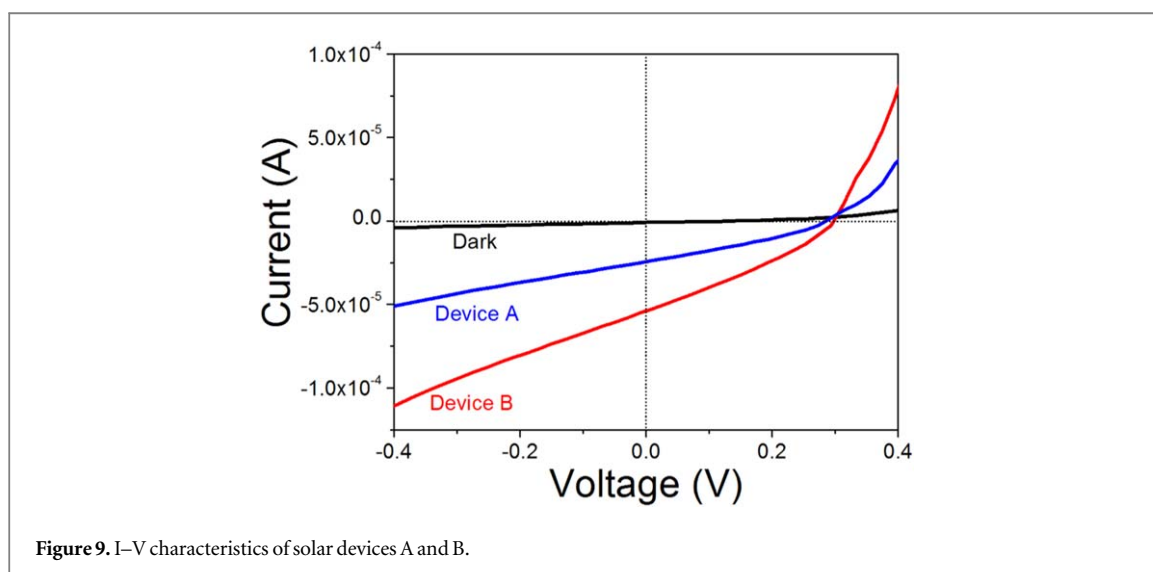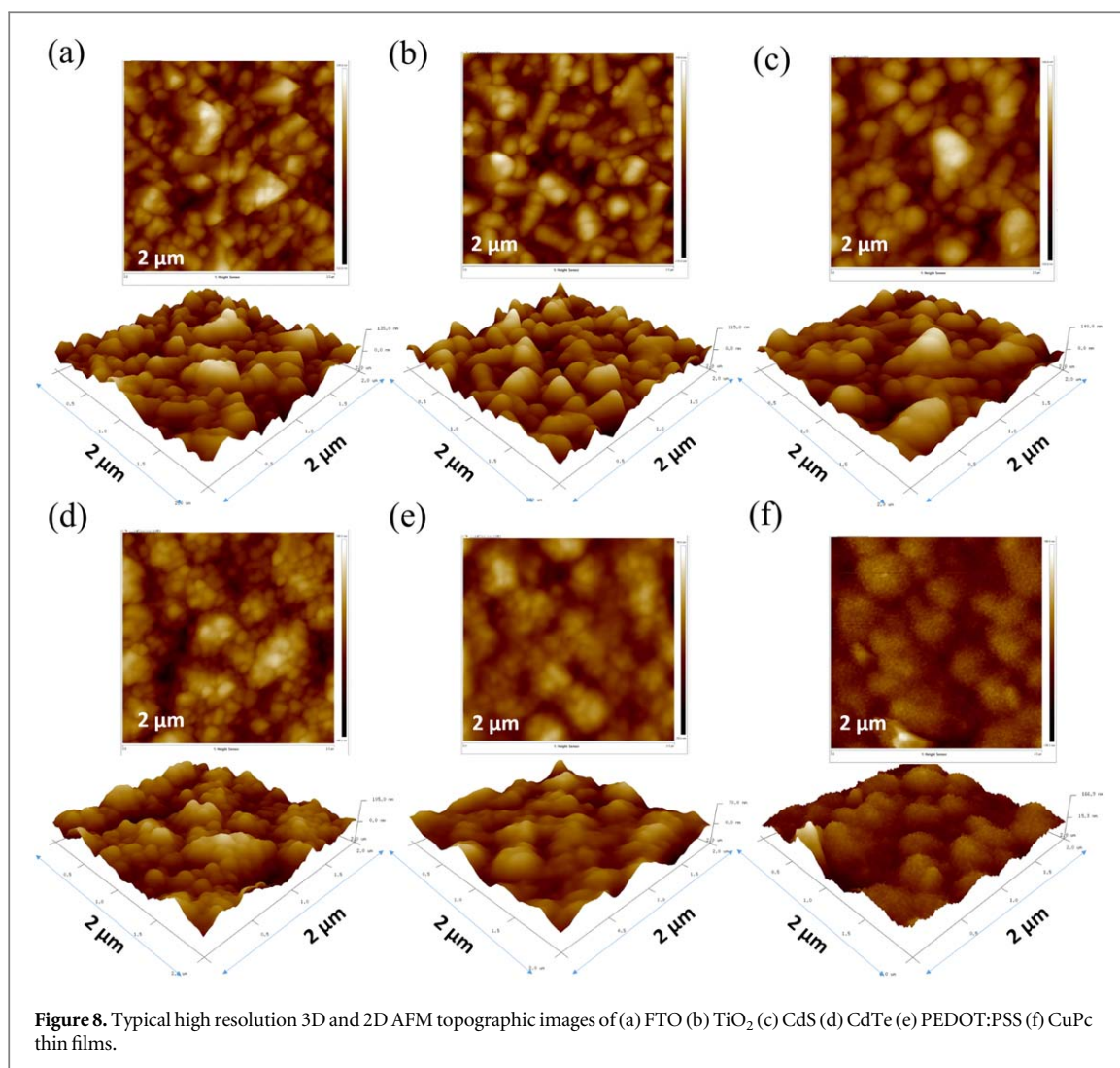
Figure 7. Surface morphology and cross section FESEM images (200 nm scale) of (a) FTO coated on glass (b) TiO$_2$ (c) CdS (d) CdTe e) PEDOT: PSS (f) CuPc thin films.

analysis of the deposited TiO$_2$, CdS, CdTe, PEDOT:PSS and CuPc thin films (figures 8(a)–(f)). The high-resolution topological AFM images (small area) 2D and 3D of prepared films were well consistent with FESEM studies.

The current-voltage (I-V) characteristics of the fabricated planar heterojunction CdS/CdTe solar cells are shown in figure 9. All the measurement were carried out under 1 sun illumination (1000 W m^{-2}), AM1.5 solar simulator with an active area of ~0.2 mm^2. The solid-state device A exhibited PCE of I$_{sc}$ = 2.41 × 10^{-5} A, V$_{oc}$ = 0.28 V, FF = 31%, η = 1.25% and for device B, I$_{sc}$ = 5.4 × 10^{-5} A, V$_{oc}$ = 0.3 V, FF = 30.7%, η = 2.74% respectively. As compare to device A, an increased open circuit voltage and short circuit current was observed in device B from 0.28 V to 0.30 V and from 2.41 × 10^{-5} A to 5.4 × 10^{-5} A respectively. On other words, due to the influence of CuPc (HTL2) along with PEDOT:PSS (HTL1), the photovoltaic performance of device B showed significant improvement. It clearly shows that, the addition of CuPc as HTL2 causes the band bending at PEDOT:PSS/CuPc/Au interface (as described from UPS analysis), resultant increases the short circuit current in device B which leads the improved PCE. However, the observed cell parameters are considerably poor compared to the commercial CdS/CdTe (layer thickness 2–7 μm) solar cells. But this first attempt study gives the fact that, the influence of two back contact layers in planar heterojunction prototype CdS/CdTe (layer thickness 1 μm) solar cell helps to enhance the device efficiency. Also, it is observed that the device B has shown 2.74% efficiency, which is comparably higher than recently reported ultra-thin CdTe layer based thin film solar cells [22]. However, an appropriate materials design and careful optimization of layer thickness, annealing temperature and device structure modification will pave the way for high performance solar cells.

Figure 8. Typical high resolution 3D and 2D AFM topographic images of (a) FTO (b) TiO$_2$ (c) CdS (d) CdTe (e) PEDOT:PSS (f) CuPc thin films.

Figure 9. I–V characteristics of solar devices A and B.

4. Conclusions

In summary, we have investigated the effect of CuPc (HTL2) along with PEDOT:PSS (HTL1) in CdS/CdTe thin film planar heterojunction solar cells. Incorporation of CuPc in the device architecture showed the higher conversion efficiency of 2.74%, due to its effective transport of charge carriers towards the counter electrode

(Au) when compared to the device A (1.25%). The proposed solar cell architecture of introducing double hole transport layers will open a new viewpoint for the CdS/CdTe based solar cell designs to achieve higher efficiency. Also, this strategy might be compatible with a broad range of organic photovoltaic materials and offers an effective approach to enhance the performance of CdTe based solar devices. Although the present PCE achieved is low, a better theoretical understanding of the interfaces would help to improve the design and PCE.

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