

Widely Programmable High-Frequency Active RC Filters in CMOS Technology

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Abstract—We propose a circuit technique that enables the realization of widely programmable high-frequency active RC filters in CMOS technology. A fifth-order Chebyshev ladder filter having a digitally programmable 3-dB bandwidth (from 44 to 300 MHz) is used as a vehicle to validate our ideas. The opamp uses feedforward compensation for achieving high dc gain and wide bandwidth. The integrating resistors are realized as a series combination of a triode-operated MOSFET and a fixed polysilicon resistor. A charge-pump-based servo loop servoes the integrating resistor to a stable off-chip resistor. The principle of “constant capacitance scaling” is applied to the opamp and the integrating resistors so that the shape of the frequency response is maintained when the bandwidth is scaled over a $7 \times$ range. The filter core, designed in a $0.18\text{-}\mu\text{m}$ CMOS process, consumes 54 mW from 1.8-V supply and has a dynamic range of 56.6 dB.

Index Terms—Active filter, CMOS, compensation, continuous-time, feedforward, measurement, programmable.

I. INTRODUCTION

HIGH-FREQUENCY filters with *wide programmability* are important in several signal chains like hard-drive/CD/DVD electronics, where they are used for antialiasing and partial channel equalization. They are also relevant in multistandard radios (see, for example, [1]). The opamp RC architecture is attractive in such applications—the excellent linearity and low excess noise of active RC integrators can result in filters that consume very low power for a given dynamic range. However, designing high-frequency opamp RC filters is problematic, since the gain-bandwidth product of the opamps in an active RC biquad must be much larger than twice the f_oQ product of the highest quality pole pair of the filter transfer function. Moreover, the low-output-impedance stage required for the opamp is power hungry and has swing limitations. These problems can be avoided by replacing the opamp by an operational transconductance amplifier (OTA) with a sufficiently large transconductance [2]. Even so, the active RC architecture is (mostly) avoided at high frequencies due to the difficulties associated with the design of OTAs with adequate gain and bandwidth in low-voltage CMOS processes.

To address these issues, a power-efficient active RC integrator using a feedforward-compensated OTA was proposed in

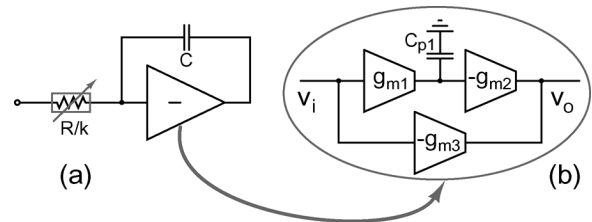


Fig. 1. (a) Programmable integrator of [3] and (b) single-ended block diagram of the OTA.

[3]. The tunable integrator and the single-ended block diagram of the OTA used in that work are shown in Fig. 1(a) and (b). The unity gain frequency of the integrator is programmed by using a resistor array. In the OTA, transconductors g_{m1} and g_{m2} are cascaded to achieve high dc gain. g_{m3} is a feedforward transconductor, which introduces a left-half plane zero. When compared to a two-stage design, this structure is advantageous due to the following. The Miller capacitor required for compensation in a two-stage design needs to be charged and discharged at high frequencies, thereby necessitating significant bias current in the second stage. Since this is avoided in the feedforward-compensated structure, it is fundamentally more power efficient. This is borne out by the experimental results presented in [3]—where the authors report a filter with a maximum bandwidth of 350 MHz, consuming only 14 mA from a 1.8-V supply and achieving a dynamic range of 52 dB. The same authors present a 500-MHz antialias filter in [4], where a three-stage feedforward-compensated OTA is used. Several authors have since used feedforward-compensated opamps in active RC filters (see, for example, [5]). Feedforward compensation of opamps is not a new technique—several authors [6]–[8] make the observation that high dc gain and good phase margin can be obtained with such structures even in low-voltage CMOS processes.

While the results achieved in [3] and [4] are impressive, observing the measured results reveals that the shape of the frequency response varies significantly as the bandwidth setting is changed. Recall that the filter bandwidth is programmed by varying the integrating resistors, while keeping the OTA unchanged. This tuning strategy is problematic due to the following. At low-filter-bandwidth settings, the excess phase lag introduced by the nonidealities in the OTA is small, resulting in a filter response close to the desired response. When the bandwidth setting is increased, the excess phase increases. This results in Q enhancement in the filter and a peaking in frequency response at the band edge. One solution to this problem is to

Manuscript received February 03, 2008; revised April 02, 2008 and May 22, 2008. First published July 22, 2008; current version published February 11, 2009. This paper was recommended by Associate Editor J. Silva-Martinez.

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Digital Object Identifier 10.1109/TCSI.2008.2001759

design an OTA with so large a bandwidth that the integrator excess phase remains very small for all bandwidth settings. Designing such wideband OTAs would lead to significant power dissipation.

It is thus seen that the usual strategy of scaling only the integrating resistors while keeping the OTA unchanged results in a filter response whose shape varies with the bandwidth setting as seen in several reported works [3], [4], [9]. The problems associated with bandwidth programmability occur in all filter architectures. In the specific case of transconductance–capacitance filters, the use of constant- C -scaled integrators [10] mitigates this problem. In [11], the authors address the problem in baseband active RC filters. The strategy they adopt is to appropriately vary the gain–bandwidth product of the Miller compensated opamp as the bandwidth is programmed. This is accomplished by using a compensating capacitor array in the place of a fixed capacitor and a programmable first stage, thereby rendering the excess phase shift caused by the opamp independent of the bandwidth setting. While this might be sufficient for low-frequency filters, the use of switches in the signal path and scaling-only-selected transconductors does not seem to be an effective technique when the filter bandwidths are in the range of several hundreds of megahertz.

In this paper, we present an active RC technique that enables the design of high-frequency filters while maintaining frequency-response shape when the bandwidth is programmed over a wide range. The basic idea is to use the “constant-capacitance scaling” principle, hitherto applied to high-speed G_m - C filters, in active RC filters. The rest of this paper is organized as follows. Section II describes constant- C -scaled active RC integrators. These integrators employ constant- C -scaled feedforward-compensated OTAs. A fifth-order singly terminated Chebyshev active RC ladder filter is used as a vehicle to demonstrate the efficacy of the proposed techniques. Implemented in a $0.18\text{-}\mu\text{m}$ CMOS process, the 3-dB bandwidth of the filter is digitally programmable from 44 to 300 MHz [12]. The test chip incorporates a resistor servo loop, an efficient bias-distribution technique, and provisions for accurate testing of the packaged prototype. The design of the filter and the supporting circuitry is discussed in Section III. Experimental results of prototype chips are shown in Section IV. As expected, the shape of the frequency response is maintained over the $7\times$ programming range. At the highest bandwidth setting, the filter core achieves a dynamic range of 56.6 dB, while consuming 54 mW from a 1.8-V supply. Conclusions are given in Section V.

II. CONSTANT- C -SCALED ACTIVE RC INTEGRATORS

To preserve the shape of the frequency response of a linear network when the bandwidth is programmed, it is necessary to scale *all* the poles and zeros of the network by the same factor. One way of ensuring this in a network of transconductors is constant-capacitance scaling—where *all* conductances/transconductances in a network are multiplied by a factor α , while *all* capacitances (both intentional and parasitic) remain unchanged. It can also be shown [13] that the integrated output noise of the network (considering thermal noise) and maximum signal-handling capability of the network (when it is nonlinear) are preserved under constant- C scaling.

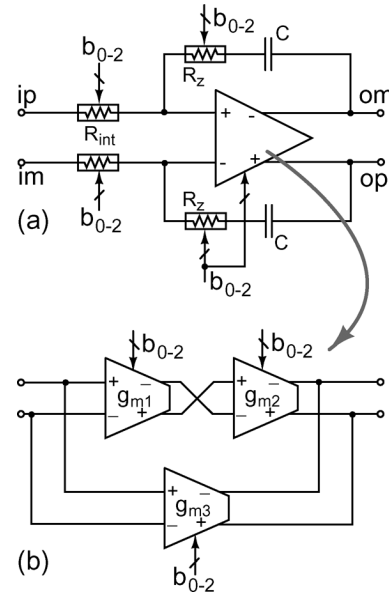


Fig. 2. Schematic of constant- C -scaled (a) active RC integrator and (b) OTA.

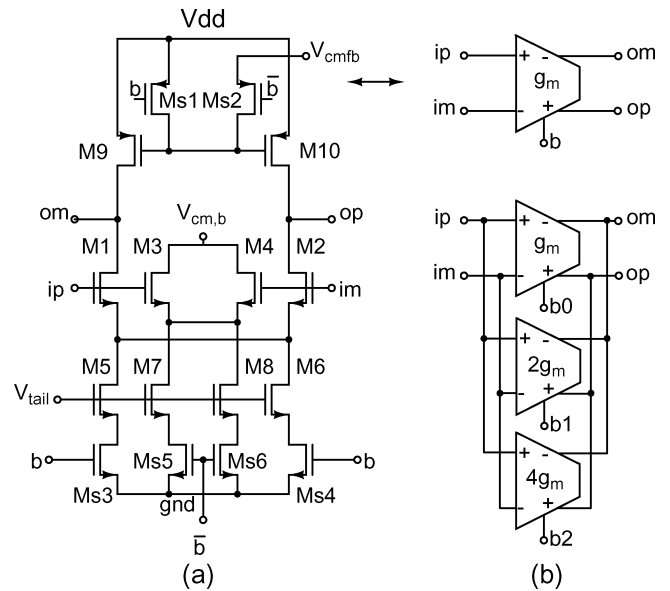


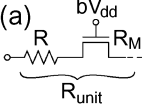
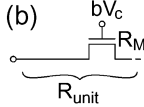
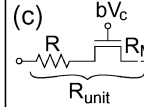
Fig. 3. (a) Unit constant- C G_m -Cell. (b) Binary weighting of unit cells to realize a 3-bit programmable constant- C transconductor.

The constant- C -scaled programmable active RC integrator proposed in this paper is shown in Fig. 2(a). R_{int} and R_z are the digitally programmable integrating resistor and feedforward-compensating resistor, respectively. The OTA is constant- C scaled and based on the topology of Fig. 1(b). All the (trans)conductances in the OTA, R_{int} and R_z , are digitally programmed by a 3-bit word ($b_0 - b_2$).

A. Programmable OTA

The block diagram of the programmable OTA used in this paper is shown in Fig. 2(b). Transconductors g_{m1} and g_{m2} form the main signal path, and g_{m3} forms the feedforward path. Each transconductor is made 3-bit programmable by connecting binary-weighted constant- C unit transconductors in parallel as shown in Fig. 3(b). The schematic of the

TABLE I
CHOICES FOR IMPLEMENTING THE UNIT RESISTOR

	(a) bV_{dd}	(b) bV_c	(c) bV_c
			
R_M/R_{unit}	$\ll 1$	1	< 1
Parasitics	Large	Small	Medium
Linearity	High	Medium	High
Control	No	Yes	Yes

unit transconductor is shown in Fig. 3(a). M1–M2 forms the main differential pair, the tail current of which is formed by M5–M6. The differential pair is turned on/off by switching the tail currents using triode-operated MOSFETs Ms3–Ms4. M9–M10 forms the pMOS load and are switched on/off using triode-operated MOSFETs Ms1–Ms2. Transistors M3–M4 form the dummy differential pair with M7–M8 as tail-current sources and Ms5–Ms6 as switches. When the main pair is “on,” the dummy pair is “off,” and vice versa. It can be shown that connecting many such unit transconductors in parallel results in a network where all nodal capacitances remain independent of the number of unit transconductors that are “on,” while all (trans)conductances scale in proportion to the number of active elements [10]. The tail currents of the differential pairs in the OTA are derived from a fixed-transconductance-bias circuit to keep the transconductance of the differential pair intact over process and temperature. The transconductance of each programmable transconductor cell in the OTA at the maximum bandwidth setting is 7 mS.

B. Programmable R_{int}

The programmable integrating resistor is realized by connecting binary-weighted unit resistances in parallel. The unit resistance used for this purpose can be realized in several ways as shown in Table I. We denote the resistance of the MOSFET and the unit resistor by R_M and R_{unit} , respectively. b is the control bit and takes on values of zero or one. Part (a) in the table shows a switch in series with a fixed polysilicon resistor. The switch is made large, so that $R_M/R_{unit} \ll 1$. Although this strategy has good linearity, the large parasitic capacitances associated with the switch are problematic in high-frequency filters. There is also no control over the integrating resistor across process and temperature.

An alternative approach is to use a MOSFET, operated in triode region (part (b) of Table I). A tuning loop is used to control the conductance of the MOSFET. The parasitics of the MOSFET are not a problem, as a small device is sufficient to realize the desired resistance. However, it suffers from poor linearity when compared to a polysilicon resistor.

Part (c) in Table I combines the merits of parts (a) and (b) and is used in this paper. Here, the resistance is realized as a series combination of a triode-operated MOSFET resistance and a fixed resistor. The resistance of the MOSFET is made a small percentage of the total resistance. This reduces the signal swing across the MOSFET, increasing the linearity. R_{unit} can be kept constant across process and temperature by tuning the MOSFET

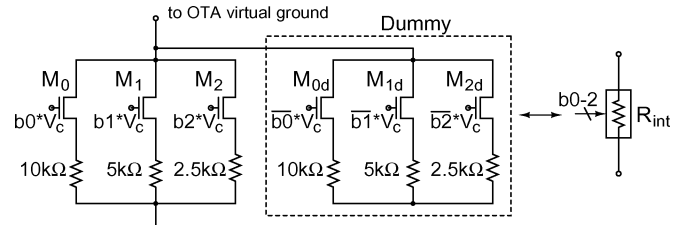


Fig. 4. Programmable integrating resistor.

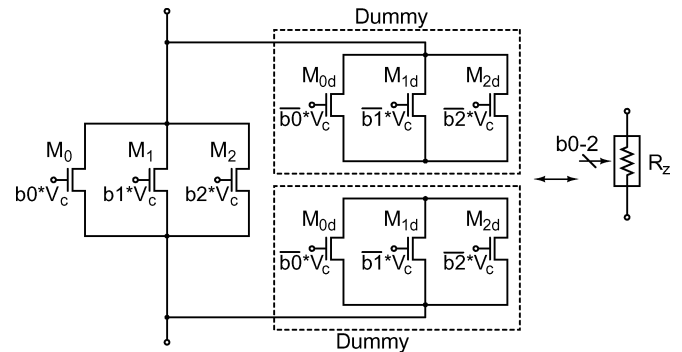


Fig. 5. Programmable compensating resistor.

resistance. In our design, the MOSFET contributes about 15% of R_{unit} . A servo loop controls the resistance of the transistor, so that R_{int} is relatively constant over process and temperature. To reduce the size of the transistor, its gate is boosted above the supply voltage.

Fig. 4 shows the complete 3-bit programmable integrating resistor. The resistance of the array is controlled using logic signals $b_0 - b_2$. The “switch-end” of the array is connected to the OTA virtual ground. Dummy resistors and switches are used in an attempt to keep the capacitance at the virtual-ground node the same, irrespective of the bandwidth setting. M_{d0} , M_{d1} , and M_{d2} are the dummies corresponding to M_0 , M_1 , and M_2 , respectively. Simulations show that maintaining the capacitance constant at the OTA virtual ground is critical. At the highest bandwidth setting, R_{int} is 1.67 k Ω .

C. Programmable R_z

The programmable resistor R_z compensates for the excess phase of the integrator caused by the feedforward effect of the integrating capacitor. It is realized using a bank of three binary-weighted MOS transistors operated in the triode region, as shown in Fig. 5. Since R_z is small when compared to the impedance of the integrating capacitor in the frequency band of interest, the swing across it is small, and distortion is not an issue. Dummy transistors are used to maintain constant- C scaling. A tuning loop is used to stabilize R_z over process and temperature variations.

Fig. 6 shows the benefits of constant- C scaling in a fifth-order Chebyshev ladder filter as its bandwidth is programmed over a $7\times$ range. The details of the filter implementation are discussed in the next section. The responses in the figure are from transistor-level simulations. Fig. 6(a) shows the simulated responses when only the resistors are programmed to vary the bandwidth, with the OTA bandwidth fixed to the highest value (the usual

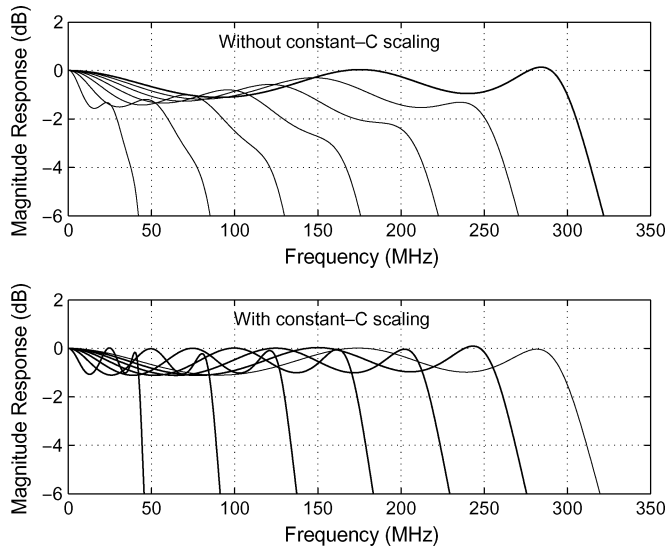


Fig. 6. Simulated filter response (a) without constant- C scaling, only R_{int} is varied to change bandwidth and (b) with constant- C -scaled OTA, R_{int} , and R_z .

technique used to achieve programmability). The filter is design centered at the highest bandwidth setting. Notice that the frequency response droops as the bandwidth setting is progressively reduced—at the lowest bandwidth setting, the third maximum of the response, characteristic of the Chebyshev approximation, has drooped by more than 6 dB. Fig. 6(b) shows the simulated passband responses when a constant- C -scaled OTA, R_{int} , and R_z are used. The dramatic improvement in performance is apparent.

From the viewpoint of integrator performance, the dc gain remains unchanged as the bandwidth is programmed due to the following—the OTA g_m 's are *increased* when the integrating resistors are decreased, resulting in a constant $g_m R$ product. Furthermore, since all the nodal capacitances remain constant, the excess phase of the integrator remains constant irrespective of the bandwidth setting. Thus, predistortion of the filter transfer function at one bandwidth setting remains valid at other bandwidth settings, resulting in a response shape that does not change as the bandwidth is programmed [as shown in Fig. 6(b)].

III. FIFTH-ORDER LADDER FILTER DESIGN

A fifth-order Chebyshev filter with 1-dB passband ripple was chosen as a vehicle to test the ideas in the previous sections. The bandwidth is 3-bit digitally programmable over a $7 \times$ range from 44 to 300 MHz. The filter is implemented as a singly terminated ladder. A single-ended node-scaled version of the filter is shown in Fig. 7. The element values shown are for the highest bandwidth setting of 300 MHz. Metal-insulator-metal capacitors are used as the integrating elements.

A. OTA Design

The schematic of the OTAs used is shown in Fig. 2(b). They are feedforward-compensated constant- C -scaled structures, with $g_{m1} = g_{m2} = g_{m3}$. Each OTA consumes about 4 mA. The schematic of the transconductors used is shown in Fig. 3. Minimum-length transistors are used for the input devices to reduce the parasitic capacitance at the virtual ground of the

OTA. The pMOS loads use devices with twice the minimum length. The tail currents of all the transconductors are derived from a “fixed-transconductance-bias” generator. The details of the fixed- g_m -bias circuit and the bias-distribution technique are described later in this section.

B. CMFB Circuit

The output common-mode voltage of each stage of the OTA is fixed by a separate common-mode feedback (CMFB) loop. Fig. 8 shows the CMFB circuitry. A resistive common-mode detector is used for linearity. The sensing resistors R_{cm} are very large (220 k Ω) in relation to the integrating resistors. Such large-valued resistors can be realized, owing to the 1 k Ω /square polysilicon layer available in the process. Feedforward capacitors C_{cm} (30 fF) are used to avoid the degradation of the loop phase margin due to the distributed capacitance of the resistors. The detected common-mode level is compared with a reference voltage, and the resulting error is amplified using an error amplifier formed by M1–M4. The source follower (M7) and C_c (2 pF) form the compensating network for the CMFB loop. The two CMFB circuits required per OTA consume about 2 mA.

C. Resistor Servo Circuit

To achieve good linearity and smaller device parasitics, the triode-operated MOS transistors in the integrating and feedforward-compensating resistor arrays (denoted by R_i and R_z , respectively) are biased with gate voltages above the power supply. A resistor servo loop adjusts the value of the gate voltages so that R_i and R_z track an external resistor. The simplified schematic of the servo loop is shown in Fig. 9. V_{bat} is a battery that boosts the control voltage above the supply. It is seen that, if the opamps are ideal, $R_i = R_{\text{ext}}/\alpha$ and $R_z = R_{\text{ext}}/\beta$. The voltage drop across R_{ext} was chosen to be 200 mV. The battery is implemented by a large capacitor (2 pF) charged to an appropriate voltage ($V_{\text{dd}} + V_a$), as shown in Fig. 10.

D. Fixed-Transconductance-Bias Generation

A fixed-transconductance-bias generator that is robust with respect to supply voltage and ambient temperature is used to stabilize the transconductances of the opamp over process and temperature. Fig. 11 shows the fixed-transconductance-bias generator employed in this design [14]. The salient features of this bias generator are the following.

- 1) The generator does not rely on the MOSFET square law, unlike more traditional circuits [15], [16].
- 2) The generated bias current is very tolerant of the large output conductances of short-channel MOSFETs.
- 3) The circuit is robust with power-supply variations.

Referring to Fig. 11, M1 and M2 are devices whose transconductance g_m need to be stabilized. The circuit servos the g_m of M1 and M2 to the stable off-chip conductance $1/R$. Circuit operation can be understood as a negative-feedback system. Any deviation of g_{m1} , M1 from $1/R$ causes the negative feedback to adjust the current through M1 to bring g_{m1} , M1 back to $1/R$. The drain potentials of M1 and M2 are identical and independent of the supply voltage. Simulations (in the absence of mismatch) show that g_m 's of M1 and M2 vary by less than 0.1%

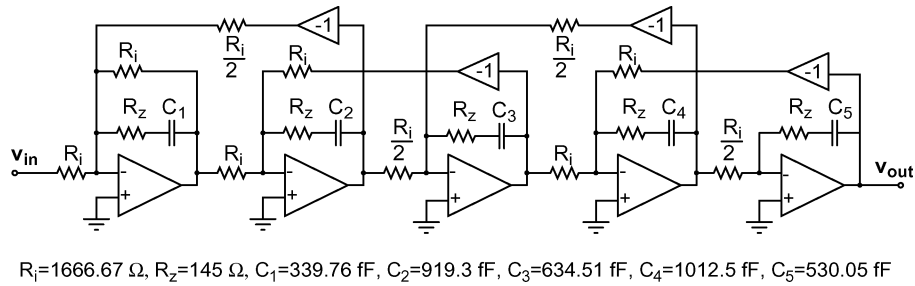


Fig. 7. Single-ended schematic of the filter—component values are for the highest bandwidth setting.

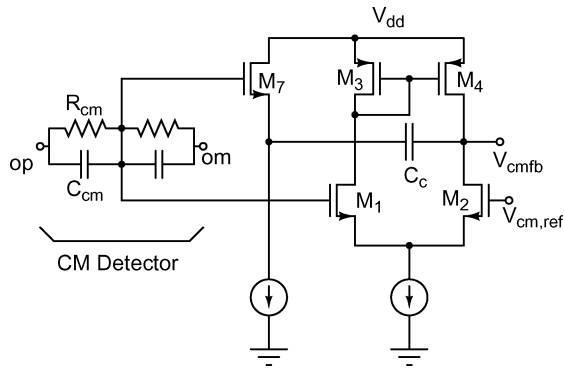


Fig. 8. Simplified schematic of the CMFB circuit.

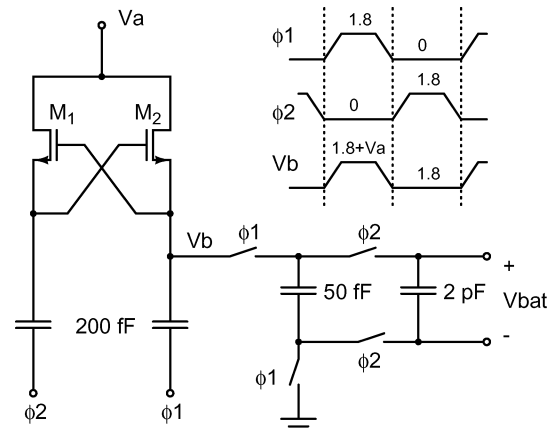


Fig. 10. Charge-pump-based battery generator.

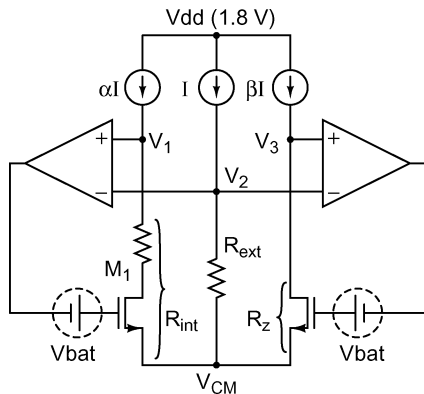


Fig. 9. Simplified schematic of the resistor servo loop.

for a V_{dd} varying between 1.6 and 2.0 V. M_{11} 's drain-current is distributed to all transconductors on the chip.

E. Bias-Distribution System

The current generated by the fixed-Gm bias circuit should be mirrored to all the filter transconductors as accurately as possible. Fig. 12(a) shows the simplest circuit that can be used to do this. I_{bias} is generated in the fixed-Gm bias block and routed to the filter transconductor, where it is converted into a voltage by M_{2r} . M_2 represents the tail-current source of the filter transconductor (the switch used to turn the current source off is not shown for simplicity). Notice that the V_{DS} of M_2 is dependent on V_{cm} , the input common-mode voltage of the filter. During chip layout, M_{2r} and M_2 should be placed in close proximity, which is easy to accomplish. One problem with this approach is that the current in M_2 no longer equals I_{bias} due to the different

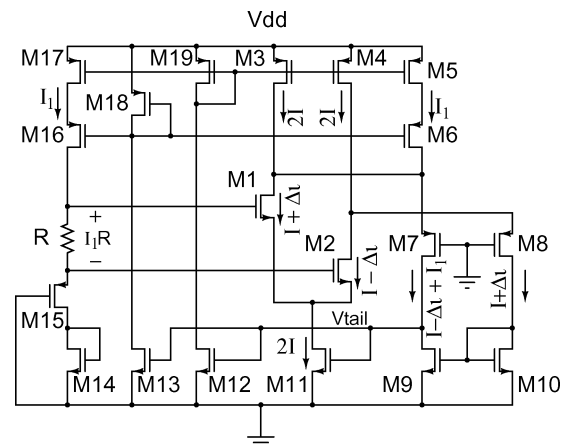


Fig. 11. Fixed-transconductance-bias generation circuit (start-up circuitry not shown).

drain-source voltages of M_{2r} and M_2 . The drain current of M_2 is seen to be $I_{D,M2} = ((1 + \lambda V_{DS,M2}) / (1 + \lambda V_{GS,M2r})) I_{bias}$.

To mitigate this problem, a common solution is to employ the precise current mirror shown in Fig. 12(b). M_{1r} is sized so that it has the same current density as M_1 in the filter. Hence, M_2 and M_{2r} have the same V_{DS} , thereby ensuring that the transconductor current is I_{bias} . C_c compensates the negative-feedback loop formed by M_{2r} , M_{1r} , M_3 , and M_4 . While this approach certainly eliminates systematic error in the drain-current of M_2 , it poses a layout problem due to the following—four devices (M_{1r} , M_{2r} , M_3 , and M_4) need to be placed in close proximity to M_1 and M_2 . C_c is also usually larger than these devices. Since

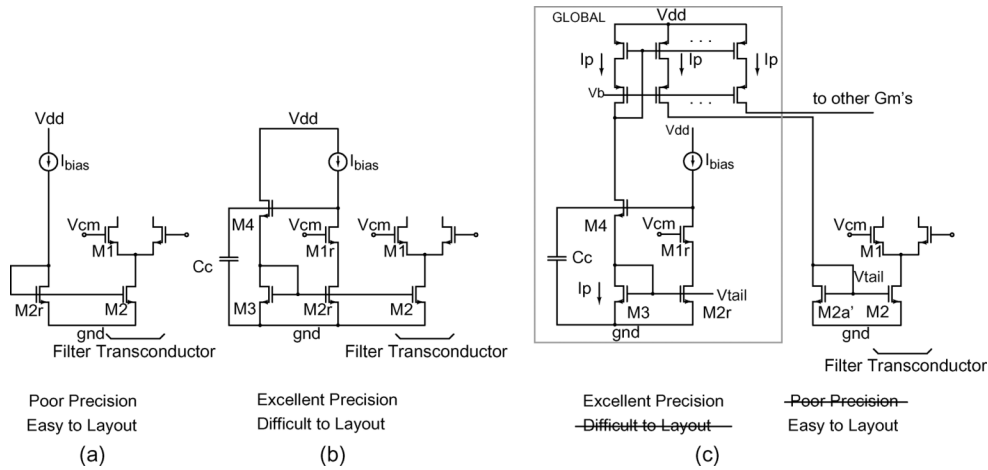


Fig. 12. (a) and (b) Conventional bias-distribution schemes. (c) Proposed technique with the advantages of both schemes.

M1 is a part of the high-speed signal path of the filter, it is preferable that the layout be compact. It is therefore seen that, while the simple technique of Fig. 12(a) is advantageous with respect to layout, it has poor accuracy. On the other hand, the circuit in Fig. 12(b) results in an accurate reproduction of current, while resulting in a suboptimal layout.

The basic idea behind the technique that combines the advantages of both circuits discussed earlier, while avoiding their disadvantages, is the following. Precision of the circuit of Fig. 12(a) could be improved by deliberately modifying I_{bias} to I_p , where $I_p = ((1 + \lambda V_{GS,M2r}) / (1 + \lambda V_{DS,M2})) I_{bias}$. Since I_p is a pre-distorted version of I_{bias} , the percentage error in the drain-current of M2 is seen to be zero. A circuit that generates I_p is shown in Fig. 12(c). The devices shown in the box are global. They are laid out far away from the high-speed signal path. M3 and M2r have identical sizes. It is easy to see that $I_p = I_{bias}((1 + \lambda V_{GS,M2r}) / (1 + \lambda V_{DS,M2r}))$. I_p is sensed by precision pMOS mirrors, and multiple copies of I_p are routed to the individual transconductors. At the transconductor, I_p is mirrored by M2a' – M2, generating I_{bias} in M2. Notice that the layout near the transconductors (the high-speed signal path) is very simple and compact. In practice, M2a' and M2 are merged into the same multifinger structure. While the proposed technique is discussed here in the context of continuous-time filters, it is generic and can be applied to a whole range of analog-circuit blocks. A BiCMOS mirror employing a similar principle was used in [17].

F. Filter Testing

Accurately measuring the frequency response of the filter is a challenge due to the following. Since the filter is not a stand-alone block but intended to be a part of a larger SoC, it is not designed to drive package and board parasitics. On-chip buffers, which are turned on only during test time are used to interface the filter with the external world. The test buffers, the package, and the PCB used for characterization have a frequency response which must be deembedded to determine the characteristics of the filter accurately.

A conventional technique for accurate measurement of on-chip active filters is that proposed in [18], as shown in

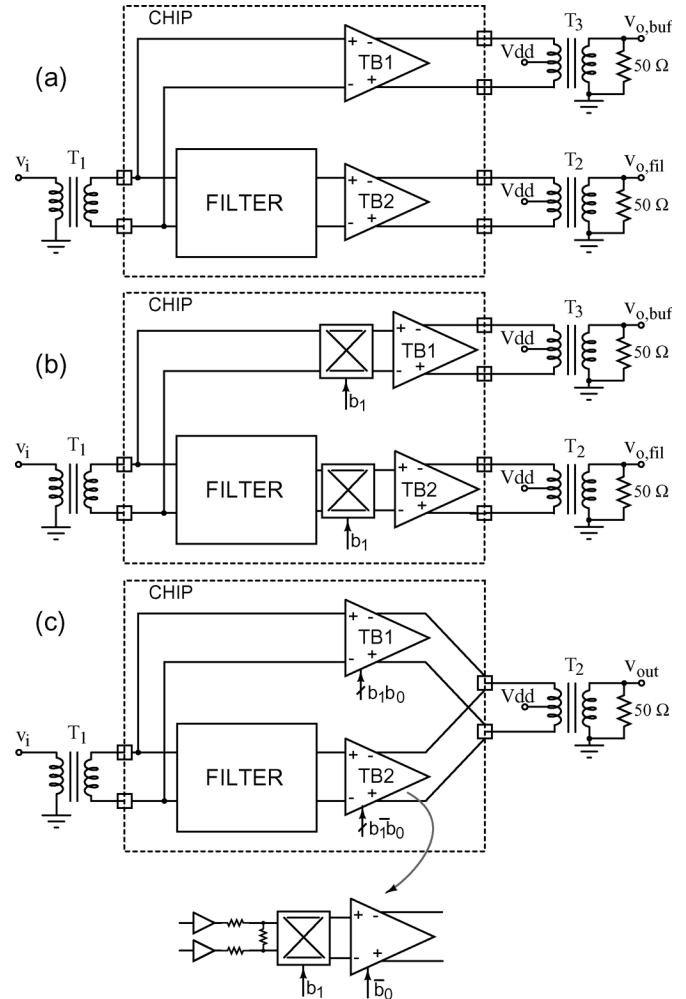


Fig. 13. Measurement of filter frequency response. (a) Conventional technique [18]. (b) Technique with increased accuracy [19]. (c) Improvement over [19] to increase buffer linearity, as well as cancel package feedthrough.

Fig. 13(a). T1 and T2 are baluns that accomplish single ended to differential conversion so that the fully differential filter can be measured with single-ended test equipment. Two measurement paths are created within the filter—one is a direct

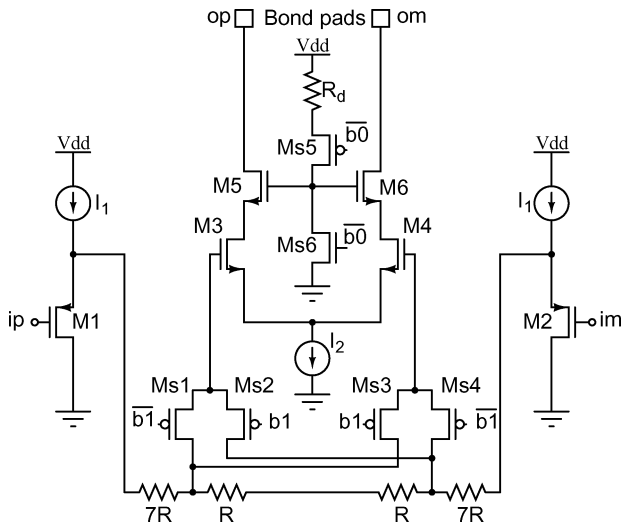


Fig. 14. Simplified schematic of the test buffer.

path that bypasses the filter, and the other is the filter path. Both these paths contain two nominally identical test buffers, TB1 and TB2. It can be shown that, in the absence of package feedthrough, the filter response is the ratio of the responses of the filter path and direct path.

In a recent work [19], it was shown that the measurement technique of [18] is accurate in the filter passband but is prone to error in the filter stopband. The poor stopband-measurement accuracy was attributed to direct feedthrough in the IC package. It was shown experimentally that a simple polarity-reversal-switch network added before the buffers [as shown in Fig. 13(b)] could be used to effectively cancel package feedthrough. However, this technique has a few issues. First, the measurement accuracy is still limited by mismatch between the external measurement paths through the output baluns. The test buffers were implemented as source-follower stages driving a differential pair. While the linearity of a differential pair was adequate to test a G_m - C filter, it is clear that a more linear buffer is needed to accurately measure the distortion of an active RC filter (whose inherent distortion is smaller).

In this paper, we propose an improvement over the test method proposed in [19]. The technique is shown in Fig. 13(c). The outputs of the two test buffers are shorted together so that the external signal paths for the direct and filter measurements remains identical. Only one of these buffers is “on” at any time—thus, either the direct path or the filter path can be activated. Note that the only difference between the direct path and the filter path is the filter itself—the external path (package and PCB) are common to both paths. To improve the linearity of the test buffer, a resistive attenuator is used. A polarity-reversal-switch network is placed between the attenuator and the differential pair following the attenuator. This is used to cancel the effect of package feedthrough, as discussed in [19].

Fig. 14 shows the simplified schematic of the test buffer. It has a two-stage design. The first stage is a source follower formed by M1, M2, and current sources I_1 . The second stage is a transconductor formed by M3–M6 and current source I_2 . The first-stage output is attenuated by a factor of eight using a resistor divider.

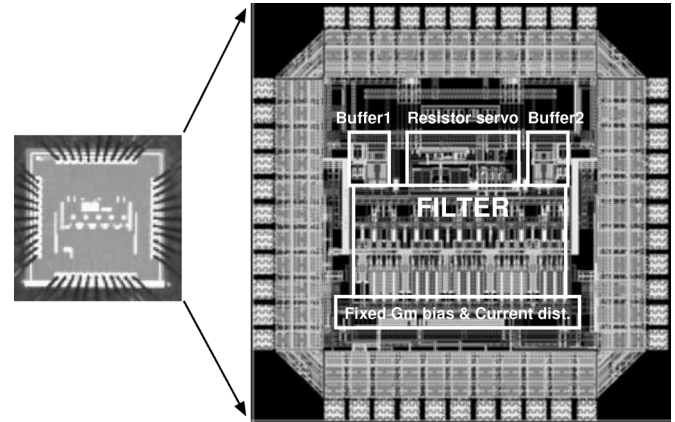


Fig. 15. Die photograph and top-level layout.

This enhances the linearity of the following stage at the expense of gain. Having a linear test buffer is important as the DUT is an active RC filter (which is expected to be linear). The output of the resistor divider is connected to the second stage (which is a cascoded differential pair) through a set of polarity-reversal switches implemented using transistors Ms1–Ms4. The gain polarity of the buffer (+ or –) is controlled by the bit $b1$. The control bit $b0$ is used to power down the buffer. When $b0$ is low, all the bias currents and the bias voltage for the cascode transistors M5–M6 are switched off. R_d damps any potential common-mode oscillation of the cascode and the package inductance. Each test buffer consumes 15 mA and is only turned on at test time.

IV. MEASUREMENT RESULTS

The filter test chip was fabricated in a $0.18\text{-}\mu\text{m}$ CMOS process through the Europractice program. The die photograph and the top-level layout of the chip are shown in Fig. 15. The filter has an active area of 0.63 mm^2 and is mounted in a 44-pin JLC package.

A. Frequency-Response Measurements

Fig. 16 shows the measured frequency response of the filter for all bandwidth settings. The passband details are shown in the inset. It is seen that, owing to constant- C scaling, the shape of the response remains virtually unaltered in spite of being programmed over a $7\times$ range.

Fig. 17 shows the normalized response of 15 chips on the same plot, at the highest and lowest (in the inset) bandwidth settings. Good repeatability is seen.

B. Noise Measurements

Fig. 18 shows the measured noise spectral density at the output of the filter for all bandwidth settings. To make accurate measurements in spite of the high-noise figure of the spectrum analyzer, the filter output is amplified by a low-noise amplifier before being fed into the spectrum analyzer. The technique described in [19] was used to account for the frequency-dependent gain of the measurement paths. The rms output noise is $860\text{ }\mu\text{V}$, rms at the highest bandwidth setting and increases to 1.3 mV , rms at the lowest bandwidth setting. The increase in

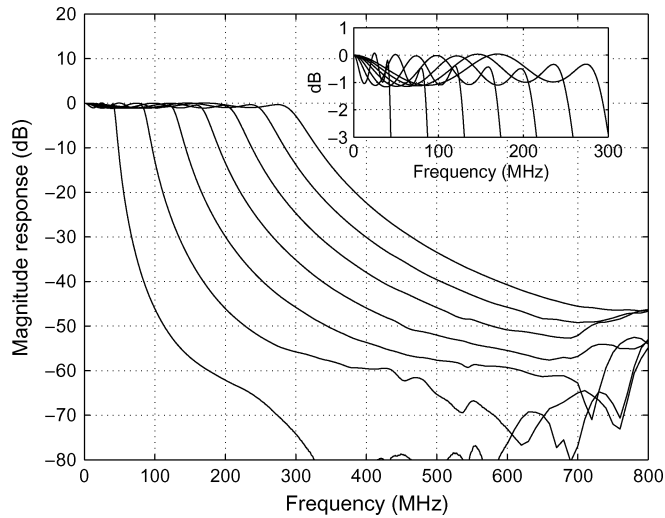


Fig. 16. Measured frequency response across all bandwidth settings.

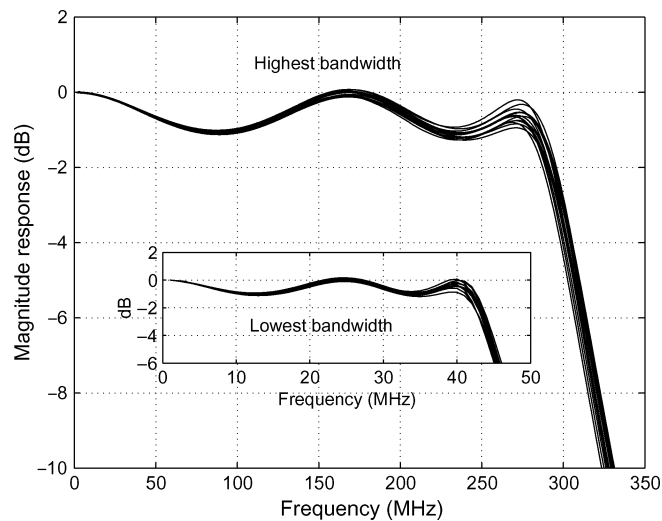


Fig. 17. Passband detail for 15 chips at the highest and lowest bandwidth settings.

the integrated noise for lower bandwidths is due to $1/f$ noise. The charge-pump-based resistor servo loop introduces clock feedthrough into the filter. The inset in Fig. 18 shows a zoomed version of the filter-output noise spectral density (for the lowest bandwidth setting). The clock frequency used in the charge pump is 1 MHz.

C. Distortion Measurements

Owing to the use of active RC integrators, the measured third-harmonic distortion of the filter is 1% for a peak-to-peak differential input as large as 2.2 V. For the distortion test, the test tone was applied at one-third the band-edge frequency (which corresponds to the worst case tone for distortion measurement). The dynamic range of the filter for 1% harmonic distortion was measured as 56.6 dB for the highest bandwidth setting.

A two-tone test was performed to determine the intermodulation performance of the filter. Fig. 19 shows the IIP_3 of the filter as a function of the average frequency of the two input

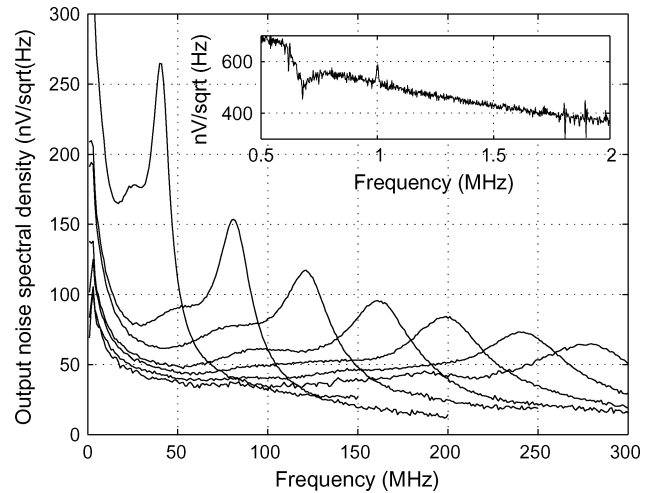


Fig. 18. Measured noise spectral density of the filter output.

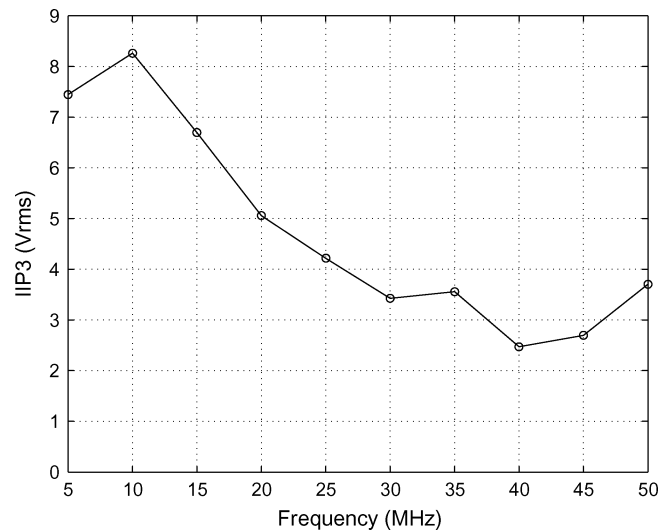
Fig. 19. Measured IIP_3 of the filter as a function of frequency for the lowest bandwidth setting.

TABLE II
SUMMARY OF MEASUREMENT RESULTS

Technology	0.18 μm CMOS
Filter type	5 th order Chebyshev, Opamp-RC
Supply voltage	1.8 V
3 dB bandwidth	44–300 MHz
Active chip area	0.63 mm ²
Power (filter core)	54 mW
Integrated output noise	860 μV rms
IIP_3 @ band-edge	2.5 V rms
Test tone at $\frac{f-1\text{dB}}{3}$	
$V_{in,pp}$ differential for THD \leq -40 dB	2.2 V
Dynamic range for THD \leq -40 dB	56.6 dB

tones. For this test, the filter was set to the lowest bandwidth (44 MHz). The lowest IIP_3 is 2.5-V rms (the filter is “most nonlinear”) and occurs (as expected) at the band edge, since all the opamp output swings are large when the input-frequency content is at the band edge.

Table II summarizes the measured results.

TABLE III
COMPARISON WITH SOME PUBLISHED FILTERS

Reference	Bandwidth (MHz)	Order	Supply voltage (V)	Power (mW)	Q_{max}	Dynamic range (dB) (for THD ≈ -40 dB unless specified)	Topology	Technology	FOM (aJ)	Comments
[3]	350	5	1.8	25.2	3.1	52	Active-RC	0.18 μm CMOS	29.3	4X programmability 4 dB peaking
[4]	500	5	1.8	90	3.1	64	Active-RC	0.18 μm CMOS	4.6	5X programmability 6 dB peaking
[20]	500	5	3.3	100	5.55	52	Gm-C	0.35 μm CMOS	45.4	7X programmability 0.5 dB droop
[21]	550	4	± 1.65	140	1.065	40	Gm-C	0.35 μm CMOS	5781	Fixed bandwidth
[22]	200	4	2.3	72	1.065	52	Gm-C	0.35 μm CMOS	651.6	2.5X programmability
[23]	120	8	2.5	120	1.5	45	Gm-C	0.25 μm CMOS	2633	4X programmability
This work	300	5	1.8	54	5.55	56.6	Active-RC	0.18 μm CMOS	14.1	7X programmability No peaking

Table III compares this paper with recently reported high-frequency CMOS filters. The figure of merit (FOM) used for comparison is [2]

$$\text{FOM} = \frac{P_{\text{diss}}}{pQ_{\text{max}}f_oDR^2} \quad (1)$$

where P_{diss} is the power dissipation, p is the number of filter poles, f_o is the filter cutoff frequency, Q_{max} is the maximum quality factor of the filter poles, and DR is the dynamic range. A lower FOM indicates a more power-efficient design. [3] is a design with a feedforward OTA design similar to that used in this paper. However, the shape of the response changes significantly as the bandwidth is programmed. [4] uses a three-stage feedforward opamp in a 500-MHz filter design. The power dissipation does not include contributions from the tuning or bias-distribution circuitry. Since the OTA is kept fixed as the bandwidth setting is varied, the shape of the response changes with bandwidth setting. [20]–[23] are Gm- C filter designs. [20] achieves a 500-MHz bandwidth with a sharp transition band in a 0.35- μm process. As expected, the power efficiency is not as good as that in the active RC case. It is seen that the filter presented in this paper compares favorably with others reported in the literature—particularly considering that the frequency-response shape is maintained over a $7\times$ range.

V. CONCLUSION

Design considerations for widely programmable active RC integrators were given. A constant- C programmable active RC integrator based on a feedforward OTA was proposed. This integrator has the same dc gain and excess phase at all bandwidth settings, resulting in a constant frequency-response shape as the bandwidth is programmed over a wide range. This integrator was used as a building block in a fifth-order Chebyshev low-pass filter with a 3-dB bandwidth programmable from 44 to 300 MHz. The theory is borne out by measured results from a test chip fabricated in a 0.18- μm CMOS process. At the highest bandwidth setting, the filter achieves a dynamic range of 56.6 dB while consuming 54 mW from a 1.8-V supply.

REFERENCES

- [1] T. Hollman, S. Lindfors, M. Lansrinne, J. Jussila, and K. Halonen, "A 2.7-V CMOS dual-mode baseband filter for PDC and WCDMA," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1148–1153, Jul. 2001.
- [2] Y. Tsvividis, "Integrated continuous-time filter design—An overview," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 166–153, Mar. 1994.
- [3] J. Harrison and N. Weste, "350 MHz opamp-RC filter in 0.18 μm CMOS," *Electron. Lett.*, vol. 38, no. 6, pp. 259–260, Mar. 2002.
- [4] J. Harrison and N. Weste, "A 500 MHz CMOS anti-alias filter using feedforward op-amps with local common-mode feedback," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2003, vol. 1, pp. 132–483.
- [5] J. Hwang, M. Lee, C. Jeong, and C. Yoo, "Active-RC channel selection filter tunable from 6 kHz to 18 MHz for software-defined radio," in *Proc. IEEE ISCAS*, 2005, pp. 4803–4806.
- [6] M. Schlarmann, E. Lee, and R. Geiger, "A new multipath amplifier design technique for enhancing gain without sacrificing bandwidth," in *Proc. IEEE ISCAS*, 1999, vol. 2, pp. 610–615.
- [7] B. Thandri, J. Silva-Martinez, and F. Maloberti, "A feedforward compensation scheme for high gain wideband amplifiers," in *Proc. ICECS*, 2001, vol. 3, pp. 1115–1118.
- [8] B. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 237–243, Feb. 2003.
- [9] H. Khorramabadi, M. Tarsia, and N. Woo, "Baseband filters for IS-95 CDMA receiver applications featuring digital automatic frequency tuning," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1996, pp. 172–173.
- [10] S. Pavan, Y. Tsvividis, and K. Nagaraj, "Widely programmable high-frequency continuous-time filters in digital CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 503–511, Apr. 2000.
- [11] S. D'Amico, V. Giannini, and A. Baschirotto, "A 4th-order active-Gm-RC reconfigurable (UMTS/WLAN) filter," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1630–1637, Jul. 2006.
- [12] T. Laxminidhi, V. Prasadu, and S. Pavan, "A low power 44–300 MHz programmable active-RC filter in 0.18 μm CMOS," in *Proc. Custom Integr. Circuits Conf.*, Sep. 2007, pp. 77–80.
- [13] S. Pavan and Y. Tsvividis, "Time-scaled electrical networks—Properties and applications in the design of programmable analog filters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 2, pp. 161–165, Feb. 2000.
- [14] S. Pavan, "A fixed transconductance bias technique for CMOS analog integrated circuits," in *Proc. ISCAS*, 2004, vol. 1, pp. 1-661–1-664.
- [15] J. Steininger, "Understanding wideband MOS transistors," *IEEE Circuits Devices Mag.*, vol. 6, no. 3, pp. 21–26, May 1990.
- [16] R. Zele and D. Allstot, "Low power cmos continuous time filters," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp. 157–168, Feb. 1996.
- [17] S. Pavan, M. Tarsia, S. Kudszus, and D. Pritzkau, "Design considerations for integrated modulator drivers in silicon germanium technology," *Int. J. High Speed Electron. Syst.*, vol. 15, no. 3, pp. 477–495, Sep. 2005.

- [18] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, Feb. 1992.
- [19] S. Pavan and T. Laxminidhi, "Accurate characterization of integrated continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1758–1766, Aug. 2008.
- [20] S. Pavan and T. Laxminidhi, "A 70–500 MHz programmable CMOS filter compensated for MOS nonquasistatic effects," in *Proc. Eur. Solid State Circuits Conf.*, Sep. 2006, pp. 328–331.
- [21] P. Panday, J. Silva-Martinez, and X. Liu, "A CMOS 140-mW fourth-order continuous-time low-pass filter stabilized with a class AB common-mode feedback operating at 550 MHz," *IEEE Trans. Circuits Syst I, Reg. Papers*, vol. 53, no. 4, pp. 811–820, Apr. 2006.
- [22] M. Chen, J. Silva-Martinez, S. Rokhsaz, and M. Robinson, "A $2 V_{PP}$ 80–200-MHz fourth-order continuous-time linear phase filter with automatic frequency tuning," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1745–1749, Oct. 2003.
- [23] G. Bollati, S. Marchese, M. Demicheli, and R. Castello, "An eighth-order CMOS low-pass filter with 30–120 MHz tuning range and programmable boost," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1056–1066, Jul. 2001.



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