PERFORMANCE AND RELIABILITY CODESIGN OF DRAIN EXTENDED MOS DEVICES FOR ADVANCED SoC APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

by
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OCTOBER, 2018

DECLARATION

I hereby ***declare*** that the Research Thesis entitled **PERFORMANCE AND RELIABILITY CODESIGN OF DRAIN EXTENDED MOS DEVICES FOR ADVANCED SoC APPLICATIONS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to certify that the Research Thesis entitled **PERFORMANCE AND RELIABILITY CODESIGN OF DRAIN EXTENDED MOS DEVICES FOR ADVANCED SoC APPLICATIONS** submitted by **JHNANESH SOMAYAJI B** (Register Number: 135061EC13F03) as the record of the research work carried out by him, is accepted as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

Prof. M.S.Bhat
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Chairman-DRPC
(Signature with Date and Seal)

Faith,

Its all about *Believing,*

YOU DON'T KNOW, HOW IT WILL HAPPEN. BUT YOU KNOW IT WILL

Dedicated to my Parents

Acknowledgements

It is a genuine pleasure to express my deep sense of thanks and gratitude to my mentor and guide **Dr. M. S. Bhat**,Professor, Department of E&C Engineering, NITK Surathkal. The door to his office was always open whenever I ran into a trouble spot or had a question regarding my research or writing. His dedication, keen interest and above all, his overwhelming attitude to constantly support his students at every step has been solely and mainly responsible for the completion of my work. Also, his timely scholarly advices and meticulous scrutiny have helped me to a very great extent to accomplish this task.

I profusely thank **Dr. Navakanta Bhat**, Professor & Chairperson, CeNSE, IISc Bangalore. His timely recommendation with kindness, has enabled me to join ANCL at IISc as an intern.

I owe a deep sense of gratitude to **Dr. Mayank Shrivastava**, Assistant Professor, DESE, IISc, Bangalore, who showered the light to my research work by providing me an opportunity to join his team Advanced Nano-Electronics Computational Laboratory (ANCL) as an intern at IISc. His immense knowledge, insightful comments and encouragement has led me to widen my research perspectives and to complete the work. It is a great honour to work under his supervision.

I am extremely thankful to my friend **B. Sampath Kumar**, Research Scholar, ANCL, DESE, IISc, Bangalore, for his unwavering support, collegiality and mentorship throughout the work at IISc. I would like to extend my thanks to the entire team of ANCL for their generous advices and kind support during my internship.

I would like to express my deepest thanks to **Mr. Puneeth Kumar**, Senior Team Lead, KarMic Design Pvt. Ltd., Manipal, for his kind endless help in solving software related issues.

Besides my advisor, I would like to thank the rest of my RPAC committee: **Dr. U. Shripathi Acharya**, Professor and Head, Department of E&C Engineering, NITK, Surathkal and **Dr. A. Chittaranjan Hegde**, Professor, Chemistry Dept., NITK, Surathkal, for their valuable comments. I would also like to thank **Dr. Murlidhar Kulkarni**, Professor and Former

Head, Department of E&C Engineering, NITK, Surathkal for his valuable advices and moral support during this research.

My special regards to ECE non-teaching staffs, **Mrs. Pushpalatha, Mr. Sanjeev poojary, Mrs. Amitha, Mr. Subramanya Karanth, Mrs. Prabha, Mrs. Soumya Mr. Tilak and Mr. Ratish**.

Also, I am gratefully indebted to **Mr. Girish Navada**, Assistant Professor, Department of E&E Engineering, NITK, Surathkal and his wife Ramya Navada for inserting the seed of research thought and being a constant support throughout my work.

I thank my friends at NITK for accompanying the sleepless nights at research labs especially before deadlines, and for all the fun we have had in the last five years.

This research was supported by MHRD, Government of India. I would like to thank the organization for providing me with the financial support.

Finally, I must express my very profound gratitude to my parents for providing me with unfailing support throughout my years of study.

Last but not the least, I thank my goddess of wisdom for always being there in my beliefs.

Abstract

In order to address the demands of advanced functionalities of System on Chips (SoC), interfacing various modules operating at different voltage levels is very much essential. In this work, effectively utilizing the superjunction concept with Drain extended MOS (DeMOS) device is explored for SoC applications. For the first time, design of four different CMOS-compatible DeMOS devices, namely, Double and Triple RESURF (Single Superjunction (SJ) devices) and Multiple RESURF (Multiple Superjunctions-I and II) devices is studied for optimized breakdown voltage and on-resistance parameters. The work investigates the primary parameters of the devices relating to p-implant. The device parameters are optimized to maximize the breakdown voltage (V_{BD}) to on-resistance (R_{ON}) ratio. The superjunction concept has helped in improving the breakdown voltage by 2× without affecting the on-resistance or has allowed reducing on-resistance by 2.5× without changing the breakdown voltage. Also, hot carrier generation, safe operating area concerns and electrostatic discharge (ESD) reliability behavior is studied for various superjunction DeMOS structures and is compared with conventional DeMOS device. Further, the work is extended to tri-gate structures. Four different Drain extended FinFET devices are proposed, namely, Silicon On Insulator based, p-stop based, well doped with and without p-implant structures. The devices are designed and simulated to explore the suitability of DeFinFETs for sub-micron high voltage applications. The well doped DeFinFET devices give the best performance metrics compared to SOI and p-stop based DeFinFETs.

Keywords: RESURF, Superjunction, Drain Extended MOS, Breakdown voltage, On-resistance, ESD, HCI, SOA Drain extended FinFETs.

Contents

List of Figures

List of Tables

Abbreviations

Abbreviation	Expansion
BOX	Buried OXide
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DeMOS	Drain extended Metal Oxide Semiconductor
DeFinFET	Drain extended Fin Field Effect Transistor
ESD	Electro Static Discharge
HCI	Hot Carrier Injection
I/O	Input/Output
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PIC	Power Integrated Chip
PAE	Power Amplification Efficiency
RESURF	REduced SURface Field
RF	Radio Frequency
SAD	Substrate Assisted Depletion
SJ	Superjunction
SHE	Spherical Harmonic Expansion
SOI	Silicon On Insulator
SoC	System-on-Chip
SOA	Safe Operating Area
STI	Shallow Trench Isolation
TCAD	Technology Computer Aided Design

Chapter 1

Introduction

1.1 Background

Ever increasing use of portable battery operated devices such as smart phones, PDAs, MP3 players, laptops, digital cameras etc., have led to the growing research interest in Power Integrated Circuits (PICs). Power devices with medium range (5 - 25V) of breakdown voltages form an integral part of many PICs in the sub- 100nm technology nodes. Power management modules play an important role in these systems where longer battery operating time and power saving features are the matters of concern. The most important block in power management modules is the output power stage that regulates or switches large amount of power to the functional unit.

Over the last decade, the technology of power semiconductors has made massive progress. The evolution has led to the development of new power devices in terms of design, size, structure and manufacturing. The entry of MOS technology in power electronics hastened the way of integration as the technology of integrated circuits and power devices has become compatible. This has produced a direct bridge between integrated circuits and the power devices. The most critical step in the evolution of a new generation of power devices is the introduction of power MOSFET. MOS power transistors have definite advantages over bipolar transistors, such as lower power consumption, lower forward voltage and simpler device circuitry requirements. These advantages make MOS transistors extremely useful power devices. In this chapter, power semiconductor market trends, their applications, and the objectives of this thesis are addressed.

Fig. 1.1 shows the growth of semiconductor devices, that have lined up for power

electronics. In the 1960s, thyristor opened up many possibilities for the growth of power electronics and generated the first wave in the history of power semiconductor devices. For the growing demand of power conversion equipment, in the second half of the 1970s, the bipolar transistor module and the gate turn-off thyristor (GTO) started the second wave and became the major focus of power electronics growth.

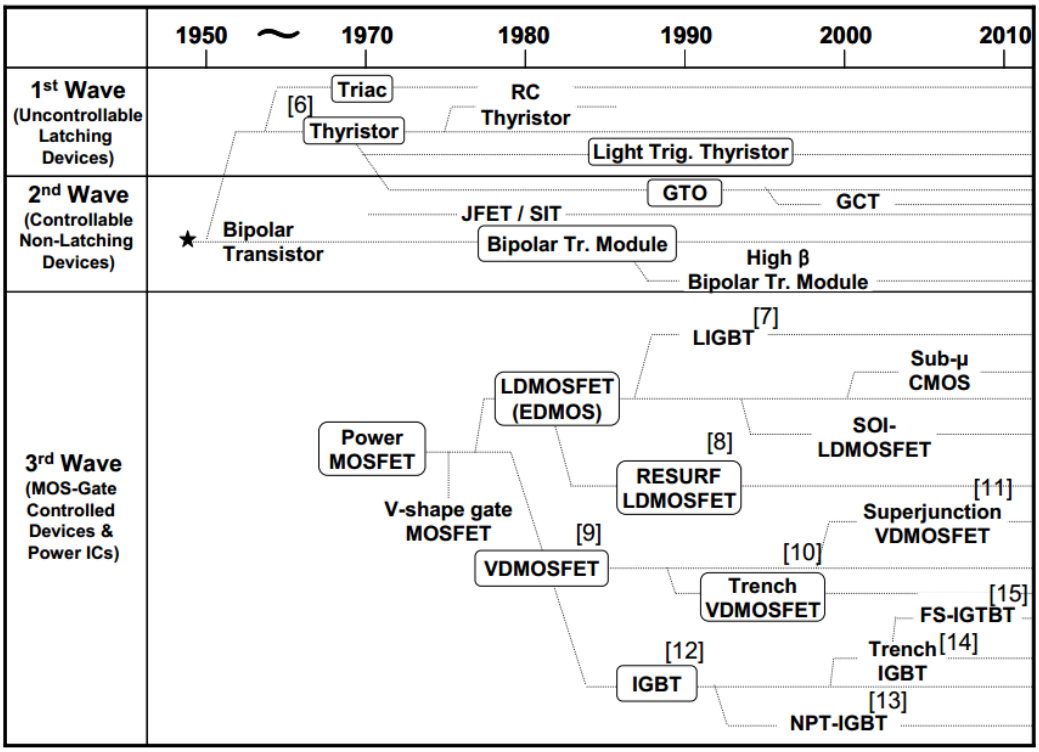


Figure 1.1: Evolution of power semiconductors devices [Yoo (2010)]

During the next decade (1980s and 1990s), the third wave started with the introduction of power MOSFETs. MOS-gate controlled devices were built focusing on the applications that enabled efficient and compact system designs particularly for those that operate on low voltages (<200V). Also, the power MOSFETs such as the DMOS (Double-diffused MOS), IGBT (Insulated Gate Bipolar Transistor), trench gate, RESURF (Reduced SURface Field) technologies were explored in order to improve the performance and reliability aspects. Also to minimize conduction and switching losses, efforts were made to improve the performance during high current/fast switching operations. Enhancing Safe Operating Area (SOA) was a challenge under short circuit related stresses. Gradually, power MOSFETs started gaining at-

tention and today these devices hold major market share in the power semiconductor industry.

1.2 Market trends and Power semiconductor technology

Presently, power management IC technology is one of the major research fields and efficient power devices are central to its reliability and robustness. Fig. 1.2 and 1.3 presents Yole's power management IC market revenue and its market size, respectively, for the period ranging from 2015 to 2022. From Fig. 1.2 it can be observed that power ICs and power modules contribute major revenue to the market share upto $35 billion by 2022. The power semiconductor market is expected to increase at a compound annual growth rate of 3.6% per year to $15.7 billion in 2022 (Fig. 1.3).

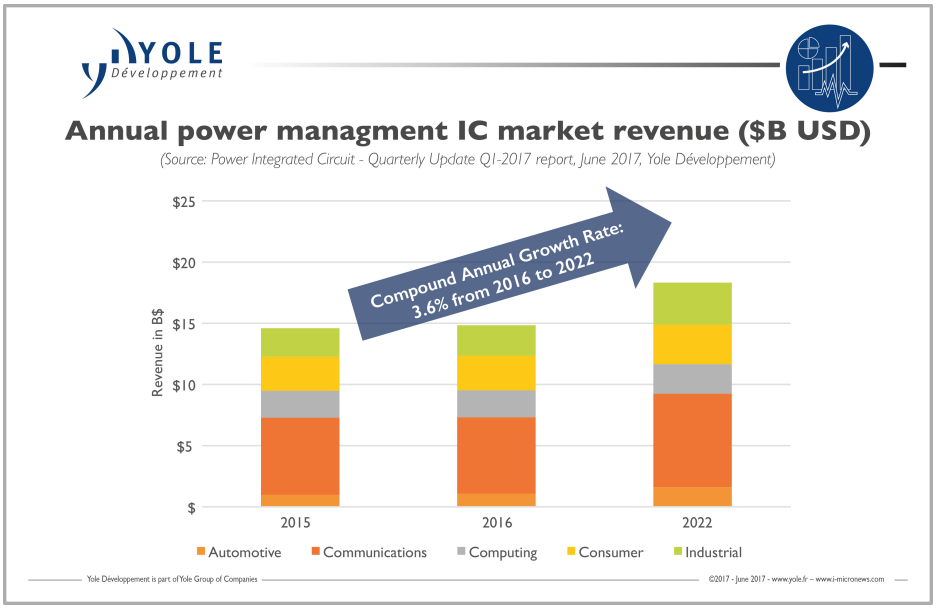


Figure 1.2: Annual power management IC market revenue Yole (2017)

1.3 Application fields for Power MOSFETs

Power MOSFETs are used in almost all modern day electronic and consumer applications to deliver power to the functional blocks. The application space of power

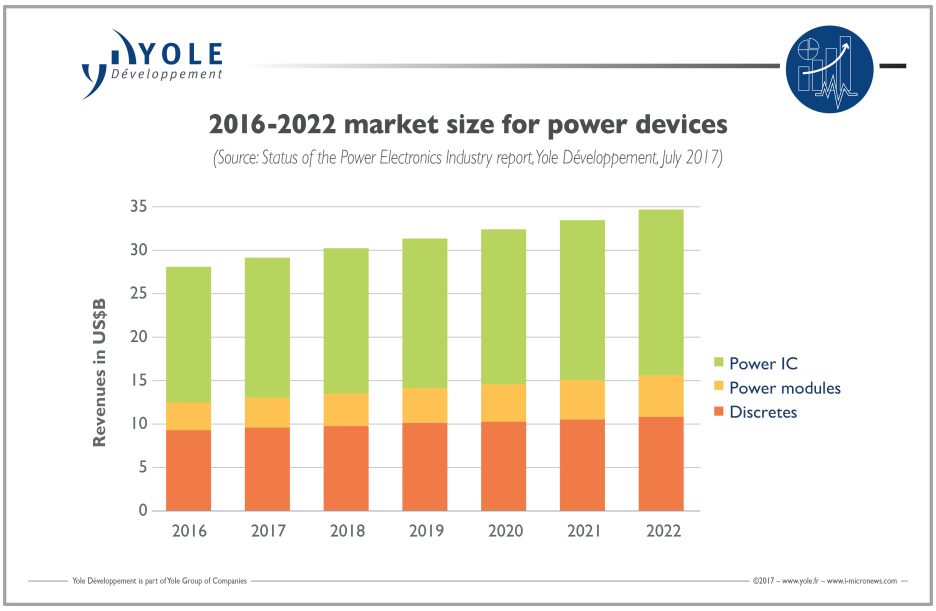


Figure 1.3: Estimation of market size for power devices Yole (2017)

semiconductors extends to a very wide range of power levels. The device blocking voltage and current handling needs of both device technologies and applications are summed up in Fig. 1.4. DC-DC converters are very much popular in portable applications for the conversion of battery power to DC output voltage. Automotive industry is another fast growing area where low voltage power MOSFETs are widely used in vehicle safety, vehicle body electronic subsytems, engine control etc.

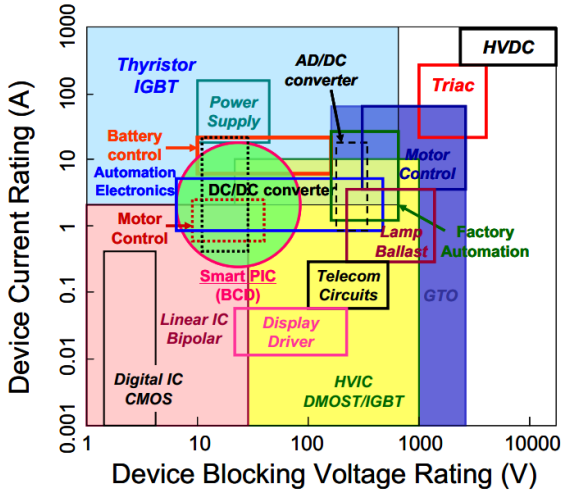


Figure 1.4: Power device technologies and applications with respect to their voltages and current ratings [Yoo (2010)]

1.4 Research focus

Since the inception of integrated circuits in 1959, silicon-based semiconductor industry has grown many fold. By about 1965, Gordon Moore observed that for silicon-based integrated circuits, the number of transistors per square centimeter doubled every 18 months. The increasing demand of RF devices suitable for high power applications such as in cellular base stations, transceivers, pulsed radar etc. has led to the design of high voltage power devices like IGBT, Laterally Diffused MOSFET (LDMOSFET), Vertically Diffused MOSFET (VDMOSFET), Superjunction MOSFET etc.

With the evolution of scaling and market demands, silicon devices have always been the choice of technology for integrated circuits on a single chip. Due to the rapid scaling of CMOS technology, integration of analog and RF components into a single chip has been in great demand Toulon *et al.* (2011). The application space of power devices includes, from smart power technologies to all kinds of portable applications (smart phones, digital cameras, MP3 players etc Fig. 1.5).

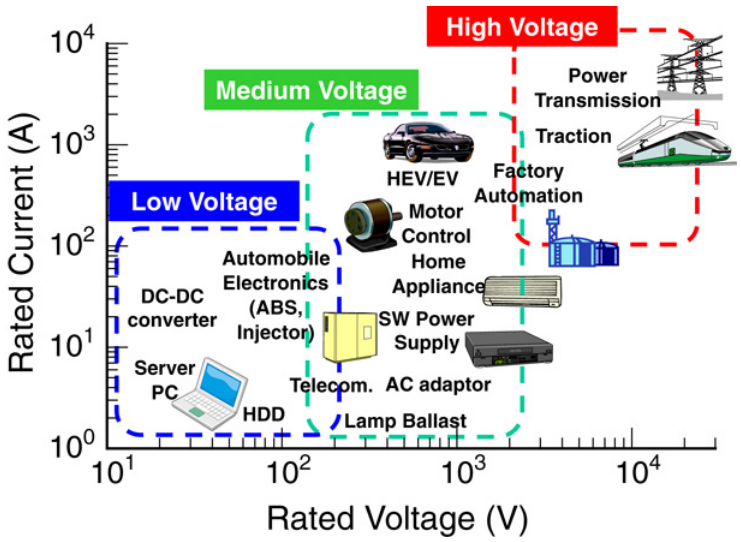


Figure 1.5: Major application areas of power devices plotted as a function of rated voltage [Kimoto (2015)].

The special feature of portability of RF wireless systems is one of the driving factors for growing market under CMOS-SoC platforms Gupta *et al.* (2015). Most of the modern SoCs come with multiple CMOS technologies embedded within the same chip Bianchi *et al.* (2009). In order to address the demands of advanced functionalities of SoC chips, interfacing various modules operating at different voltage levels is very

much essential. In the past, RF circuit modules are fabricated as separate chips having high frequency input-output voltage/current transitions. These RF modules are often interfaced with the core ICs and other components through peripheral ICs, and calls for the design of high voltage interfaces with ultra-fast connections. Therefore, I/O circuit model is one such design interface that grants flexibility of interaction between the modules. One of the efficient ways to implement these high voltage I/O circuitry is to design a power device that can support higher power delivery with higher Power Amplification Efficiency (PAE) Toulon *et al.* (2011). Such high power DeMOS based circuits can be found in power management ICs, level shifters, DC-DC converters, high voltage drivers and RF power amplifiers working up to 10-20 volts (Fig. 1.5) Yoo (2010).

The third generation "smart" cell phones combine the traditional 2G cellular phone with PDA-like features as well as digital still cameras (DSCs) and music players (MP3s). Fig. 1.6 shows a simplified block diagram of a 3G phone with its major subsystems and their respective voltage rails. A sub-module operating at a supply of 2V may access a peripheral module that operates at 12V Shrivastava *et al.* (2010*a*). Such diversity in functionality requires numerous components, most of which have different power rail voltages, with each rail having varying power demands and application-specific requirements. At the same time, consumers want smaller phones with maximum battery life and minimal battery charge time. All of these requirements have driven development of various high performance and/or highly specialized power management integrated circuits Reno (2002). Fig. 1.7 shows the strategy for power management in hand-held power devices. In general, any complex portable device such as a cell-phone requires anywhere between 5 to 7 regulators for generating different power rails. Therefore, depending on the application, the design of high voltage I/O circuitry becomes a primary part of any RF design which needs power conversions at various stages.

Breakdown voltage (V_{BD}) is an important parameter that separates power devices from the normal MOS transistor. This parameter is likely to degrade when the device undergoes multiple events such as premature avalanche, self heating, electrostatic discharge (ESD), hot carrier degradations or the device physical parametric variations. Reduction of breakdown voltages curtail the technology scaling further Shrivastava *et al.* (2010*a*), therefore an alternative design of power devices is highly essential in the integration perspective. Also, due to shrinking of feature size, hot carrier degradation

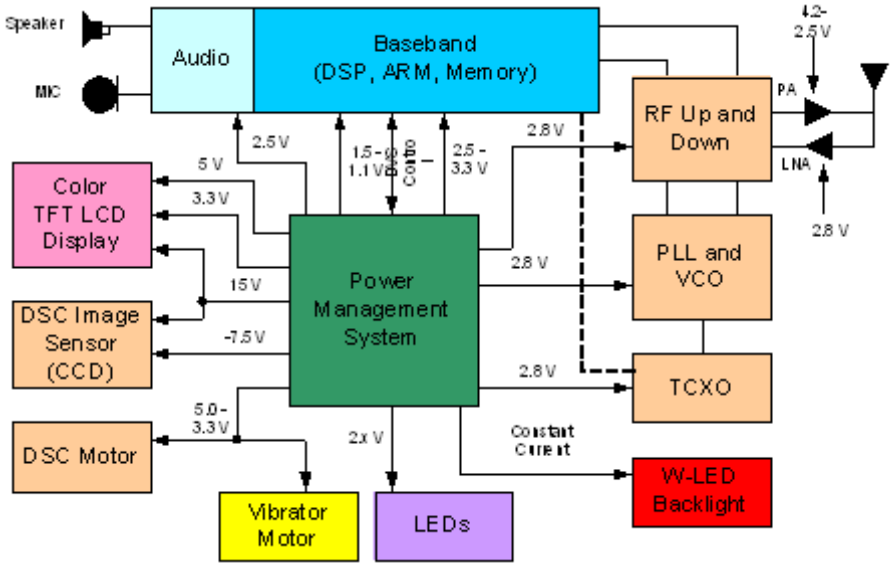


Figure 1.6: 3G Smart Phone Block Diagram [Jeff (2004)].

Qian *et al.* (2010) Belaïd and Daoud (2010) and oxide reliability pose serious problems Shrivastava *et al.* (2010*a*). Further, lower V_{BD} leads to limited usage of these devices in RF power applicationsShrivastava *et al.* (2010*a*). In short, serving to meet all the primary attributes such as higher breakdown voltage (V_{BD}) at low on-resistance (R_{ON}) and immunity to hot carrier degradation defines the basic boundary for a design of high-voltage devices. LDMOS and DeMOS are the major class of devices for high voltage I/O application space. DeMOS transistors, being an important class of power devices, are capable of sustaining high terminal breakdown voltages and can be fabricated along with conventional MOS devices with minor process cost penalty. Silicon LDMOS devices having longer channel lengths (μm) have been employed since many years for discrete RF applications, such as base-stations which operate at 28-30V and having V_{BD} upto 100V. In overcoming the bottleneck of power design challenge in technology scaling, Reduced Surface Field (RESURF) principle provides further scope for designing and integrating the power transistors.

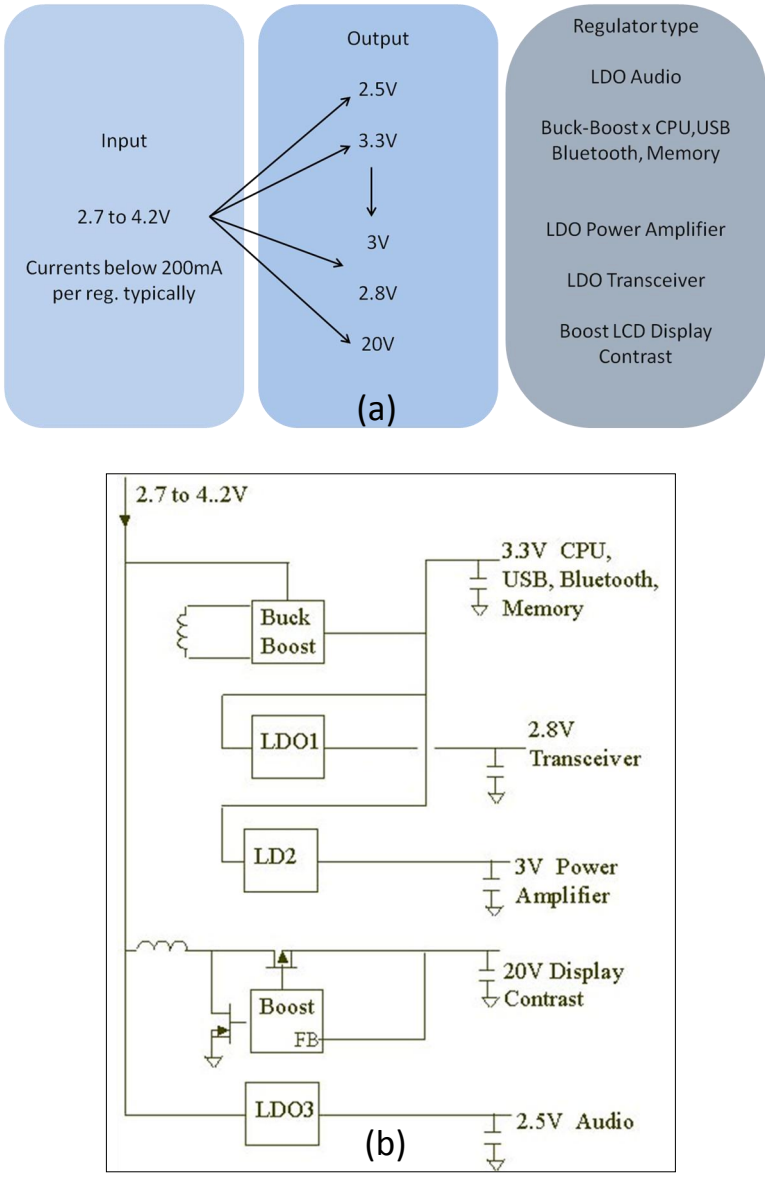


Figure 1.7: (a) Strategy for power management modules in hand-held wireless systems. (b) Power management in hand-held wireless systems [Reno (2002)]

1.5 Research Objectives

This work focuses on the design of efficient HV-DeMOS devices by optimizing device dimension for increased power handling capacity and improved breakdown voltages at submicron MOS technology (below 100nm) for single-chip RF-system-on-chip (RF-SoC) applications. The work comprehensively analyzes the high voltage device design

criteria to achieve higher V_{BD} - R_{ON} ratio and provides an over all view of figure of merits and design trade-offs. Furthermore, well constructed optimization is carried out to lay down the design guidelines for the use of power devices in RF-SoC integrated circuits. The work also explores various device structures of DeMOS for wide range of breakdown voltages. Investigations into the possibility of merging a new device like double gate structure (FinFETs) with conventional LDMOS for improved device characteristics and better channel control is also considered.

Following are the research objectives taken up in this work.

1. Improve the efficiency (V_{BD}/R_{ON} ratio and I_{ON}/I_{OFF} ratio) of existing DeMOS structures for high voltage RF SoC applications.

2. Design of Drain extended FinFETs and performance evaluation of various device parameters. Exploring the suitability of Drain extended FinFETs for high voltage applications.

1.6 Organization and Contribution of the Thesis

In this work, four different RESURF based super junction DeMOS devices, namely, double RESURF, triple RESURF and multiple RESURF (I & II) are designed, simulated and their performance is compared with conventional RESURF devices. The RESURF principle is later extended to DeFinFETs and their performance metrics are compared.

It is shown that, incorporating p-implants in the drift region and a careful tuning of the implant length, thickness, position and doping concentration results in,

- Higher breakdown voltage, V_{BD} of 23V for double RESURF device, V_{BD} of 21V for triple RESURF device, and a V_{BD} of 19V for multiple RESURF devices. This is an improvement of 50%-80% over the conventional device with an R_{ON} of $\approx 2.5k\Omega$.

- The simulation studies using Spherical Harmonic Expansion shows that the devices have improved immunity towards gate oxide breakdown, better hot carrier and ESD reliability and provide a good boundary for safe operating area.

Finally, high voltage DeFinFET structures are proposed and simulated for submicron high voltage applications. The simulated structures show,

- Improved Breakdown voltage of V_{BD}=8-9V compared to the conventional DeFinFET devices (V_{BD}=3V).
- Higher I_{ON}/I_{OFF} ratio upto 10^8, mitigating the quasi-saturation effect.

The thesis is organized as follows. Chapter 2 presents the basic theory of conventional drain extended MOS devices. Chapter 3 to chapter 5 presents the performance trade-offs with respect to device parameters of double RESURF, triple RESURF and multiple RESURF devices respectively. Chapter 6 presents the detailed performance comparison (viz., figure of merit, long term reliability, electro static discharge behavior etc.) of these structures with the conventional device. Chapter 7 explores the suitability of DeFinFETs for power applications. Chapter 8 concludes the thesis by listing the contributions and with a description of pros and cons of the methods proposed, followed by possible future extensions.

Chapter 2

Theory of Power MOSFETs

2.1 Conventional MOSFETs

Metal-oxide-semiconductor field effect transistor (MOSFET) forms the basis of a vast majority of integrated circuits and Complementary MOS (CMOS) is a dominant technology having two important characteristics, namely high noise immunity and low static power consumption. In circuits built using this technology, significant power is drawn only when the transistors are switched between on- and off-states. Accordingly, CMOS based circuitry dissipates less power and allows a denser integration of devices for a given functionality.

However, the conventional MOSFETs cannot be used for high voltage applications due to their low breakdown voltage characteristics. On applying the gate bias, most of the voltage drops across the gate oxide region. This results in large electric field in the oxide region and a comparatively low voltage drop in the silicon substrate below the gate. Secondly, in order to achieve a low channel resistance, shorter channel length and thinner gate oxide is essential. Since both gate length and the gate oxide thickness are related to breakdown voltage of the MOS device. Thus, Gate-oxide breakdown, avalanche breakdown, hot-carrier effect etc. prohibit the use of conventional MOSFETs in high power/high voltage applications and the conventional MOS structure is out of choice as a power device.

2.2 HVMOS structure

High Voltage MOS (HVMOS) structure is similar to that of a conventional MOS except it has an additional feature in the device structure known as extended n-region (p-region for PMOS), called the drift region, between the channel and the drain region. Charge carriers flow through the drift region between the source and drain. The current in the drift region can flow in either vertical direction or horizontal direction. Based on the direction of flow of current in drift region, HVMOS can be classified as Vertical MOS (vertical direction) or Lateral MOS (horizontal direction) (Fig. 2.1). Vertical MOS offers higher breakdown voltages and transconductance. However, HVMOS requires complex fabrication steps and hence finds fewer applications.

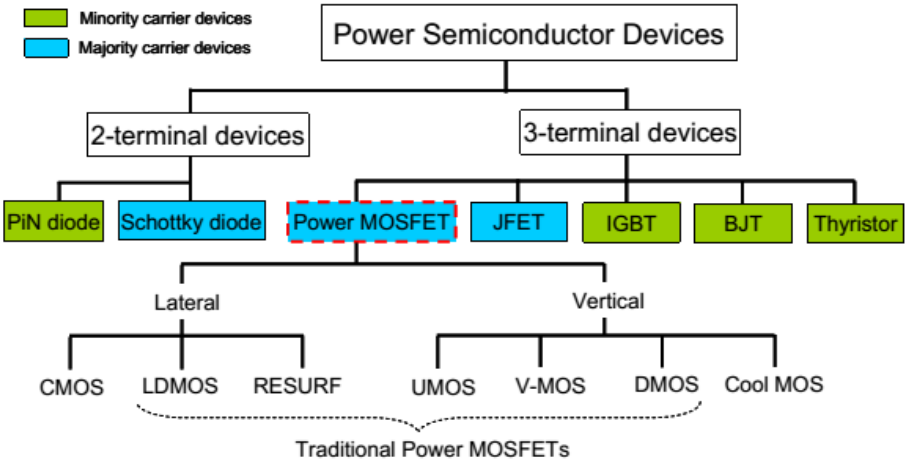


Figure 2.1: Classification of power semiconductors devices

2.2.1 LDMOS/DeMOS

Laterally diffused MOS (LDMOS) or Drain extended MOS (DeMOS) transistors are an important class of power devices. HV LDMOS are widely used in various integrated power circuits for smart power applications. It does not require complex processing steps unlike in Vertical MOS. The critical parameters that decide the power handling capability and performance of power devices are breakdown voltage (V_{BD}) and on-resistance (R_{ON}). Breakdown voltage for LDMOS is an important parameter that distinguishes a power device from other MOS devices. This parameter is likely to

degrade over multiple issues.

The basic LDMOS structure is shown in Fig. 2.2. Drain current flow in n-LDMOS is induced by applying positive bias to gate electrode. When the transistor is turned on, the drift region simply acts as a voltage variable resistor and creates a voltage drop such that potential under drain is much less than the applied DC voltage thereby ensuring that the hot carrier injection is limited Baliga (2010). If a high voltage is applied at the drain, there will be a high voltage drop at the drain region itself Baliga (2005). Ideally, electric field is expected to be uniformly distributed throughout the drift region. For smaller values of V_{DS}, potential drop along drift region is smaller and is linear indicating a resistive behavior. However, at higher values of V_{DS}, the potential drop along the drift region is highly non linear with more potential drop toward the gate end of the drift region. The pinch off of Junction Field Effect Transistor (JFET) can be seen to occur near gate edge of drift region. Baliga (2010).

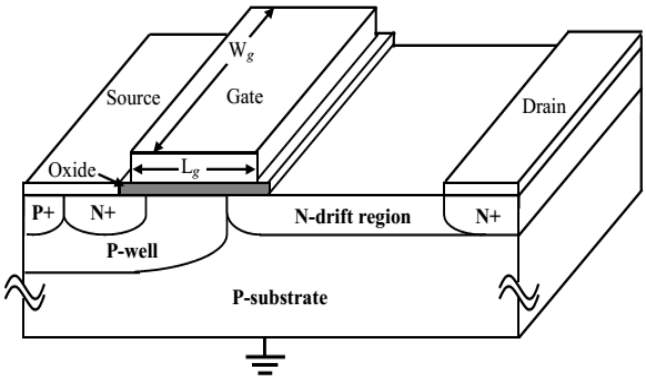


Figure 2.2: Schematic of conventional laterally diffused MOS device Yoo (2010)

The additional voltage drop that need to be supported near the gate edge, is achieved by receding the drain region away from the gate edge by the introduction of the drift region between the gate and the drain.

On-resistance of LDMOS consists of active channel resistance in series with the resistance of accumulation region at the surface, resistance in the drift region and also the resistance of bulk/p-type substrate. Resistance can be reduced by increasing the charge (doping). At lower gate voltages, the conductivity is poor since the device is in weak inversion mode and channel has just formed between source and drain regions. The channel resistance is considered to be the dominant resistance at this gate voltage. At higher gate voltages, carriers conduct freely through the channel, indicating low

resistance in channel. But accumulation layer exits at higher gate voltages and the bulk region resistance R_{bulk} become substantial in this situation. So, the total on-resistance is given by, (Jun-Ning *et al.* (2006))

$$R_{ON} = R_{ON-channel} + R_{accumulation} + R_{spreading} + R_{bulk} + R_{distribution} \tag{2.1}$$

where $R_{ON-channel}$ is the channel resistance, $R_{accumulation}$ is a resistance of the accumulation layer under the field plate, $R_{spreading}$ is spreading resistance caused due to current scattering, R_{bulk} is a bulk resistance in drift region, and $R_{distribution}$ is a distribution resistance at drain. When the current carriers arrive at the drain terminal, distribution resistance $R_{distribution}$ at drain causes the electric field to rise making the device vulnerable to breakdown.

The ideal specific on-resistance of drift region is given by, Baliga (2005)

$$R_{ON,sp} = \frac{W_D}{q\mu_n N_D} = 5.93 \times 10^{-9} (V_{BD})^{2.5} \tag{2.2}$$

where N_D is the doping concentration of the N-drift region for a desired breakdown voltage V_{BD} and W_D is the thickness of the N-drift region. The epi-depth/doping as well as n-drifts depth/doping/extension must be optimized such that peak electric field across this depletion region doesnt exceed critical breakdown levels during high voltage swing.

2.3 Principle of RESURF

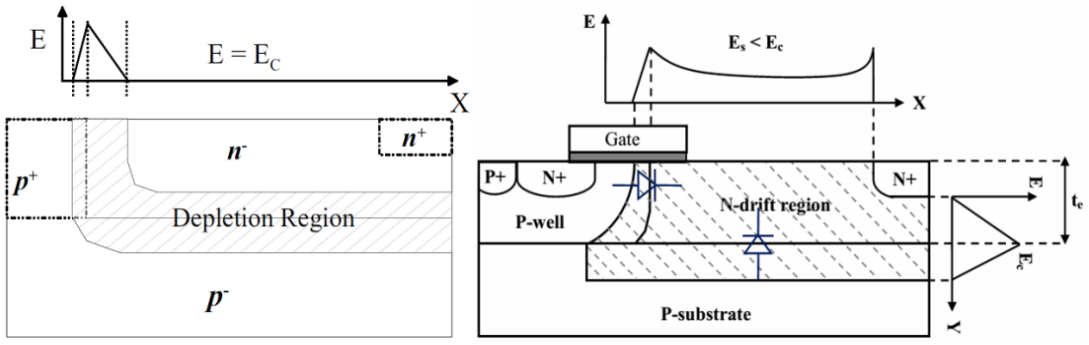


Figure 2.3: Schematics explaining principle of RESURF

High voltage levels are sustained in LDMOS/DeMOS devices when drift region is incorporated between the gate and the drain. But, a simple extension of drift region is not sufficient to improve the breakdown characteristics Perugupalli *et al.* (1998). To sustain high voltages, a thin epitaxial n-type layer is to be employed in such a way that the electric field at the surface is suppressed Asif (2011). Hence the name Reduced Surface Field or RESURF Drain Extended MOS. Under normal conditions, breakdown occurs at p+/n- (p-well-n-drift) lateral junction. The depletion cannot penetrate in the p+ region, which results in early junction breakdown due to a high electric field for relatively low voltages/low charge density conditions. The RESURF technique results in expansion of the depletion region for high drain bias and keep the peak electric field below the critical field that causes impact ionization, without compromising the low value of drain resistance, R_{DSON}.

Using RESURF technique, the doping density of drift region and its thickness is adjusted so that depletion region of the vertical diode (p-substrate-n-well junction diode) reaches the surface before the breakdown of the lateral diode (p-well-n-well junction diode) occurs Baliga (2010). Hence, the RESURF condition is decided by, Ludikhuize (2000),

1. Length, depth and doping of the drift region
2. Doping of p-substrate and p-well

The doping concentration and thickness of drift region for obtaining the desired breakdown voltage is given by, Baliga (2005)

$$N_D = \left[\frac{5.34 \times 10^{13}}{V_{BD}}\right]^{4/3} \tag{2.3}$$

$$W_D = 2.67 \times 10^{10} {N_D}^{-7/8} \tag{2.4}$$

For conventional LDMOS fabricated on a thick epitaxial layer, the breakdown voltage is given by,

$$V_{BD} = \phi_{cy} + \frac{t_{ox}}{\epsilon_o \epsilon_{ox}} (2\epsilon_o \epsilon_{si} q N_D \phi_{cy})^{1/2} \tag{2.5}$$

where, $\phi_{cy} = \phi_{pp}\{[(2+\gamma)\gamma]^{1/2} - \gamma\}$ and $\gamma = (\epsilon_{Si} t_{ox})/(W_{pp}\epsilon_{ox})$.
Here ϕ_{pp} is the surface potential at which breakdown occurs in a plane structure and W_{pp} is the depletion depth in the drift region at an applied surface potential ϕ_{pp} Parpia and Salama (1990).

RESURF principle is governed by evenly distributed electric field and depletion width in the device. The more uniformly distributed electric field results in a better breakdown behavior. So, in order to have a better field distribution, effective utilization of silicon in depleting the n-well drift area is very essential Fu *et al.* (2014).

2.4 Breakdown Mechanisms

Breakdown occurs due to many factors such as variation in thickness of various physical parameters involved or doping profiles. Breakdown characteristics is determined by the utilization of silicon area beside the channel effectively for depletion. In power semiconductor industry, the basic thumb rule is to design 20-30% of safety margin in breakdown voltage from the aspect of fabrication tolerance and degradation in long term. Some of the breakdown mechanisms are explained below Asif (2011).

1) Avalanche breakdown: In HVMOS structure, the reverse-biased depletion regions sustain high voltages. Under the high electric field conditions, any electron that enters the depletion region is swept away. The carriers gain sufficient energy and generates additional electron-hole pairs due to interaction with lattice atoms in their path. Generated E-H pairs, on moving towards depletion boundaries, continue to produce additional E-H pairs and thus, a large amount of carriers are generated causing breakdown.

2) Surface breakdown: Breakdown also depends upon the type of junction and junction termination at the surface. Dopants may diffuse laterally or vertically after implantation. The junctions can be abrupt or linearly graded. The junction edges take the form of cylindrical or spherical contour. The electric field lines get crowded at the edges in order to maintain charge balance. This crowding of field lines leads to a high rate of impact ionization and an early junction breakdown at the edges .

3) Snapback breakdown: It occurs when a high-voltage across the drain-substrate junction forces a higher number of E-H pairs to cause impact ionization and the holes to start moving towards the substrate. The intrinsic substrate resistance will increase the substrate potential. As the substrate potential reaches higher value, source-substrate junction gets forward biased and source starts injecting electrons to the drain terminal through substrate. This forms a parasitic Bipolar Junction Transistor (BJT). When electrons reach drain-substrate junction, E-H pairs get generated again and this increases forward biasing and hence positive feedback loop leads to

junction breakdown Qian *et al.* (2010).

4) Gate oxide breakdown: This is the common breakdown that occurs when there is a conductive path which provides low resistance path or a short between gate-metal-poly and source-drain-substrate region through a very thin gate oxide (in nm). It is due to hot carrier injection, the dominant effect of charge trapping mechanism that occurs due to driven acceleration of charge carriers by high internal electric fields due to V_{DS} and V_{GS} (both horizontal & vertical electric fields).

2.5 LDMOS Structures from literature

Silicon LDMOS transistors having channel lengths of 3-4μm have been employed since many years, as a choice for high-power power amplifiers due to excellent cost and performance ratios in base station applications, which require a high blocking voltage upto 100V for a given supply voltage of 28-30V. Some of the prominent LDMOS structures having moderately large channel lengths are given below.

2.5.1 The Basic structure

The structure has n-epi layer acting as a drain-drift region which supports most of V_{BD}. Peak field occurs right below the gate edge corresponding to a peak impact ionization rate. This reduces V_{BD} of the device He and Zhang (2001).

2.5.2 With field plate

The structure has metal layer connecting the source and body, is extended beyond the edges of the gate to relax the electric field in silicon underneath gate region. The field plate successfully extends the equipotential lines and the peak electric field get shifted from gate edge to the oxide region. Since oxide has higher critical electric field ($> 10X$) than silicon, it is immune to provoke avalanche breakdown. So impact ionization takes place at bulk rather than surface. Field plate increases the V_{BD} as V_{BD} depends on length of the field plate. Increasing the field plate length increases V_{BD}. Also V_{BD} reduces drastically if the plate edge and drift/drain junctions are close to each other Hossain *et al.* (2004).

2.5.3 With STI

The device structure has Shallow Trench Isolation (STI) that is located in drain drift region but also has a certain overlap with poly-gate. Using STI in the drift region, enables a wider spread of equi-potential lines. So uniform electric field is spread between junction and bulk. The peak electric field underneath the gates right edge is now held by the STI oxide material. So it does not support the onset of impact ionization Haynie *et al.* (2010). Structures having both field plate and STI support diversion of the peak electric field towards oxide.

2.5.4 RESURF structure with p-epi layer

Here, the depletion of n-well is caused by horizontal and vertical depletion regions, due to p-body and p-epi. In this structure, the p-body is connected to p-epi, where p-epi is placed under n-well. This gains low potential from either a grounded substrate or p-body. P-epi depletes the n-well in larger volume. Hence, V_{BD} is comparatively higher than the earlier structures. In these structures, 2D depletion effect is seen which makes the electric field uniformly distributed. Hence most of the n-well region is depleted Ludikhuize (2000).

2.5.5 RESURF Dielectric region inserted (REDI)

The structure is an improved version of STI based structure (Fig. 2.4(a)). The inserted oxide can reduce electric field near drain and p_+ doped region, which reduces surface electric field near drain side and increases the V_{BD}. Hence, the inserted oxide layer acts as electric field line absorber in the drift region and holds most of drain potential drop. This structure has a better reliability metric compared to other structures Xiao *et al.* (2009).

2.5.6 Charge compensation using P-IL

In Han *et al.* (2013), an idea of P-Implant Layer (P-IL) methodology in 0.18μm is proposed to improve V_{BD} by compensating charge balance (Fig. 2.4(b)). After high voltage p-well and n-drift well implantation is carried out, P-IL is implemented using p-drift implantation technique (same as in p-type LDMOS). Apart from width and length of P-IL, the placement of P-IL also play a major role. Accordingly, P-IL is

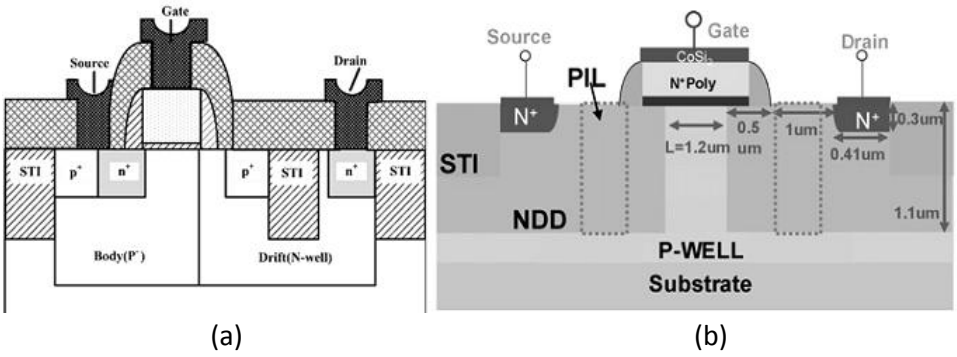


Figure 2.4: (a)RESURF Dielectric region inserted structure Xiao *et al.* (2009) (b) P-implanted structure Han *et al.* (2013)

placed at three different positions, out of which, P-IL placement in n-drift region between the channel and drain is found to give better distribution of electric field and performance than placing near to drain or channel region. This also gives an improvement in V_{BD} Han *et al.* (2013).

2.5.7 Structures with Double/Triple/RESURFs

Incorporating an additional p-region instead of STI yields better characteristics. Therefore, n-well is depleted by three regions: p-epi, p-body and additional p-RESURF Fu *et al.* (2014). Floating island depletes the n-well within its surrounding. Triple-RESURF structure, yields low on-resistance Hu *et al.* (2012). Triple-RESURF has two lower electric field peaks which results in reduced bulk electric field because of uniform field distribution Hu *et al.* (2012).

2.5.8 SOI LDMOS structures

Presently, the SOI structure has wide applications such as lighting electronics and motor control due to its advantages over conventional LDMOS on bulk silicon. It is well known that application of RESURF principle on bulk silicon makes it possible to achieve good breakdown boundaries. But according to recent research from 2007, SOI RESURF effect has been found effective and high breakdown voltages can be achieved if the SOI layer is a thin film structure Bawedin *et al.* (2004), preferably fully depleted SOI. SOI device is doped with a linear doping profile so that electric field peak does not vary linearly. In Wang *et al.* (2010), it is shown that with uniform profile and with

a doping concentration of $1.5 \times 10^{16}/cm^3$, the V_{BD} is just 153V whereas with linearly varying profile, V_{BD} is found to be 655V for $5 \times 10^{12}/cm^3$. The reason for the high V_{BD} is that the surface lateral electric field is almost uniform throughout the channel and drift region.

These are some of the structures from literature having large channel lengths (in μm) that have been used in discrete power applications. The power modules operate at a voltage ranging from 100V to 700V. The application space includes power conversions (AC-DC conversions), power delivery (HVDC, electric trains), RF transmission (GSM base station), automotive and locomotive control units etc.

But RF-system-on-a-chip (RF-SoC) implies that RF/analog/digital circuits are all integrated with memory blocks and microprocessors/DSP as a complex single-chip digital communication system. The primary advantage of a single-chip RF-SoC is that the component will be less susceptible to external noise pickup, have a smaller area, simple assembly, and is likely to achieve lower system cost in the long run. Conventional DeMOS devices from recent literature Gupta *et al.* (2015), Shrivastava *et al.* (2010*a*) with a channel length of 420 nm reported a breakdown voltage, V_{BD}, in the range of 18-23V, on-resistance, R_{ON}, of $5.5 - 6\ k\Omega$ and an f_{max} of 50 GH_z.

Power Amplifiers (PAs) are one of the most difficult RF components to be integrated on-chip for RF-SoC products because of their high breakdown voltage requirements. Device technology based on III-V group elements may be preferred for PA design since breakdown voltages tend to be higher in GaAs-based devices featuring a larger band gap. However, when it comes to integration on a single chip, silicon devices dominate due to the ease of integration, its lower fabrication cost and scalable properties. Hence its application space includes high performance core, power management blocks, low standby power on circuitry, high voltage I/O etc. This work concentrates on designing such power devices in 65 nm regime with a target of superior V_{BD} and R_{ON} metrics compared to Gupta *et al.* (2015), Shrivastava *et al.* (2010*a*) for applications in RF-SoC platforms.

2.6 TCAD Simulation setup

The device structures in this work are designed and simulated using well-established Sentaurus Technology Computer-Aided Design (TCAD) tool. The process flow here is same as that of the conventional CMOS transistor except for two modifications:

Firstly, the drain has to be implanted in the n-well (drift) region and source in the p-well region. Secondly it requires one additional mask for the RESURF implants. But it is worth mentioning that advanced processes do have both n-well and p-well implants along with RESURF implant masks in sub-100nm node CMOS technologies Shrivastava *et al.* (2010*a*). The p-well and n-well has retrograde doping profile which helps in improving the breakdown voltage of the device. The device dimensions used in this work are given in the Table 2.1. Single halo implant is used for improving the subthreshold behavior. Breakdown simulations of the device are carried out using well calibrated New University of Bologna (UniBo2) impact ionization model. Carrier-carrier scattering is included in the mobility models. Shockley-Read-Hall (SRH) and Auger recombination models are used for accounting excessive carrier recombination.

Table 2.1: Dimensional specification of Conventional DeMOS device

Dimension parameter	**Values nm**
t_{OX}	5nm
L_G	250nm
L_{Drift}	700nm
L_{OV}	150nm
X_{Well}	500nm

2.7 Conventional Drain Extended MOS (DeMOS)

Fig. 2.5 shows the conventional RESURF DeMOS structure. The n-well depth of the DeMOS is kept higher than the conventional LDMOS structure. In order to build a better field distribution, effective utilization of silicon in depleting the n-well drift area is very essential Fu *et al.* (2014). On applying a high voltage at the drain terminal with V_{GS}=0V, it is evident that the total voltage drop is equivalent to the drops at the junctions of drift-drain and drift-p-well Parpia and Salama (1990). Subjecting to a lower concentration of doping in the drift region, the electric field predominates at the drift-drain junction as explained in Shrivastava and Gossner (2012). Denoting N_{drift} as the doping concentration of drift region, the field gradient along Y-direction is given by,

$$\frac{dE}{dy} = \frac{1}{\epsilon_{si}} q[N_{drift} - n(e)] \tag{2.6}$$

This implies that at higher current injections, the carrier concentration $n(e)$ exceeds the background doping and electric field peaks at the drift-drain junction which is well known as Kirk effect. Fig. 2.6 exhibits the conventional device under Kirk effect. Also, it is observed that if the doping concentration of substrate is higher than that of the n-well, the unintended high field confines at the drain region He and Zhang (2001). Now the possible ways to improve breakdown behavior in a conventional DeMOS can be explained as follows.

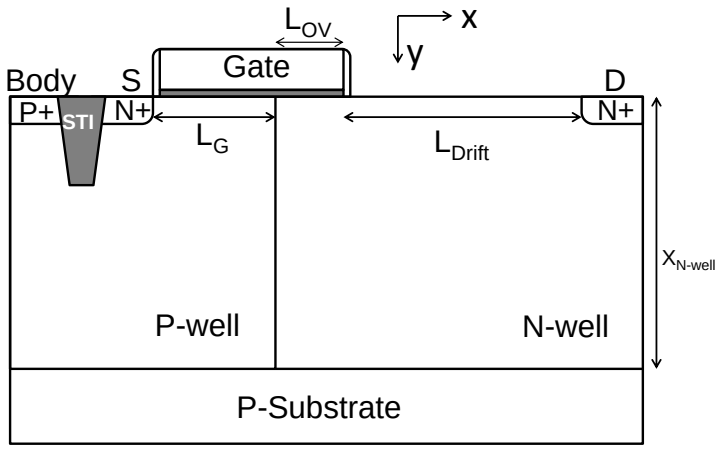


Figure 2.5: Schematic of Conventional RESURF DeMOS device used in our simulation

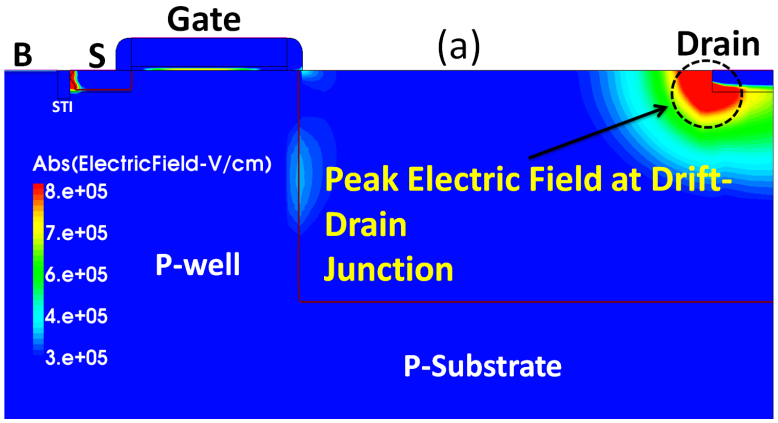


Figure 2.6: Electric Field distribution contour for conventional RESURF structure exhibiting KIRK effect.

1) Increasing the doping concentration of the drift region: This leads to a changed potential distribution and redistributes the field at the drift-p-well junction and resulting in a reduced field at the drift-drain junction He and Zhang (2001) and eliminating the Kirk effect. Thus drift-drain early junction breakdown is prevented.

2) Increasing n-well depth (keeping the n-well region with moderate doping): This makes the electric field distribution more uniform and increases V_{BD}. (Fig. 2.7).

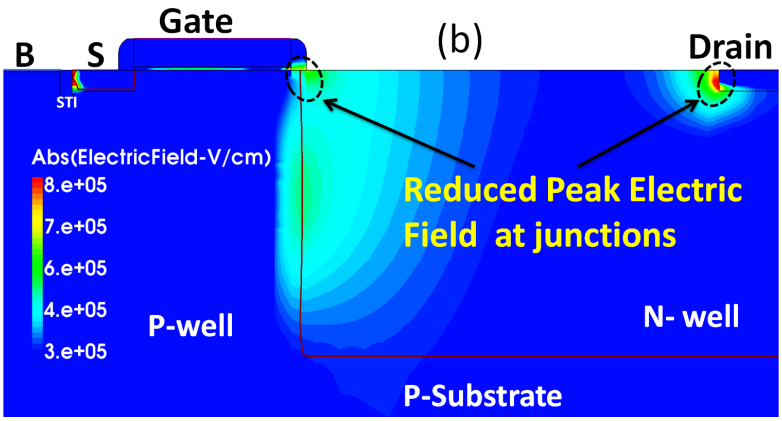


Figure 2.7: Electric Field distribution contour for conventional RESURF structure on increasing the n-well depth.

3) Increasing the gate overlap region length L_{OV}: By increasing the gate overlap region, the peak electric field is now observed in the drift region underneath the edge of the overlap region (Fig. 2.8).

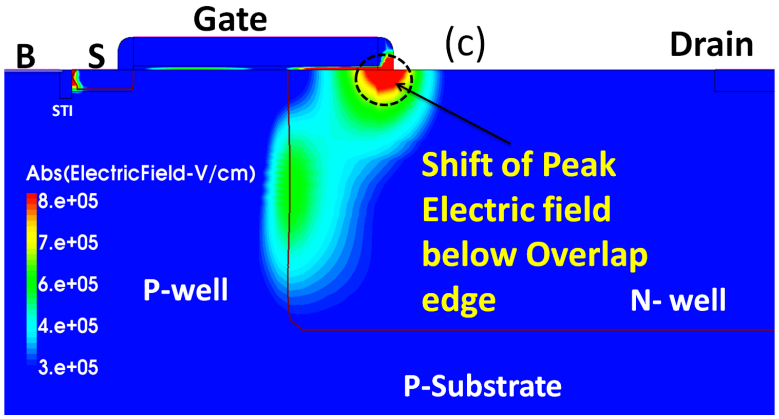


Figure 2.8: Electric Field distribution contour for conventional RESURF structure for increased gate overlap L_{OV}

But increasing the gate overlap region length degrades the R_{ON} linearly Shrivastava *et al.* (2010*a*). However, Gupta *et al.* (2015) mentions that although the R_{ON} improves by changing the lateral dimensions such as gate-overlap L_{OV} and drain diffusion length, the field profile remains almost same, resulting in an unchanged V_{BD} behavior beyond a particular L_{OV}. This is because, the Y-component of the electric field $E_y(x, 0)$ at

the gate-overlap edge, given by,

$$E_y(x,0) = -\frac{\epsilon_{ox}}{\epsilon_{si}}\frac{\phi_f(x)}{t_{ox}} \tag{2.7}$$

is of the order of 10^6V/cm. These field lines terminate into gate oxide because the critical electric field for SiO_2 is much higher than that of the silicon.

4) Apart from the above mentioned key points, it is found that the breakdown behavior can also be improved at the cost of higher substrate depth keeping all the other parameters unchanged. The device breakdown voltage improves drastically as the field lines terminate at the substrate-n-well junction vertically.

With the above modifications, it is reported in Shrivastava *et al.* (2010*a*) that, inspite of achieving good breakdown characteristics, R_{ON} continues to remain high and does not result in a good design. Thus, it is difficult to maximize the V_{BD}/R_{ON} ratio merely by following the above mentioned modifications. Hence, there is a need to look at the device geometry for enhancing the RESURF actions in order to meet the actual design goals.

Chapter 3

Double RESURF (Single SJ, $X_{imp} = 0$) DeMOS Device

The low R_{ON} and high V_{BD} in conventional DeMOS devices, make them suitable for use in high voltage applications. Although worthy, these devices suffer from accurate charge control in the drift region and are very sensitive to charge balance conditions. Charge imbalance conditions may lead to lower V_{BD} limiting on the device performance, Imam *et al.* (2003).

Fig. 3.1 shows the schematic of a 2D Superjunction (SJ) structure. It is shown in Disney *et al.* (2001) that the breakdown behavior is improved by enhancing the RESURF actions in superjunction devices. This is true if the entire n-well region is depleted vertically and the total charge density is doubled compared to that of the conventional device Imam *et al.* (2003). Therefore, an additional p-type implant is incorporated in the extended drift region as shown in Fig. 3.1. Let L_{imp} be the length of the p-implant, X_{imp} be the depth of p-implant from the surface ($X_{imp} = 0$ for this device) and t_{imp} be the thickness of the p-implant.

By implanting such a p-type implant, electric field at the surface is reduced and the magnitude of electric field peaks 2x across the n-well depth Hossain *et al.* (2004). The resistance in the drift region is given by

$$R_{drift} = \frac{L_{drift}}{Q_{drift} W q \mu} \tag{3.1}$$

where L_{drift}, W, q and μ have usual meaning, and the integrated charge density, Q_{drift}, of n-well drift region for double RESURF DeMOS as reported in Imam *et al.*

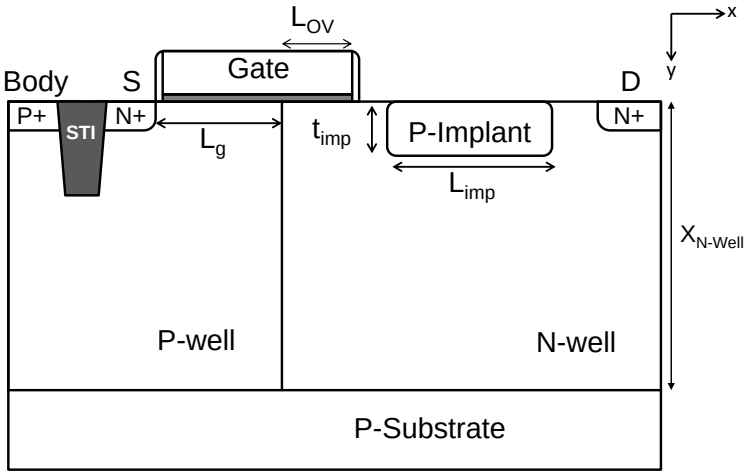


Figure 3.1: Schematic of double RESURF (Single Superjunction with $X_{imp} = 0$) DeMOS device

(2003) is given by,

$$Q_{drift} \leq 2 \times 10^{12} \left[\sqrt{\frac{N_{nwell}}{N_{imp} + N_{nwell}}} + \sqrt{\frac{N_{sub}.N_{nwell}}{N_{imp}.(N_{sub} + N_{nwell})}} \right] \tag{3.2}$$

where N_{nwell} is the doping concentration of n-well, N_{sub} is the doping concentration of p-substrate and N_{imp} is the doping concentration of p-implant. Hence,

$$Q_{drift} \leq Q_{imp} + Q_{nwell} \sqrt{\frac{N_{nwell}}{N_{imp}}} \tag{3.3}$$

in which $Q_{imp} = N_{imp} \times t_{imp}$ defines the integrated charge density of p-implant.

Hence from eq.(3.1) it can be seen that the resistance of drift region ($R_{ON} = \Sigma(R_{channel}, R_{drift})$) decreases with the increase in the total intergrated charge density. Fig. 3.1 shows the schematic of double RESURF device used in our simulation. The additional p-type layer is implanted at the top surface and is kept floating. In order to attain higher depletion width in the n-well region, the p-implant doping concentration is kept higher than that of n-well doping. Now the p-n junction created due to p-implant has to relax the field component E_y (x,0) such that field lines are re-directed towards the junction vertically. Thus, maximum field lines sink at this junction. The peak electric field shared between the gate overlap edge and p-well drift junction region is now re-distributed to an additional depletion space created by the p-implant. This results in a uniformity of the field distribution leading to significant improvement in

breakdown charateristics.

The additional p-implant layer needs a tight charge control to maintain appropriate charge balance conditions. This adds more complexity to charge control requirements which makes the implementation of double RESURF devices with controllable V_{BD} difficult. Since the use of double RESURF technology is highly dependent on charge balance sensitivity, careful strategy in optimizing the device physical parameters is an important requirement of such technology.

3.1 Parameter variations and guidelines

The double RESURF device performance greatly depends on 1) p-implant parameters 2) n-well depth and 3) substrate thickness.

3.1.1 P-implant Variation

The design parameters of p-implant namely implant length, implant doping and implant thickness are discussed in this section.

a) P-implant Length: Introducing the p-implant in the drift region always improves the breakdown characteristics because the major portion of the n-well area is now depleted. Also the induced positive charge leads to optimal charge balance. This improves the resistivity of the drift region. But, as the p-implant length is elongated towards the drain region, consuming effective conductive area in the n-well region, the R_{ON} starts rising gradually. Increase in the length of the p-implant increases the breakdown voltage (Fig. 3.2) until it reaches the drain region.

However, once the p-implant adjoins the drain region, there is a large concentration gradient between drain and p-implant. This provides an additional junction with a large electric field that degrades V_{BD}. Now the injected charge leads to changed potential distribution which increases ionization rate dramatically. Therefore, the length of the p-implant is limited to the longitudinal region between gate overlap (L_{OV}) and drain region. This decides the maximum length of the p-implant.

b) P-implant doping: This parameter is interdependent on the length as well as the depth of p-implant. When the p-implantation is done with a Gaussian profile, for a given n-well doping condition, R_{ON} increases gradually with the increase of p-implant doping. This is due to the reduced conductivity of the counter-doped n-well

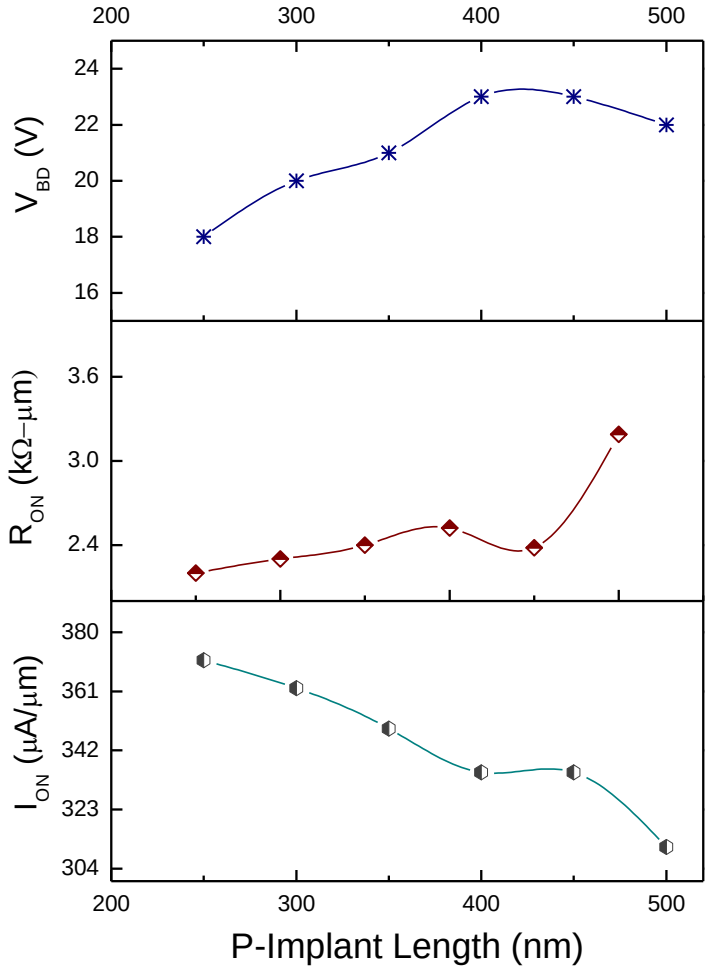


Figure 3.2: Varitation of V_{BD}, R_{ON} and I_{ON} with implant length. V_{BD} simulations taken at V_{GS}=0V and V_{DS}=6V. I_{ON}-R_{ON} taken at V_{GS}=1.8V and V_{DS}=6V

drift region. Increase in doping increases V_{BD}, while R_{ON} starts deteriorating due to disturbed carrier conduction path. A small amount of minority charge density always exists in the depletion region. The drift velocity of these carriers is limited by scattering. As a result the time between scattering decreases with the impurity ionized charges and the scattering events occur more often. This obstructs the continuous sweep of charge carriers towards the drain region resulting in degraded mobility as seen from the mobility equation,

$$\mu = \frac{q\tau_c}{2m} \tag{3.4}$$

where q is the electronic charge, τ_c is the scattering time interval, and m is the

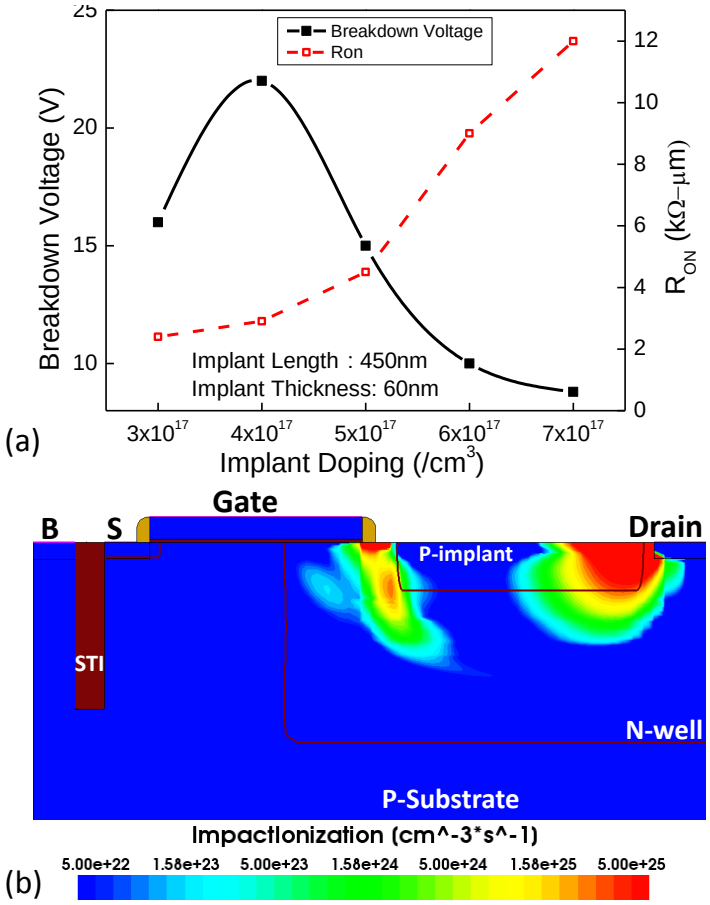


Figure 3.3: (a) Plot of V_{BD} - R_{ON} as a function of implant doping. (b) Contour of impact ionization for increased implant doping. The V_{BD} is simulated for V_{DS}=6V and V_{GS}=0V and R_{ON} for V_{DS}=6V and V_{GS}=1.8V

effective electron mass. R_{ON} being a function of mobility ($\mu \propto \frac{1}{R_{ON}}$), R_{ON} degrades significantly as the doping concentration increases beyond n-well doping levels. Fig. 3.3(a) shows that V_{BD} falls if the doping concentration exceeds $4.5\times10^{17}/cm^3$ for the given n-well doping of $3\times10^{17}/cm^3$. Also a higher p-implant doping increases the peak electric field leading to impact ionization (Fig. 3.3(b)).

c) P-implant thickness: The implant thickness is the thickness of the p-layer and depends on how deeper the p-layer diffuses into the n-well region from the surface. The minimum depth of the implant is that for which the depletion occurs vertically in the p-implanted region. So according to the equation $X_{nwell}N_{nwell} = t_{imp}N_{imp}$, in order to meet the proper depletion and the charge balance conditions, the minimum

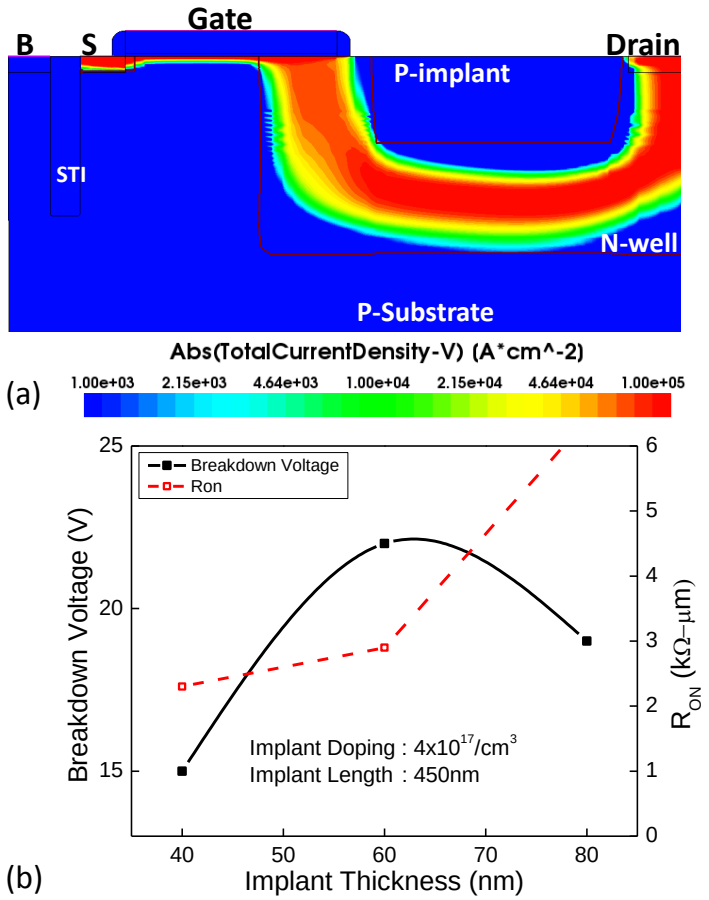


Figure 3.4: (a) Contour of absolute current density simultated for V_{GS}=1.8V and V_{DS}=6V. (b) V_{BD}-R_{ON} as a function of implant thickness.

depth X_{imp} is given by

$$t_{imp} = \sqrt{\frac{2\epsilon_s V_{Bi}}{qN_{imp}}} \tag{3.5}$$

where N_{imp} is the concentration of implant doping. Implant thickness is the major parameter that creates an optimum design window for good V_{BD} - R_{ON} trade-off. Although the breakdown behavior is improved for a higher thickness of p-region, there are several other factors that result in performance degradation. Following are the adverse effects of changing the implant thickness. Firstly, the carriers along the source-drain path will be subjected to a shift in the conduction path with the increase of implant thickness (Fig. 3.4(a)). This in turn has secondary effects such as a) increased transit time of carriers and hence lower unity gain frequency (f_T) (b) degraded R_{ON} and (c) early g_m roll off. Secondly, as the depth increases the lateral field near the

implant-drain junction starts increasing. This filed is given by the equation

$$V_{BD-lateral} = \frac{\epsilon_s E_c^2}{2qN_{imp}} \tag{3.6}$$

where E_c is the critical breakdown electric field, q is the electronic charge. This produces large variations in the performance figure of merits. Thus the p-implant thickness is limited to a moderate value of 60nm for an n-well depth in excess of 200nm to obtain an optimum V_{BD} - R_{ON} trade-off.

Fig. 3.5 shows four different regions with respect to p-implant variations. The shaded region in the middle indicates the optimum design window for p-implant parameters.

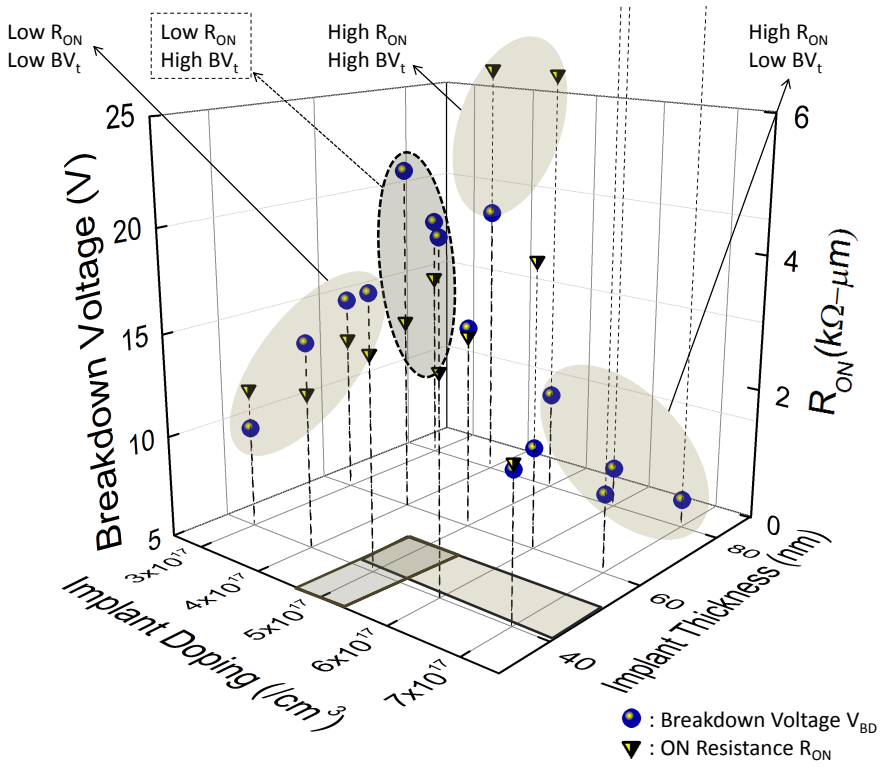


Figure 3.5: Plot of different $V_{BD}-R_{ON}$ regions. The shaded region at the bottom indicate the optimized design for V_{BD} and R_{ON} with respect to implant doping and implant thickness. All the breakdown simulations are performed at V_{GS}=0V and V_{DS}=6V.

3.1.2 N-well depth variation

In conventional devices, as the depth of n-well is increased, the breakdown characteristics and R_{ON} are expected to increase. The increase in R_{ON} is due to lack of sufficient charge density in the extended drain region. However, this phenomena is observed only upto certain range of n-well depth (150-200nm in our case), beyond which the breakdown characteristics and R_{ON} tend to remain unchanged. It is expected that incorporating the optimal condition of n-well depth that gives a good trade-off between $V_{BD} - R_{ON}$ of conventional devices into double RESURF device would improve the breakdown characteristics. However, the breakdown characteristics of double RESURF device was found to be degraded. This is because the device is more liable to undergo Kirk effect. This can be explained with the following equation.

In eq.(2.6), $n(e)$ is given by

$$n(e) = \frac{I_d/t_{eff}}{qV_{sat}} \tag{3.7}$$

Where t_{eff} is an effective passage width of the drain current, given by $t_{eff} = X_{nwell} - t_{dep}$.

When the total integrated charge density of n-well is increased, the depletion thickness t_{dep} governs the n-well area in such a way that t_{eff} becomes negligible. This causes the net carrier concentration to increase significantly over the background doping and hence drain junction becomes susceptible to undergo Kirk effect. In this condition, if the additional lateral high field component (p-implant/drain junction) is large in magnitude, then the junction is more prone to breakdown occurrence. Hence the n-well depth has to be increased. This relaxes the field over the large n-well area and prevents the field confinement at the drain terminal. The contour plots shown in Fig. 3.6 illustrates the variation of the peak electric field and the impact ionization due to hotspots at different regions for varied n-well depths (200nm-350nm).

On incrementally increasing the n-well depth, it is observed that (Fig. 3.6) the field lines start terminating vertically at the implant-n-well junctions and near gate oxide edge (as that of the conventional device). This increases the breakdown value to a maximum of 23V and balances the charge condition resulting in a low R_{ON} of 2.5kΩ (Fig. 3.6(3a)). On further increasing the n-well depth above 320nm, it is observed that the field lines begin to align laterally at p- and n-well junction rather than terminating vertically at the implant-n-well junction. As a result, the p-n junction at the p- and

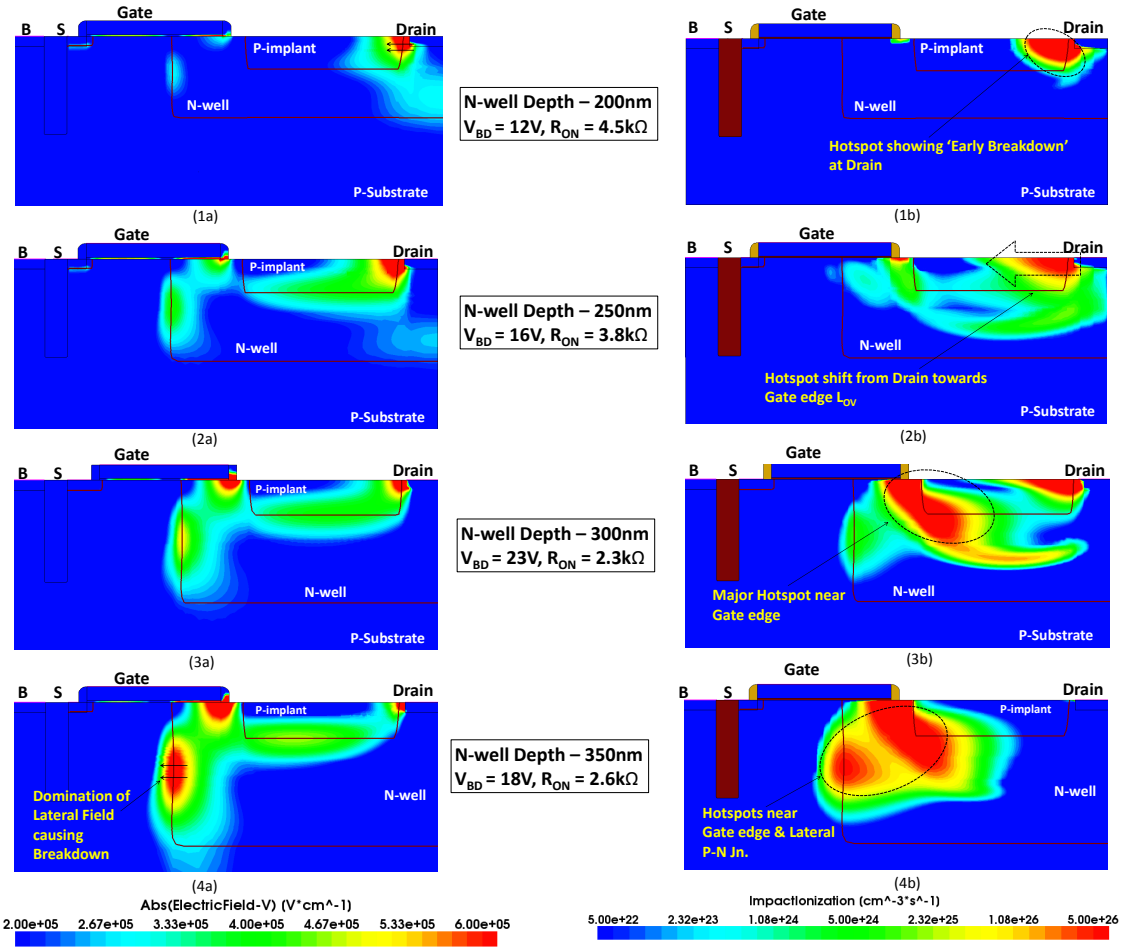


Figure 3.6: Contours on the left depicts the distribution of electric field and corresponding contours of impact ionization on the right for the n-well depths 200nm, 250nm, 300nm and 350nm. Simulations for breakdown voltage are carried out in off-state condition and R_{ON} in on-state

n-well boundary becomes the dominant lateral junction and locally generated hotspot regions will induce avalanche effect (Fig. 3.6(4b)).

Fig. 3.7 shows the variation of electric field at different regions taken (a) along the surface (Fig. 3.7(a)) and (b) taken at a depth of (≈120nm) below the surface (Fig. 3.7(b)). In Fig. 3.7(a) the regions of observation are the gate edge and the drain edge. It can be observed that as the n-well depth is increased the peak electric field increases at the gate edge and decreases at the drain edge. At a n-well depth of 200nm the electric field at the surface is lower near gate oxide and increases rapidly as one approaches the drain terminal. Whereas when the n-well depth is 350nm, it can be seen that the electric field peaks at gate oxide and correspondingly lowers at

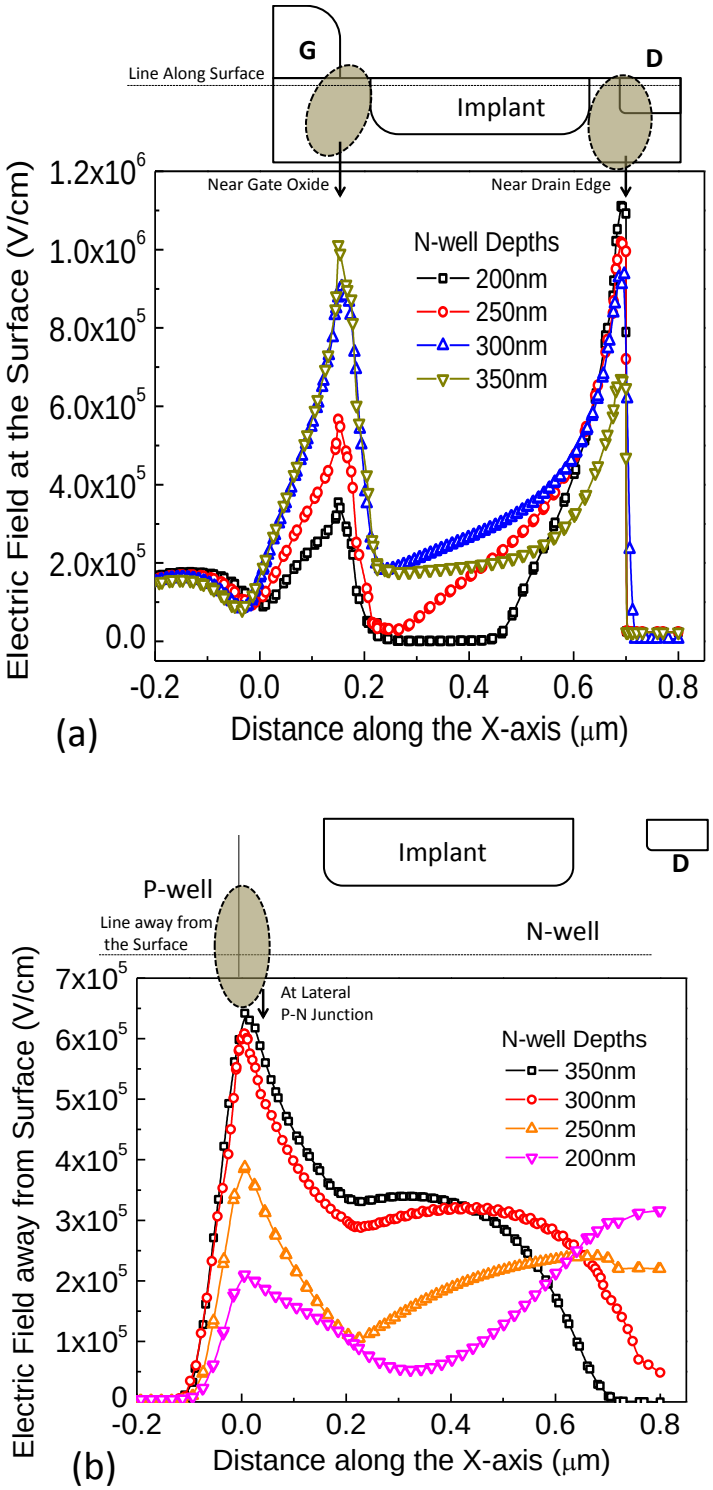


Figure 3.7: Plot of electric field variations for different n-well depths varying from 200nm-350nm taken from simulations of breakdown voltage carried out for off-state condition. (a) At the surface (b) In the bulk (at a distance of ≈120nm from surface).

drain edge. Similarly Fig. 3.7(b) shows the plots of the p- and n-well junction electric field deep in the bulk (at ≈120nm from the surface). It is observed that the electric field increases at the p-n- junction as the n-well depth increases and peaks (becomes dominant) at an n-well depth of 350nm. This can also be seen in Fig. 3.6(4a)) which depicts the domination of lateral field causing breakdown at 350nm.

Fig. 3.8 shows the $V_{BD} - R_{ON}$ variation as a function of n-well doping. Increasing the n-well doping above an optimum value of concentration ($\approx 3.2 \times 10^{17}/cm^3$), the spread of depletion width is restricted with increasing drain voltage. This results in attaining critical electric field at an early drain voltage leading to early breakdown.

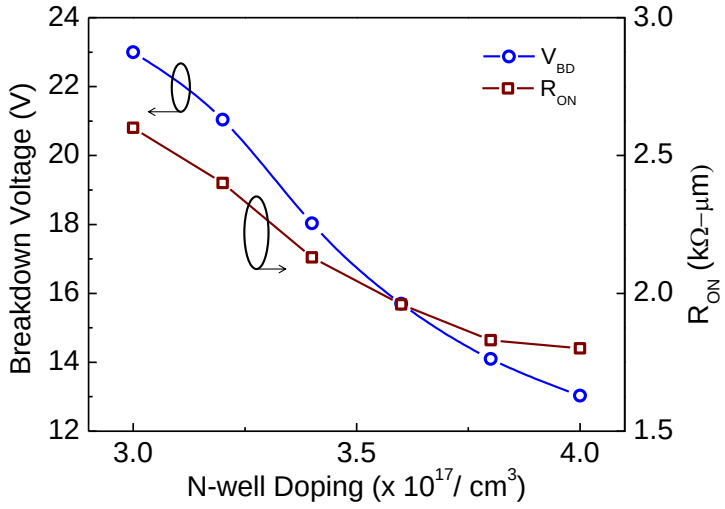


Figure 3.8: Plot of V_{BD}-R_{ON} variation as a function of n-well doping

3.1.3 Substrate depth variation

In conventional devices, if the substrate depth is increased, keeping the n-well depth constant, the field lines from the drain region tend to terminate at the n-well-substrate junction. This improves the breakdown performance of the device. Moreover, it is observed that there is a field crowding at the drain junction due to a significant number of field lines terminating near the substrate-n-well junction. (Fig. 3.9(a)). However, in double RESURF device, the field crowding occurs now at the drain-implant junction. The field lines tend to concentrate at the edges of p-implant and drain in order to satisfy the charge neutrality conditions (Fig. 3.9(b)). This field crowding increases the

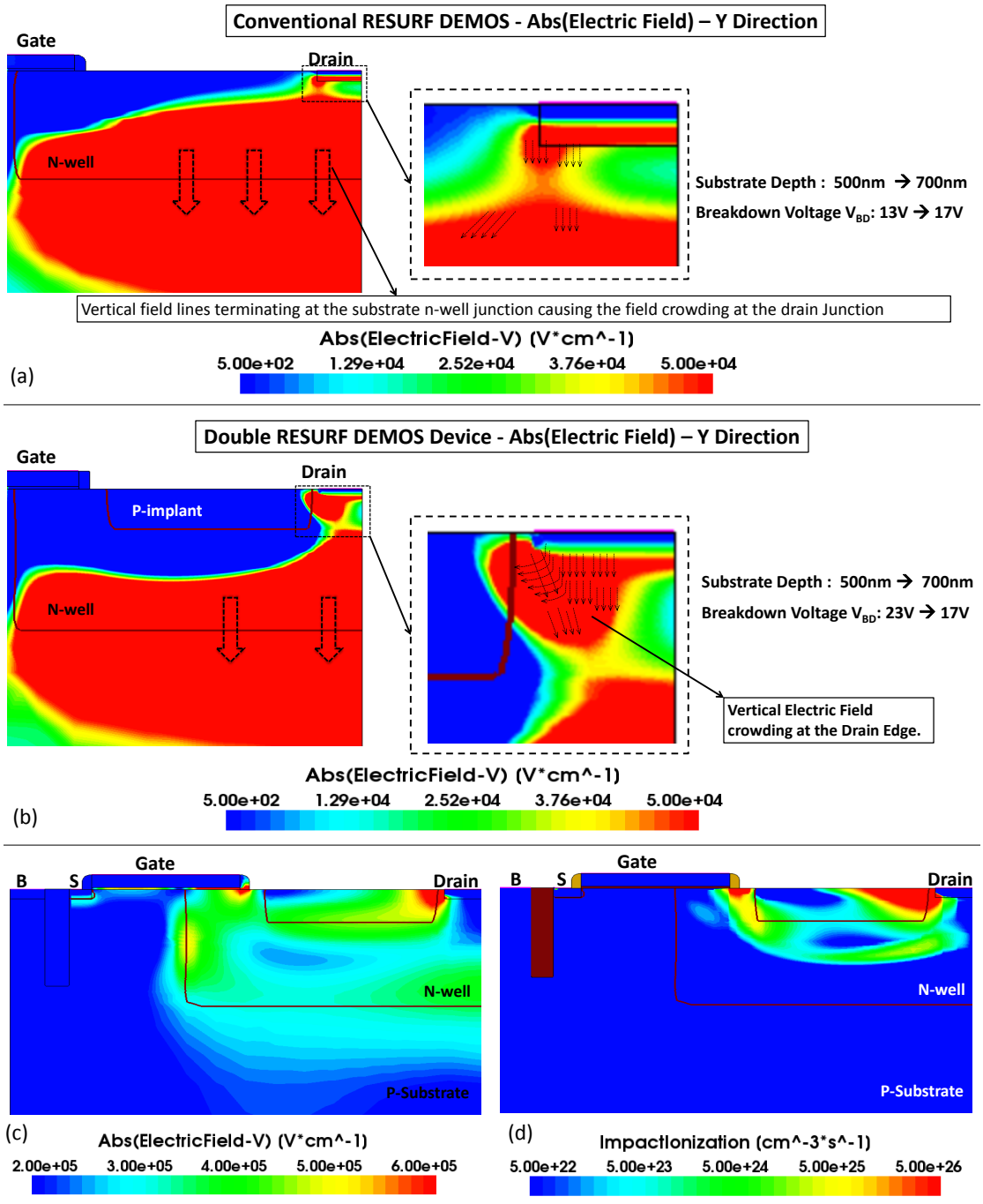


Figure 3.9: Contours of absolute Electric field for increased substrate depth in (a) conventional RESURF DeMOS and (b) double RESURF DeMOS. (c) shows the Y component of absolute electric field crowding at the drain edges corresponding to variation in substrate depth, (d) Impact Ionization showing the larger hotspot near the drain terminal

possibility of producing hot holes at the p-implant drain edges leading to breakdown (Fig. 3.9(d)).

Taking into consideration all the above mentioned electrical parameters, the best performance of the device is observed for the following device parameters. L_G=250nm, t_{OX}=5nm, L_{Drift}=700nm, width W=1μm, substrate doping of $3.5 \times 10^{16}/cm^3$ and n-well doping of $3.5 \times 10^{17}/cm^3$. With these design modifications, the double RESURF DeMOS device exhibited a larger breakdown voltage V_{BD} of 23V at a low R_{ON} of 2.5kΩ.

3.2 Conclusion

This chapter presents the impact of varying device design parameters of a double RESURF device on V_{BD} and R_{ON}. The optimized double RESURF device shows the V_{BD} improvement of 76.9% in comparison to the conventional device.

Chapter 4

Triple RESURF (Single SJ, $X_{imp} > 0$) DeMOS Device

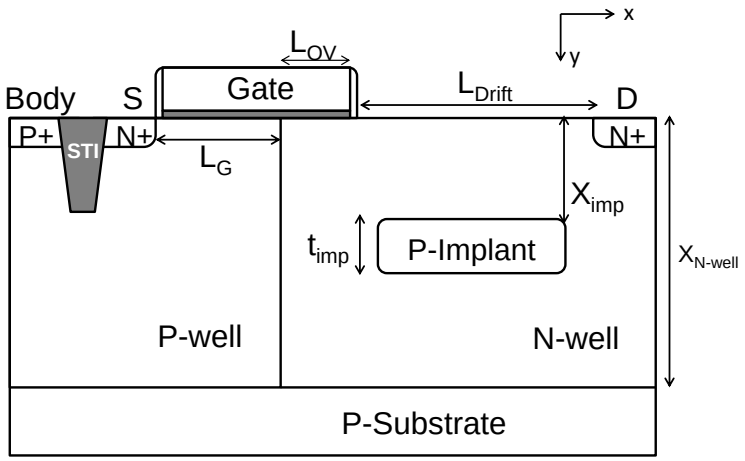


Figure 4.1: Schematic of triple RESURF (Single Superjunction with $X_{imp} > 0$) DeMOS device

Fig. 4.1 shows the structure of a triple RESURF or Single Superjunction with $X_{imp} > 0$ DeMOS device. In this device the p-implant is kept floating in the drift region much below the surface. Unlike double RESURF DeMOS (or Single SJ with $X_{imp} = 0$ DeMOS), triple RESURF DeMOS has a p-implant deep in the bulk. Due to this, the charge coupling happens around the floating p-implant. In a double RESURF device, the electric field gets modulated in the lateral direction, while in a triple RESURF DeMOS, the electric field extends both laterally and vertically Hua *et al.* (2010). With this structure the overall electric field in the drift region gets altered.

Therefore, the impact ionization at the p-n junction substantially gets lowered and device breakdown voltage increases.

Similar to the double RESURF device, the performance of triple RESURF is also highly sensitive Shan *et al.* (2011) and dependent on the physical parameters of the device namely 1) implant placement distance 2) implant thickness and 3) implant doping.

4.0.1 Implant placement - X_{imp}

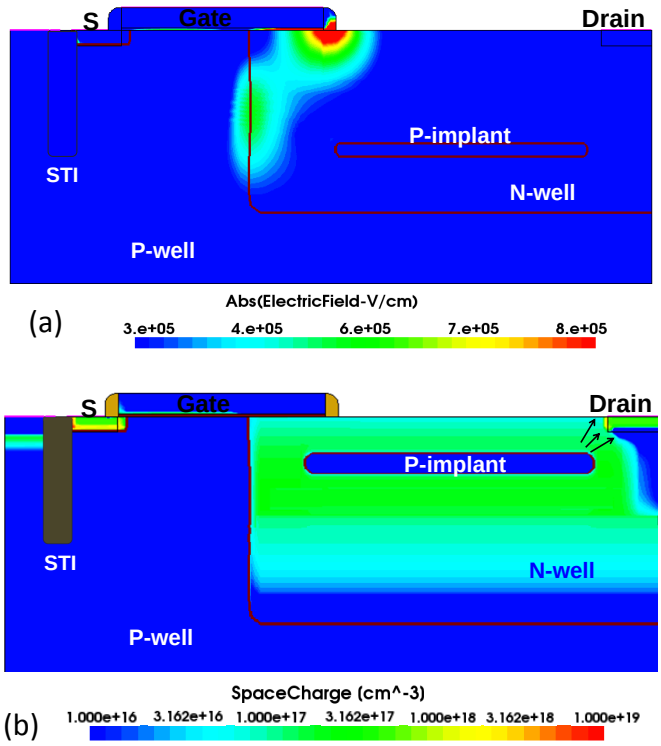


Figure 4.2: Filed contours with respect to implant placement. (a) Electric field at the gate oxide edge for larger X_{imp} (b) Space charge extending to the drain region for smaller X_{imp}.

The implant placement is the distance at which the RESURF p-implant is placed deeper from the surface. When the implant is placed at a larger X_{imp} from the surface, its influence on the electric field at gate-overlap edge E_y(x,0) is limited and hence breakdown occurs at an early stage as the electric field at gate-overlap edge reaches the critical field E_{Crit} ($E = dV/dX$). The field lines terminate into gate-oxide before the field lines start sinking with the junctions formed with p-implant and n-well

drift region (Fig.4.2(a)). On the other hand, if the implant is placed at a smaller X_{imp}, closer to the surface, it is more prone to premature avalanche initiation due to the elongation of the depletion region in drain region (Fig.4.2(b)). Since p-implant and n-well junction is a p^{+}n vertical junction, the maximum depletion width is given by

$$W_{dep-Max} = \frac{2\epsilon_{Si}(V_{bi} + V_D)^{1/2}}{qN_D} \tag{4.1}$$

where V_{bi} is the barrier potential of the junction and V_D is the drain potential. But this maximum depletion width $W_{dep-Max}$ shall be limited by the fact that depletion region hits the drain region before reaching the surface. A plot of variation of V_{BD} and R_{ON} as a function of implant placement is shown in Fig. 4.3.

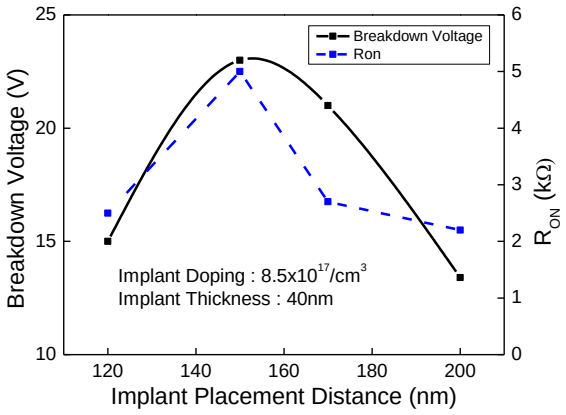


Figure 4.3: Plot showing V_{BD}-R_{ON} as a function of implant placement distance from the surface.

4.0.2 Implant Doping

Implant doping is another important parameter which specifies the boundary for V_{BD}/R_{ON}. It is seen that as the doping of the implant is increased, the breakdown characteristics also improve. However, for a device with higher p-implant doping concentration, a drain bias causes the electrons to gain high energy at an early drain voltage and turn them into hot electrons. This leads to avalanche multiplication and impact ionization (Fig. 4.4(a)-(d)). Hence the doping of p-implant should be kept moderate (i.e $X_{N_D}N_D = X_{N_A}N_A$) in such a way that the junction field,

$$E_{Max}(x, X_{imp}) = -\frac{qN_D W_{dep}}{\epsilon_{Si}} \tag{4.2}$$

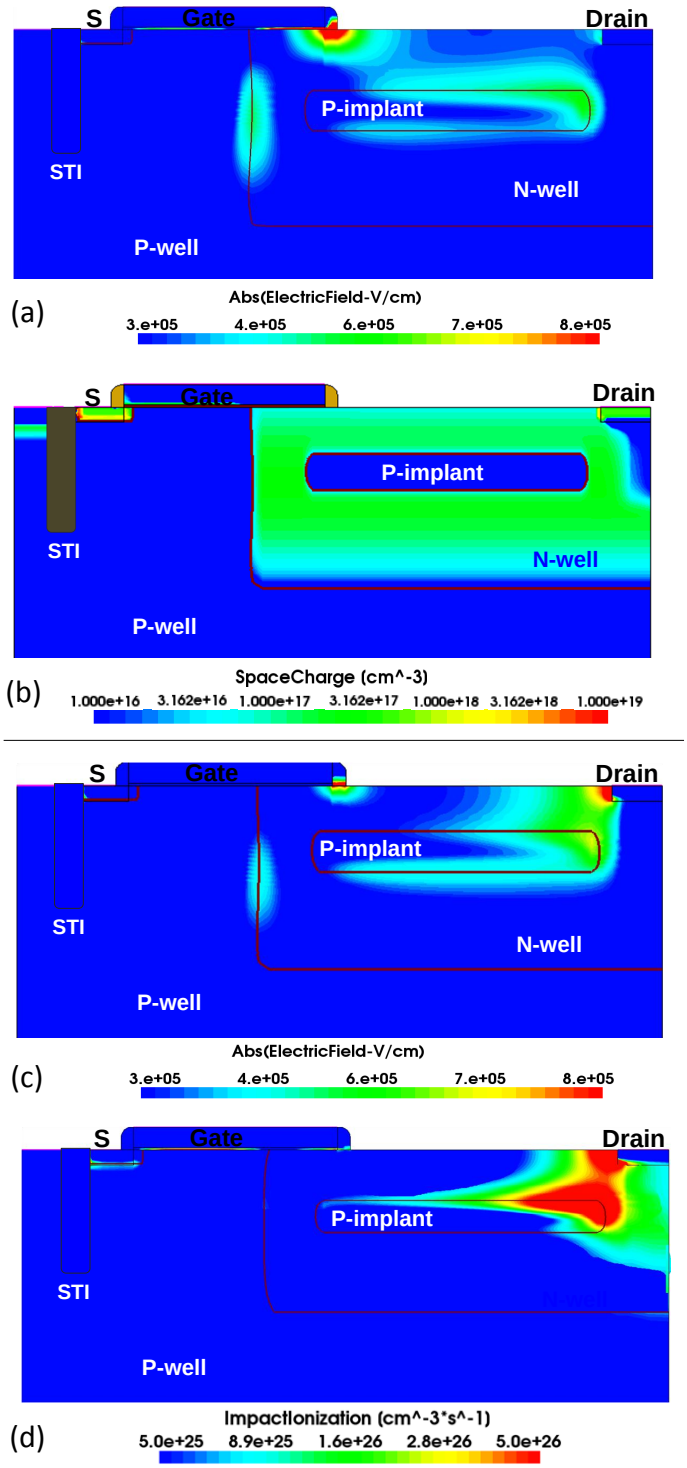


Figure 4.4: (a)-(d) Electric field contours showing the effect of Implant Doping. (a)Electric field distribution for moderate ($7.5 \times 10^{17} cm^{-3}$) p-implant doping. (b)Space charge distribution (c) Peak electric field at the drain junction with high p-implant doping ($9 \times 10^{17} cm^{-3}$) (d) Impact Ionization leading to early breakdown. V_{BD} simulaitons are performed for $V_{GS} = 0$

should not lead to premature failures. The variation of V_{BD} and R_{ON} as a function of implant doping is shown in Fig. 4.5.

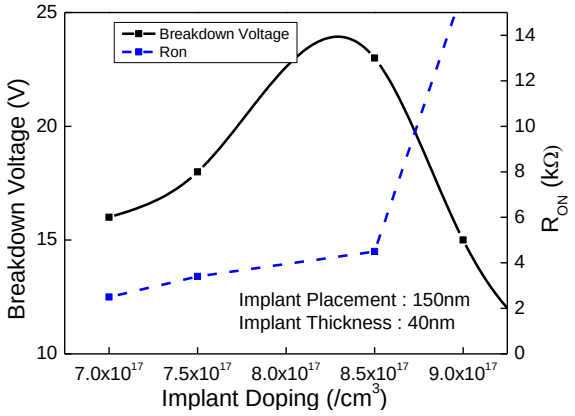


Figure 4.5: Plots showing V_{BD}-R_{ON} as a function of implant doping.

4.0.3 Implant Thickness - t_{imp}

The implant thickness is the thickness, the implant takes after the dopants get diffused in n-well area. This parameter is inter-dependent on both implant distance and doping concentration. If the p-region is implanted much deeper in the bulk with smaller t_{imp} as in Fig. 4.6(a), then the device behavior will be similar to that having a p-implant with large X_{imp}. On the contrary, if t_{imp} is large, implying a smaller X_{imp}, the depletion region ($W_{dep-Max}$) will soon hit the drain region limit. This will also result in a degraded carrier path from source to drain (Fig. 4.6(b)) and thus R_{ON} would increases significantly even though high breakdown characteristics are accomplished. Variation of V_{BD} and R_{ON} as a function of implant thickness is plotted in Fig. 4.7.

4.1 Design Guidelines

Given the fact that the most usual cause for breakdown being the punch through phenomena due to the proximity of p-implant to the drain region, it is important to find out optimal position, doping concentration and thickness of the p-implant to achieve best results. To arrive at a safe distance for the p-implant depletion to avoid breakdown, consider the following. Set a new boundary at a distance δL in the

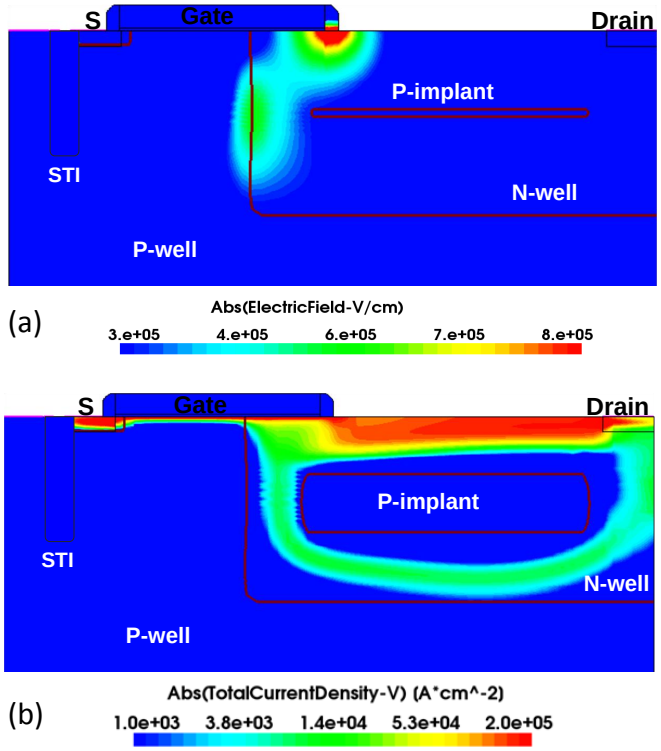


Figure 4.6: Contours showing the effect of varying implant thickness. (a) Electric field terminating at gate-oxide junctionbcausing early breakdown. (b) Absolute current density shown for larger t_{imp}. Simulations for V_{BD} are performed at $V_{GS} = 0$, and for R_{ON} at $V_{GS} = 1.8V$ and $V_{DS} = 6V$.

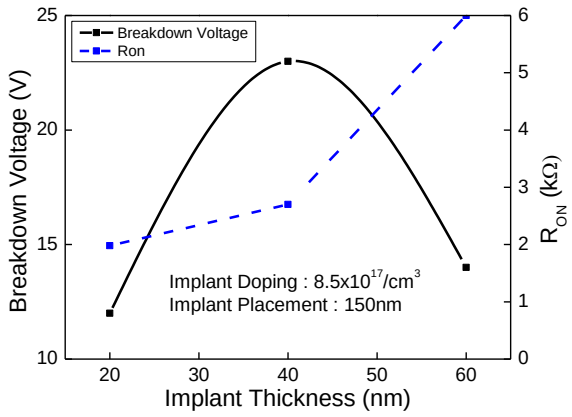


Figure 4.7: Plot showing V_{BD}-R_{ON} as a function implant thickness.

direction x and δX along direction y from the edge of the drain region as depicted in Fig. 4.8.

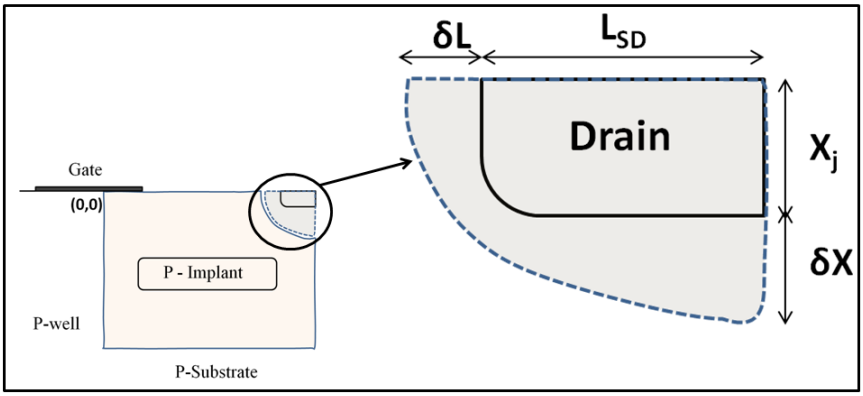


Figure 4.8: Schematic showing proposed depletion boundary for avoiding punch through with drain.

Consider the origin (0,0) to be at the left edge of the n-well below the gate region, and let L_{SD} be the length of the drain region. For the safe operation of the device, it should be ensured that the space charge region above p-implant does not reach the drain region under worst case operating conditions. To determine the location where the p-implant need to be placed $vis-\grave{a}-vis$ the drain boundary for achieving the best break-down performance, consider a new local frame of reference with its origin at the right top edge of the drain. Approximating the region around the drain to be part of an ellipse, as shown in Fig. 4.8, with its centre at the origin of this reference frame, the p-implant should be positioned in the bulk in such a way that its depletion region does not cross the elliptical boundary around the drain region. Taking $(L_{SD}+\delta L)$ as the semi-major axis and $(X_j+\delta X)$ as the semi-minor axis of the ellipse, any point (x,y) specified on the boundary of the ellipse satisfies the relation,

$$[(L_{SD}+\delta L)]^2y^2+[(X_j+\delta X)]^2x^2-[(L_{SD}+\delta L)]^2.[(X_j+\delta X)]^2=0 \tag{4.3}$$

From the above equation,

$$\begin{aligned} y^2 &= \frac{[(L_{SD}+\delta L)^2.(X_j+\delta X)^2]-[(X_j+\delta X)^2]x^2}{(L_{SD}+\delta L)^2} \\ y &= (X_j+\delta X)\sqrt{1-\frac{x^2}{L_{SD}+\delta L}} \end{aligned} \tag{4.4}$$

Similarly,

$$x^2 = \frac{[(L_{SD}+\delta L)^2.(X_j+\delta X)^2] - [(L_{SD}+\delta L)^2 y^2}{(L_{SD}+\delta L)^2}$$

$$x = (L_{SD}+\delta L)\sqrt{1-\frac{y^2}{X_j+\delta X}} \tag{4.5}$$

Thus the coordinates of a point on the ellipse can be obtained from equations(4.4-4.5).

Hence, the area of n-well depletion is given by,

Area of n-well-depletion = Area of n-well - (Area of elliptical drain boundary/4)

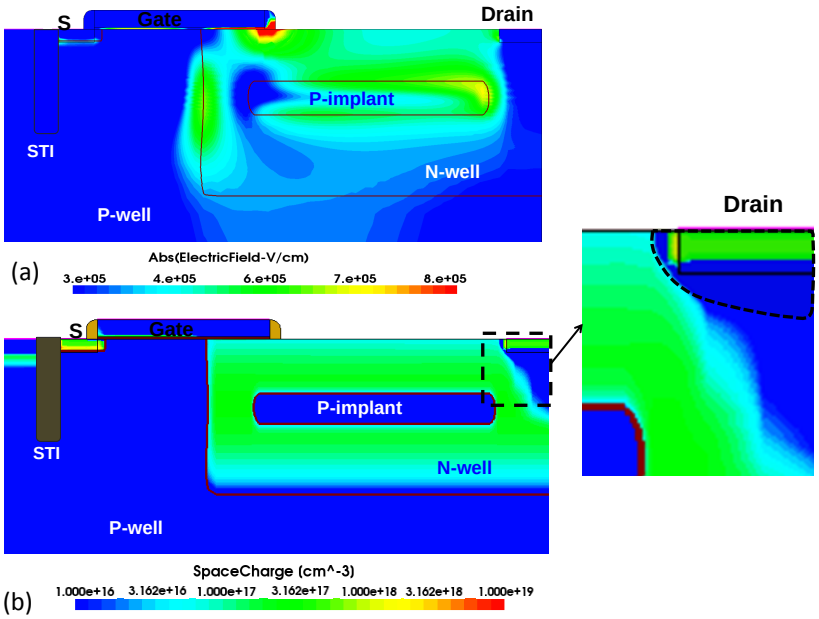


Figure 4.9: (a) Shows the optimized parametric depletion of entire n-well without punching the drain. (b) Contour showing uniformly spread electric field and reduced peak at gate-overlap edge.

$$Area_{Nwell-depletion} = [(L_{Drift}+L_{SD})X_{Nwell}] - \frac{\pi(L_{SD}+\delta L)(X_j+\delta X)}{4} \tag{4.6}$$

which states the three design parameters of implant should be adjusted such that if the depletion region due to the p-implant lies within the boundary defined by limits,

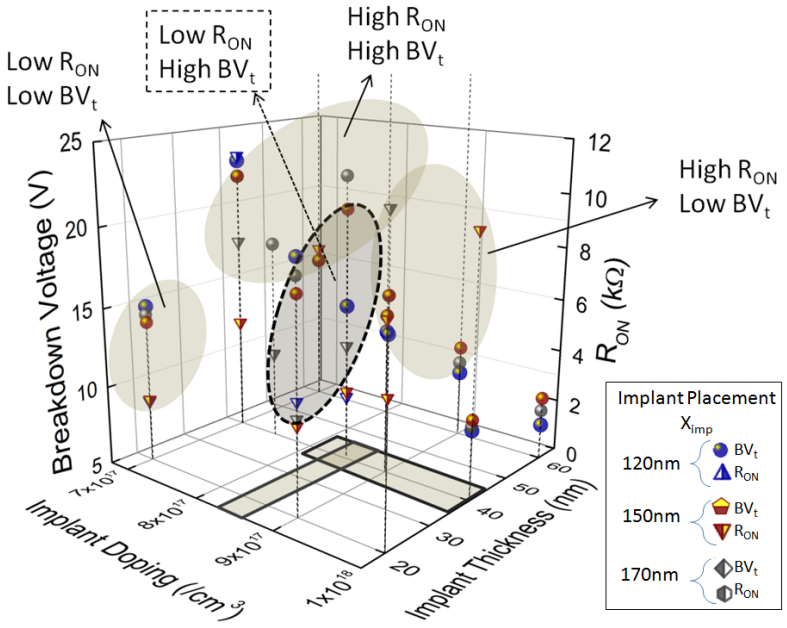


Figure 4.10: Plot of V_{BD}-R_{ON} as a function of design parameters.

$$0 \leq x \leq (L_{SD} + \delta L)\sqrt{1 - \frac{y^2}{X_j + \delta X}} \text{ and } (X_j + \delta X)\sqrt{1 - \frac{x^2}{L_{SD} + \delta L}} \leq y \leq X_{nwell}$$

the possibility of premature breakdown will be small. Thus the three parameters are optimized to obtain best performance. This is shown in Fig. 4.9. The contour plots show that the space charge region does not punch the drain region and the electric field is spread uniformly, resulting in achieving higher breakdown voltage with low R_{ON}. Fig. 4.10 shows the variation of V_{BD} and R_{ON} with variation in implant parameters, viz., doping concentration, thickness and distance from the drain edge. It can be seen that when the implant is placed at a distance of 170nm from the surface with an implant thickness of 40nm and optimum doping concentration of $8.5{\times}10^{17}/cm^3$, high V_{BD} of 21V at low R_{ON} of 2.5kΩ is achieved (shaded area with dotted lines). Altering the values of implant parameters alters the V_{BD}/R_{ON} values (other shaded areas without dotted lines in Fig. 4.10.

4.2 Conclusion

This chapter describes triple RESURF device in detail. To achieve higher V_{BD} and lower R_{ON}, the relative position of p-implant from the surface and from the drain boundary is computed. Simulations are carried-out by varying doping concentration, thickness & position of the p-implant in the bulk and V_{BD} and R_{ON} values are recorded. The optimized triple RESURF device shows the V_{BD} improvement upto 61.5% in comparison to the conventional device characteristics.

Chapter 5

3D Multiple RESURF DeMOS

5.1 Introduction

Lossless and high performance power devices are demanded by the modern SoC technology in power electronics. DeMOS devices stand as the finest class of power devices. Power Integrated Circuits (PICs) have been operating with the voltage levels upto 20V. Since the evolution of scaling, SoC based integration has been in great demand. Therefore, 3D Superjunction (SJ) devices are being revisited to further improve the performance Fujihira (1997). However, in Xu *et al.* (2003) it is said that the ideal case of conventional Superjunction drain extended devices can provide a breakdown voltage of about 20V/um. Experimentally, a V_{BD} of 12-15V has been achieved (for a drift a region of 1 μm long) with a R_{ONsp} of 7.8mΩcm^2. Conventional SJ devices consists of alternate stacks of n- and p-regions in the drift region. Under an applied bias at the drain terminal, and when the device is in off-state condition, n-regions are depleted by the neighboring p-layers and the p-substrate.

From the literature survey, we find that following are some of the issues to be considered while attempting performance improvement.

1) Accomplishing good breakdown characteristics is possible only if the total depletion region is lead by the vertical p-n junctions. Inspite of creating the Superjunctions laterally, it provides only a low R_{ON} path and the V_{BD} is still dominated by n-well/p-substrate junction which is same as in the case of 2D conventional RESURF device Qiao *et al.* (2012).

2) The conventional 3D SJ devices have multiple p-n stacks sandwiched between one another. Due to this, the device suffers from charge imbalance condition known as

Substrate Assisted Depletion (SAD). This effect is due to the fact that p-layers in the drift region are depleted by neighbouring n-regions, while the n-layers are depleted by neighbouring p-regions (p-substrate & p-stacks) Xu *et al.* (2003) Qiao *et al.* (2012).

3) Therefore, to avoid SAD effect, SOI based Superjunction devices were proposed. The structure contains p- and n-stacks of silicon layers above the buried oxide layer. The depletion of n-stacks by p-substrate is isolated by the buried oxide layer, so that charge balance conditions are maintained Wang *et al.* (2009). However, there are issues in SOI based 3D Superjunction devices and they are listed below.

a) Buried Oxide layer (BOX) and substrate layer below the SOI region forms the parasitic MOS structure whereby creating the additional field due to charge interaction between the n-stack regions and underlying substrate in the off-state. This alters the delicate charge balance conditions between n-p layers leading to V_{BD} degradation. The charge balance condition can be gained only when the total charge of the drift region Q_D is equal to $Q_A + Q_{A-Body} + Q_{A-Sub}$ where Q_A is the p-pillar charge, Q_{A-Body} is contribution of the p-body depletion charge and Q_{A-Sub} is induced charge by the BOX layer Cortes *et al.* (2007).

b) Inspite of having the drain biased at a low voltage, the current conduction is confined to a very narrow region at the centre of the n-stack regions. This is due to high lateral fields at the junction transitions of p-n layers.

c) The buried oxide layer in the device increases the current crowding effect at the gate-drift transition region. As a result of reduced conduction path area, the increased spreading resistance at the gate-drift region increases the channel resistance. Further, even if the drift region resistance is decreased, the channel resistance $R_{Channel}$ dominates and hence the total on-resistance increases. Hence, the width of n-stack layer should be kept sufficiently high. Cortes *et al.* (2007).

4) Another approach to suppress the SAD effect is to divide the p-stack regions into different dosage of doping concentration Quddus *et al.* (2004). The p-stack layers are split into two regions with variation in the doping concentrations. The p-stack will have higher dosage at the one side than the rest of the region. This will ensure the charge balanced conditions and the new peak electric field component is seen at the $p^+ - p^-$ junction. But, there is another factor that has to be considered precisely, i.e the difference in doping concentration in the p-stack layer ($\delta N = \frac{N_A - N_D}{N_D}$ where

N_D -doping of n-stack and N_A -doping of p-stack). If the δN factor is higher in magnitude, then there is higher chance of early premature breakdown that occurs at the p/p^- transition junction. On the contrary, if the δN factor is too low, then the modulation effect of suppressing the peak surface electric field to be very poor. Hence, it is essential to look at the δN factor to be well optimized, such that the charge imbalance factor is too small. The challenging aspect is to maintain δN factor very precisely, as the charge imbalance factor is highly sensitive to δN.

With these facts from literature, it is found that there are multiple drawbacks that can be observed in conventional 3D Superjunction devices. Therefore, it is important to look into further possibilities in conventional SJ device to attain the maximum efficiency in depleting the drift region under reverse bias conditions so as to achieve good V_{BD}/R_{ON} ratio.

5.1.1 Conventional 3D SJ

To understand and analyze the further possibilities of arriving at higher V_{BD} and lower R_{ON} values, the conventional 3D Superjunction device is built (as shown in Fig. 5.1) and simulated using Sentaurus TCAD simulator with the same device dimensional specifications mentioned in Chapter2.

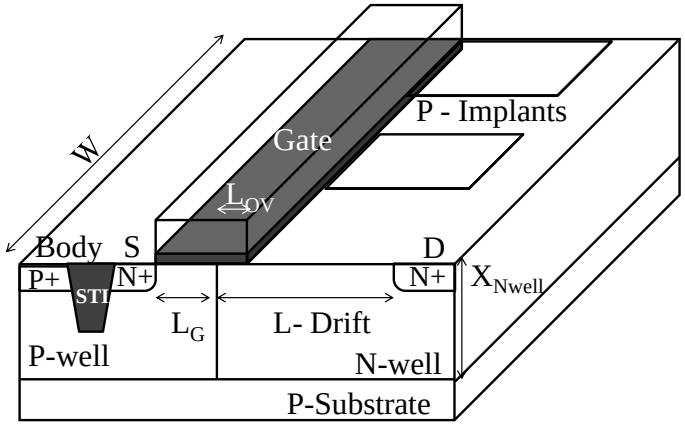


Figure 5.1: Schematic of conventional 3D Superjunction device

To attain higher V_{BD} and lower R_{ON} values, the only parameters that can be examined with the conventional 3D device are p-layer doping & depth and n-well doping & depth. For an n-well doping of 3x$10^{17}/cm^3$ and depth of 30nm,

a) P-implant doping is varied by keeping the p-implant depth constant. The breakdown characteristics is found to remain same. At a higher implant doping, breakdown spot occurs at the gate oxide region, as shown in Fig. 5.2

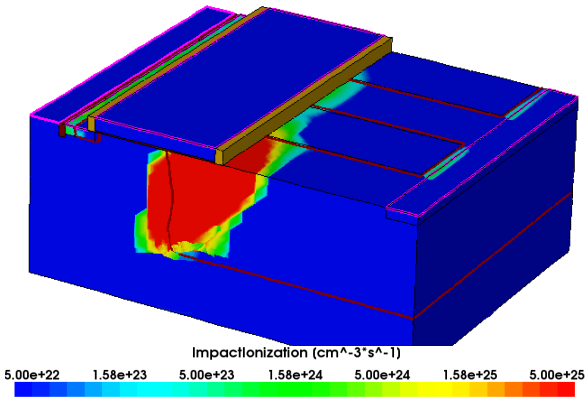


Figure 5.2: Contour showing premature breakdown occurring near gate oxide region.

b) Secondly, the p-implant depth is varied for a fixed p-implant doping. The breakdown characteristics is found to be similar to that in the case of p-implant doping variation.

After certain limit of p-implant doping concentration (9x$10^{17}/cm^3$), and p-implant depth (60nm), the drain-p-layer transition edge breaks down at early drain voltage (Fig. 5.3). Also, on reducing the n-well doping to 2x$10^{17}/cm^3$, although the R_{ON} increases, the breakdown characteristics are seen to be better than that of n-well doping with 3x$10^{17}/cm^3$, as expected. Now, the only parameter to be explored is the n-well depth. Interestingly, the n-well depth showed very little variation in V_{BD} and R_{ON} values.

One of the simple techniques that can be implemented in Superjunction devices is to modify the n-well depth. The n-well depth modification should be such that the substrate depletion effect should be mitigated and at the same time achieve best V_{BD}, R_{ON} values. Firstly, by having an larger n-well depth, the conduction area is higher and the RESURF principle is applied effectively. Secondly, the substrate assisted interaction with n-regions is reduced. Hence, the tendency of imbalancing the charge conditions is very low. Further, n-regions are exclusively used for creating vertical depletion in the n-drift region. Thus, by doing all the above said modifications, for a given n-well doping of 2x$10^{17}/cm^3$ and increasing the depth to 320nm, the best breakdown voltage obtained is 14-15V (see Fig. 5.5) for an on-resistance of 3.6kΩ.

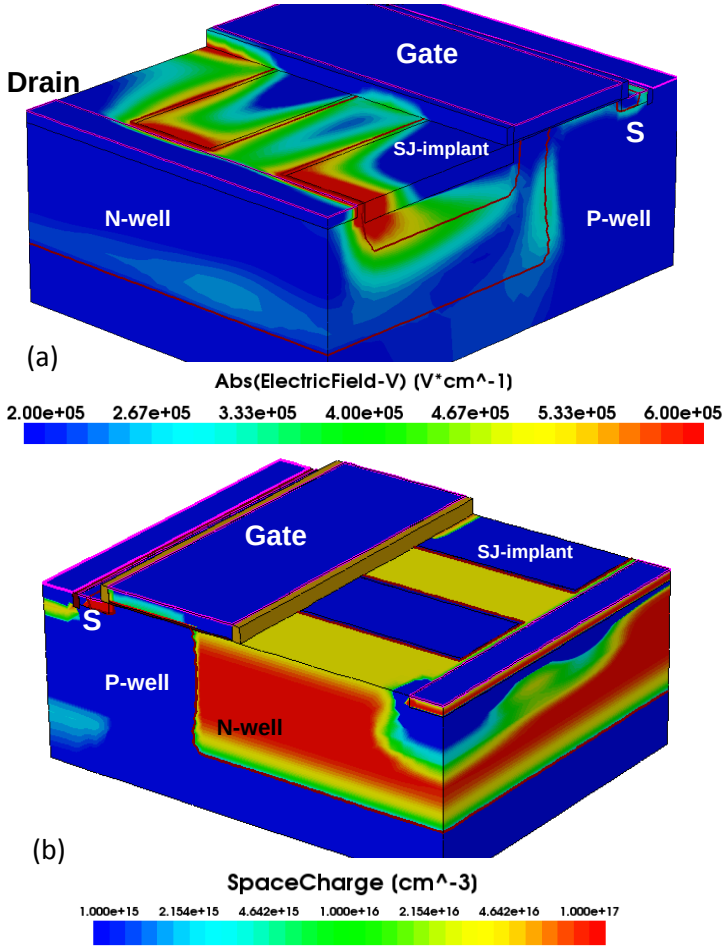


Figure 5.3: Contour showing (a) Peak electric field at the drain-SJ implant junctions (b) Unbalanced charge condition

5.2 3D Multiple RESURF-I Superjunction DeMOS

Apart from enlarging the n-well region (n-well depth), the device can also be modified with p-region implantation. Instead of creating separate p- and n-stacks in the drift region, n-well is doped moderately high and p-regions are implanted in the form of pocket islands. The structure shown in Fig. 5.6 is a 3D Multiple RESURF-I Superjunction DeMOS device. The 3D structure shown has same dimensions as that of the conventional SJ structure. The width of the device is 1μm. The p-islands are implanted at the top surface, equidistant from one another along the length of drift region. Similar to double and triple RESURF SJ structures, the p-regions play the role of reducing the surface field. Also, the n-drift region is depleted by substrate and

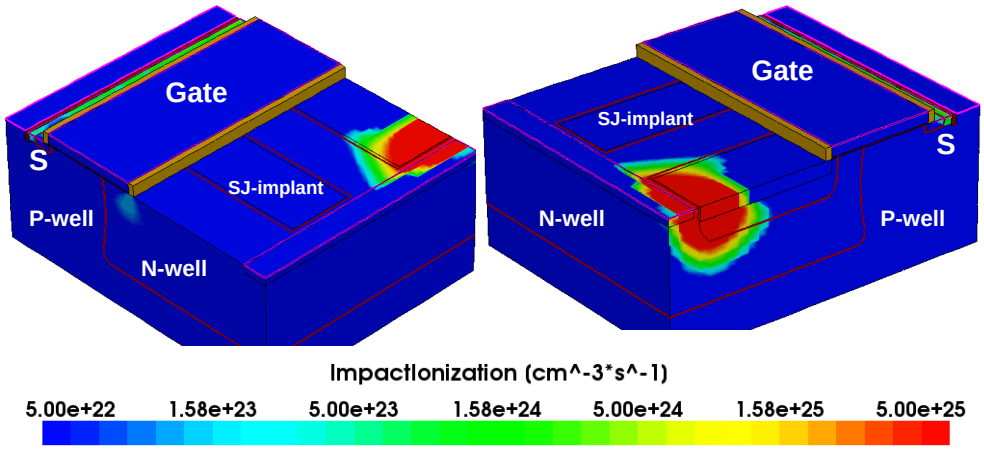


Figure 5.4: Contour showing premature breakdown occuing near drain-p region

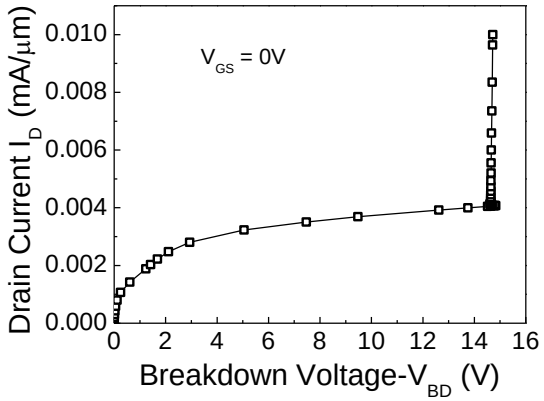


Figure 5.5: Plot of I_D Vs V_{BD} for the conventional 3D Superjunction device

the conventional RESURF action is conformed. Since there are no separate n-stack regions, the Substrate Assisted Depletion effect is not seen.

On applying the drain bias, the depletion region widens and reaches the p-implant regions. Because of the junction formed at p-implant/n-well region, the new peaks of the electric fields are created at the edge of implants, thus reducing the peak electric field residing at particular p-well/n-well junction.

5.3 3D Multiple RESURF-II Superjunction DeMOS

Fig. 5.7 shows the schematic of the 3D multiple RESURF-II DeMOS device. The device has multiple p-implants along the width of the n-drift region. This helps in 3D expansion of depletion regions, thereby increasing the multiple RESURF actions in

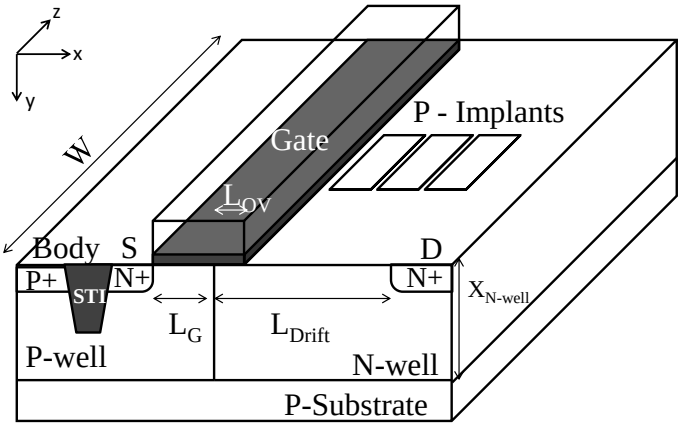


Figure 5.6: Schematic of conventional 3D Multiple RESURF-I DeMOS device

a distributed way. The multiple peaks that occur helps in reducing the overall field crowding and improves V_{BD} and R_{ON}. The current conduction occurs in the space between the implants.

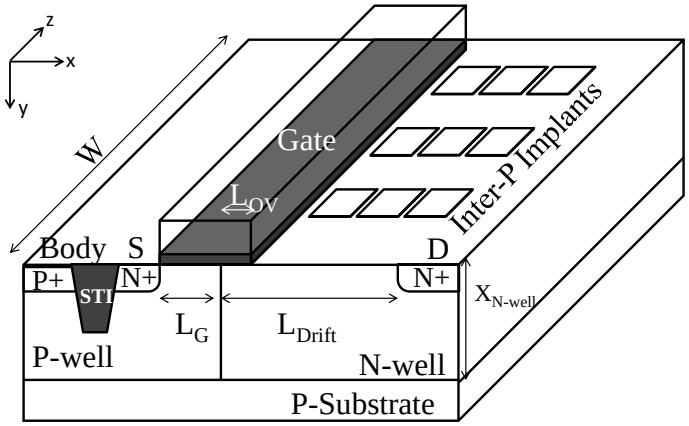


Figure 5.7: Schematic of conventional 3D Multiple RESURF-II DeMOS device

Fig. 5.8 shows the electric field along the lateral dimension taken along the surface. It can be observed that the peak electric field is slightly higher for conventional 3D Superjunction than the other two multiple RESURF SJ devices. Thus the multiple RESURF SJ devices are less prone to gate oxide breakdown failures. Secondly the circled area in Fig. 5.9 shows that multiple RESURF SJ devices render higher breakdown voltages upto 19V for the same on-resistance compared to the conventional 3D SJ device.

5.4 Conclusion

This chapter presents the description of 3D multiple RESURF devices and the effect of modifying p-implant parameters on V_{BD} and R_{ON} without altering the device on-state performance. The optimized multiple RESURF devices show an improvement in V_{BD} upto 50% in comparison to the conventional device characteristics.

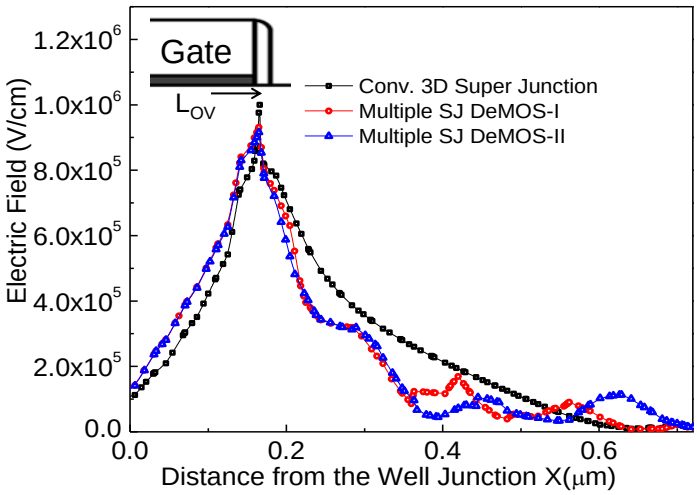


Figure 5.8: Comparison of electic field profile for the three 3D Superjunction structures

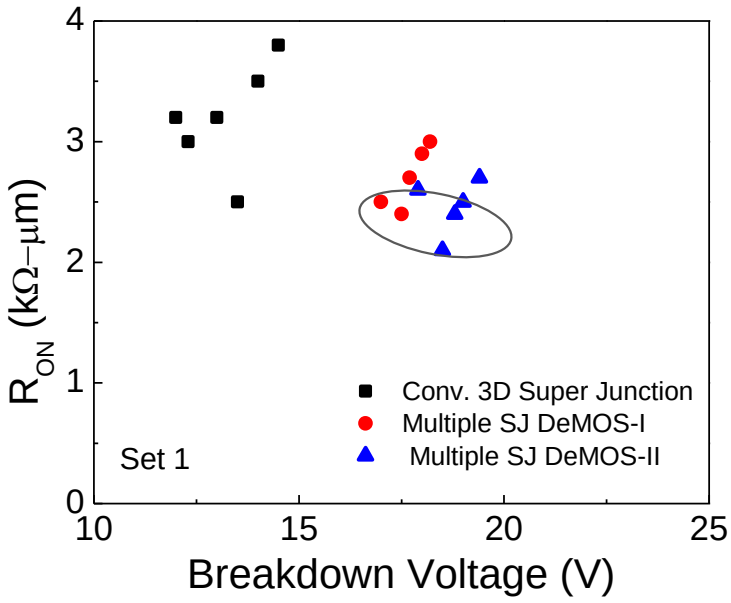


Figure 5.9: Comparison of breakdown voltage Vs on-resistance plot for all the 3D Superjunction devices

Chapter 6

Comparison of Performance and Reliability Co-design

6.1 Introduction

In this chapter, we compare different performance metrics of various devices discussed previously. The devices are designed and simulated using Synopsys TCAD 3D software. Fig. 6.1 shows the 2D (Double RESURF or Single Superjunction with $X_{imp} = 0$ and triple RESURF or Single Superjunction with $X_{imp} > 0$) and 3D (Multiple Superjunctions-I and II) Superjunction structures respectively. Different RESURF SJ structures shown are studied using TCAD simulations and compared with the conventional DeMOS structure for their suitability in integrated RF applications.

6.2 On-Resistance vs. Breakdown Voltage Trade-off

In this section we present a comparison of trade-off between on-resistance (R_{ON}) and breakdown voltage (V_{BD}) of various SJ-DeMOS devices with conventional non-STI DeMOS device. TCAD and calibration setup used in this work are similar to the one presented in earlier works Shrivastava *et al.* (2010*a*) and Shrivastava *et al.* (2010*b*). The key to minimize on-resistance while maximizing breakdown voltage is to distribute space charge as much as possible in order to suppress electric field at a given drain voltage without significantly (i) affecting cross-sectional area available for car-

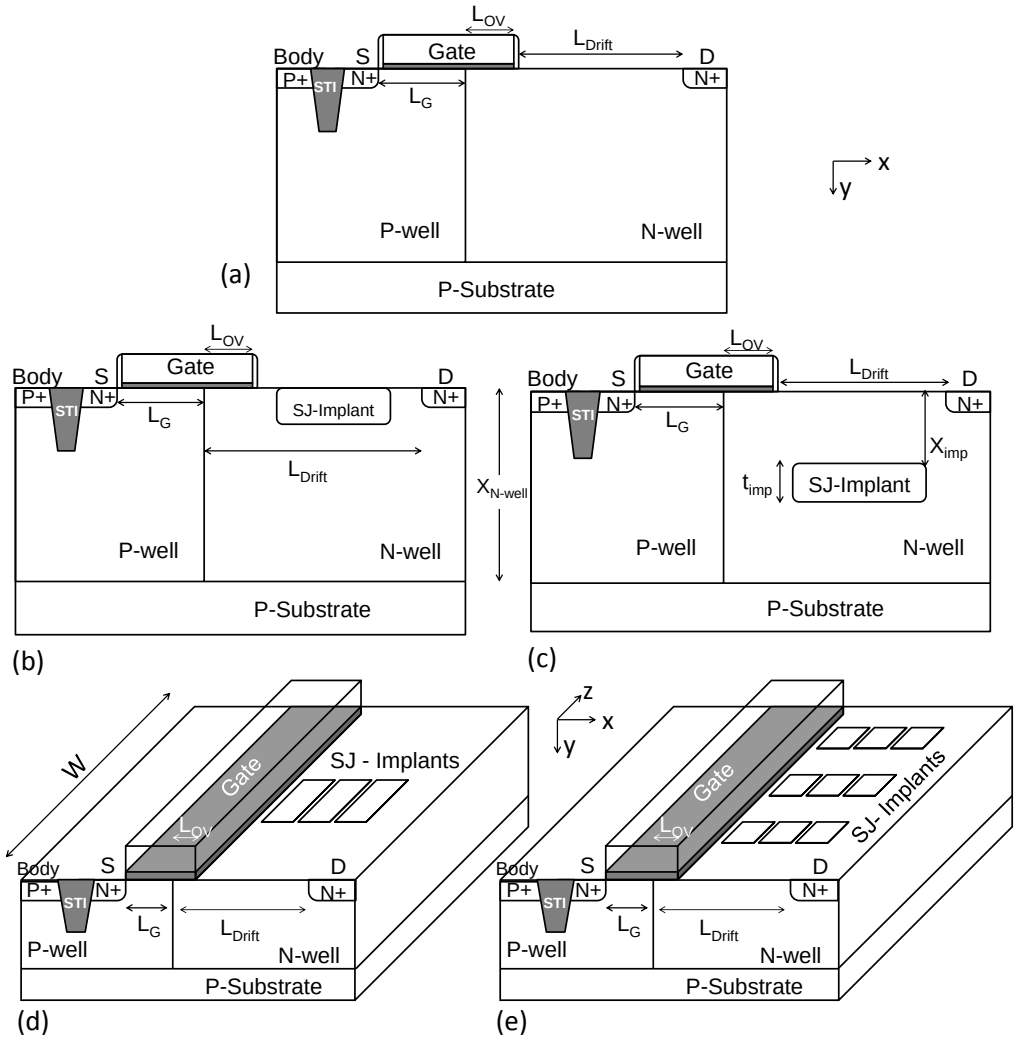


Figure 6.1: Schematic showing different SJ-DeMOS structures (a) Conventional DeMOS (b) Single SJ with $X_{imp} = 0$ (Double RESURF). (c) Single SJ with $X_{imp} > 0$ (Triple RESURF) (d) Multiple RESURF-I (e) Multiple RESURF-II

rier transport in the drift region and (ii) lowering background doping concentration. Fig. 6.2 and Fig. 6.3 shows electric field distribution across various SJ devices when the super-junction doping is increased (in figure from left to right) and compares it with the conventional non-STI DeMOS device. It shows that various SJ-DeMOS devices with lower SJ doping have an electric field profile similar to that of conventional DeMOS device; however, when SJ doping is increased the electric field gets shared between well junction as well as SJ region to n-well junction. Moreover, the field around the SJ region increases when the SJ doping concentration is increased. Independent

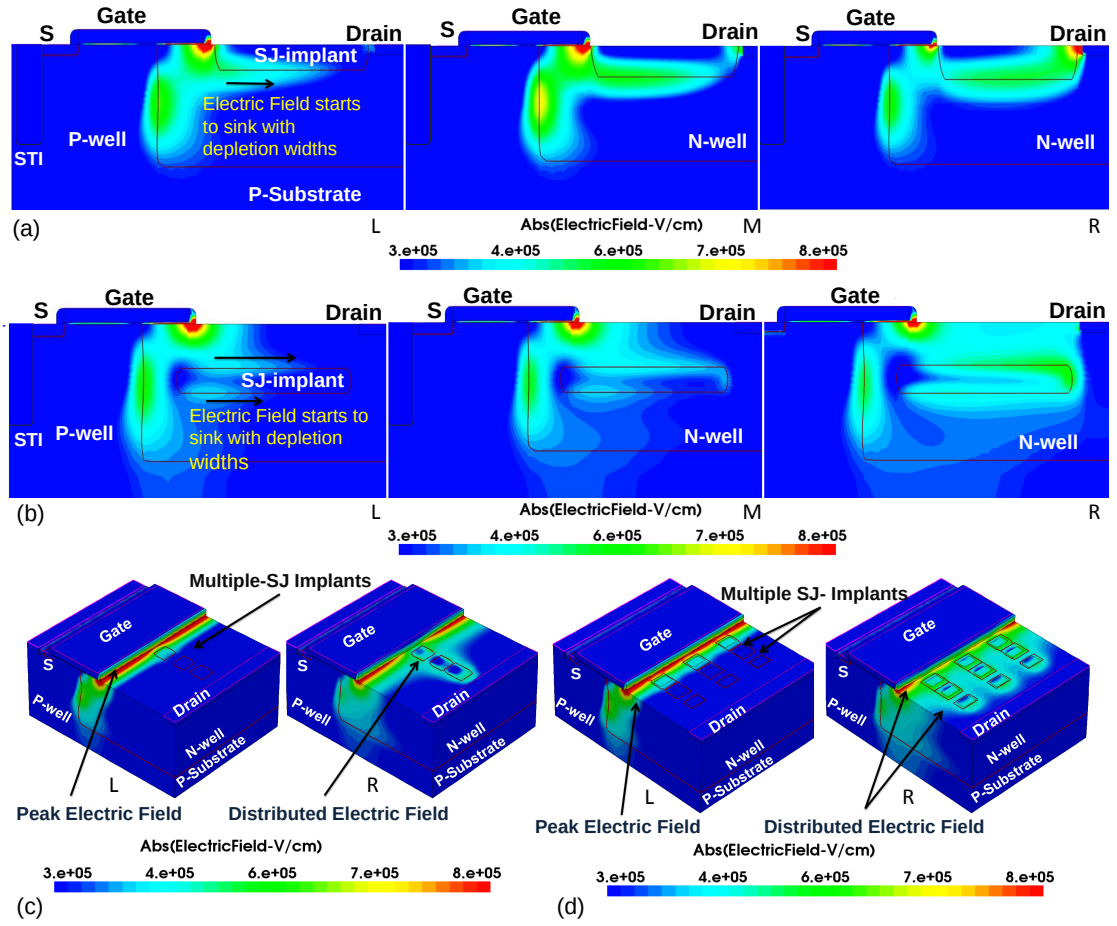


Figure 6.2: (a) - (d) Electric field contours across various Superjunction devices when the SJ doping is increased from left (L) to right (R): (a) Single SJ with $X_{imp} = 0$ DeMOS, (b) Single SJ with $X_{imp} > 0$ RESURF DeMOS, (c) and (d) Multiple SJ-DeMOS.

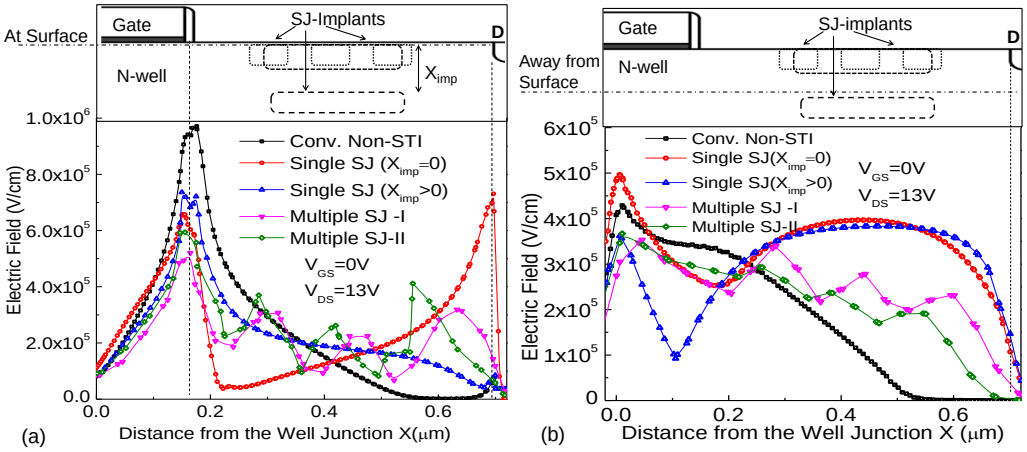


Figure 6.3: Electric field profile along the transport direction of conventional DeMOS compared with the same across various SJ devices (a) close to surface and (b) 120nm below the surface.

of SJ concept, the peak field across the SJ device is found to be lower compared to conventional device; however if the SJ doping is increased beyond a critical point, i.e. the field around SJ region continues to increase, the electric field gets crowded near the drain contact, which leads to a premature avalanche breakdown. Unlike single SJ with $X_{imp} = 0$ (double RESURF) device, the single SJ with $X_{imp} > 0$ (triple RESURF) device shows peak electric field above the SJ region. This shows that single SJ with $X_{imp} = 0$ device offers maximum reduction in peak electric field at the surface, close to gate edge; however, single SJ with $X_{imp} > 0$ device offers maximum reduction in peak electric field away from the surface, close to well junction. Moreover, the electric field away from the surface is found to be distributed in the drift region, however close to surface it is always localized close to the gate to n-well-overlap region. Among Multiple SJ-I and SJ-II, no change in the peak electric field is found, which in both the cases is higher than single SJ 2D devices.

Fig. 6.4 shows conduction current density in on-state across various devices under study. Single SJ with $X_{imp} > 0$ DeMOS tend to offer current conduction through the drift region and close to the device surface like the conventional devices. However, single SJ DeMOS device and Multiple SJ DeMOS device offers current conduction via a longer drift path attributed to presence of p-implant SJ in the surface region. This leads to a trade-off (increase) in the on-resistance when p-implant SJ is formed close to the drift region surface. Besides distributed electric field profile, the added advantage of Multiple SJ-DeMOS is that it offers surface conduction between p-implant SJ

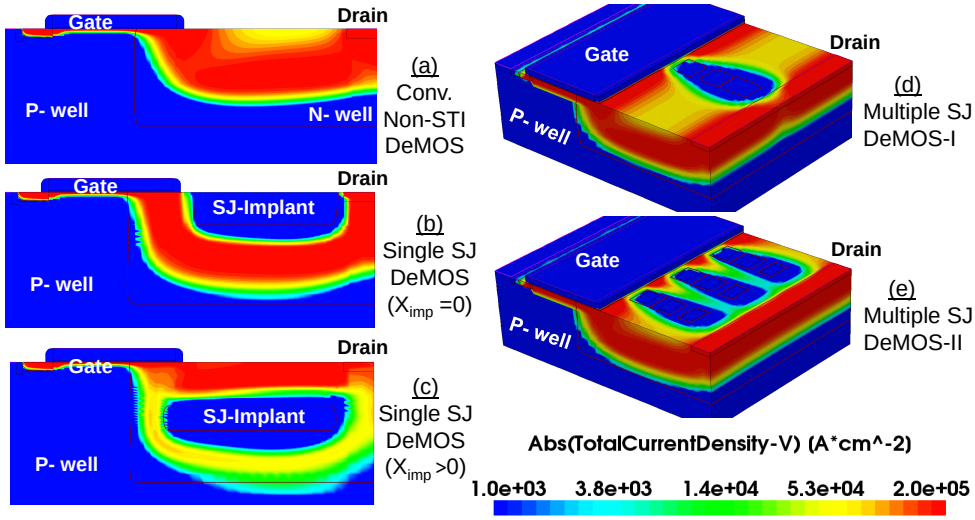


Figure 6.4: Conduction current density under on-state (a) Conventional DeMOS (b) Single SJ with $X_{imp} = 0$ DeMOS (c) Single SJ with $X_{imp} > 0$ DeMOS (d) Multiple SJ-DeMOS-I and (e) Multiple SJ-DeMOS-II.

regions. This helps in terms of mitigating R_{ON} *vs.* V_{BD} trade-off when compared to conventional device.

The additional design features relating to p-implant discussed above is expected to extend the drift region design window, which will improve the device figure of merit like R_{ON} *vs.* V_{BD}. This is depicted in Fig. 6.5 and 6.6 and discussed here. Fig. 6.5 (a) & (c) show R_{ON} *vs.* V_{BD} trade-off as a function of SJ implant doping and depth (vertical thickness) for single SJ devices. It is also seen that for a given R_{ON}, there seems to be an optimum p-implant doping level for which the breakdown voltage is higher than the rest of the doping levels. In case of lower doping, the SJ region is not effective in distributing space charge and sharing the depletion region, while at higher doping concentrations, high field around the SJ layer leads to an early avalanche breakdown around drain region, as depicted in the inset. Given that lower doping doesn't deplete the drift region, on-resistance is maintained at a lower value, however as the SJ doping increases, it reduces the effective conduction area by depleting the drift region, which increases on-resistance significantly. Similar trends are found for p-implant depth/thickness (t_{imp}), as the on-resistance trade-off is due to effectiveness of p-implant (SJ) region and a depleting drift region. Interestingly, on one hand on-resistance increases with p-implant depth/thickness, whereas breakdown voltage

for a given p-doping doesn't change in the same relation by increasing p-implant depth/thickness (t_{imp}). This allows an optimum doping and thickness combination which maximizes V_{BD}, minimizes R_{ON}, as depicted by the shaded region. Fig. 6.5(b) & (d) show that on-current (I_{ON}) falls linearly with p-implant (SJ) region doping, which can be attributed to reduced drift area due to increased depletion width at higher p-type doping. On the other hand, intrinsic gain ($g_m R_O$) of the devices doesn't change significantly. Overall, on-current and intrinsic gain of single SJ with $X_{imp} > 0$ device is found to be higher than single SJ with $X_{imp} = 0$ device, whereas R_{ON} and V_{BD} are found to be in the same range. Fig. 6.6 (a) − (d) show R_{ON} *vs.* V_{BD} and I_{ON} *vs.* $g_m R_O$ trade-off as a function of p-implant doping and depth for Multiple SJ devices. Unlike single SJ devices, Multiple SJ-I device offers relatively least variation in all the figure of merit parameters, which signifies the robustness of Multiple SJ-I design. On the other hand, when the p-implant island density is increased (Multiple SJ-II design), a trade-off between R_{ON} *vs.* V_{BD} and I_{ON} *vs.* $g_m R_O$ is found. This depicts an optimum design with maximum V_{BD}, I_{ON} and $g_m R_O$ and least R_{ON} between Multiple SJ-I and SJ-II. Overall, Multiple SJ devices offer least on-resistance compared to single SJ DeMOS devices, which is attributed to it's 3D nature, i.e. combination of conventional DeMOS and single SJ DeMOS. The shaded regions in Fig. 6.5 and 6.6 shows the optimum parameters of p-implants for all the devices which are then considered for rest of the investigations while categorizing devices into following two sets: (a) Set-1: All the devices with same R_{ON}. (b) Set-2: All the devices with same V_{BD}.

6.3 Analog/RF Performance

Beside the SOA, ESD and off-state hot carrier reliability issues, advanced DeMOS devices seriously suffer due to early quasi-saturation Shrivastava and Gossner (2012), Varghese *et al.* (2007), He and Zhang (2001), Gupta *et al.* (2015) which hinders transistor to reach it's intrinsic limits. Hence, for efficient circuit operation, especially for analog/RF and mixed signal applications, quasi-saturation effect is also worth investigating beside minimizing R_{ON} vs. V_{BD} trade-off. Quasi-saturation, which is an electrical consequence of early space charge modulation in the drift region, occurs when injected majority carrier density is higher than background doping concentration in the n-well drift region. This leads to significant mobility degradation and loss

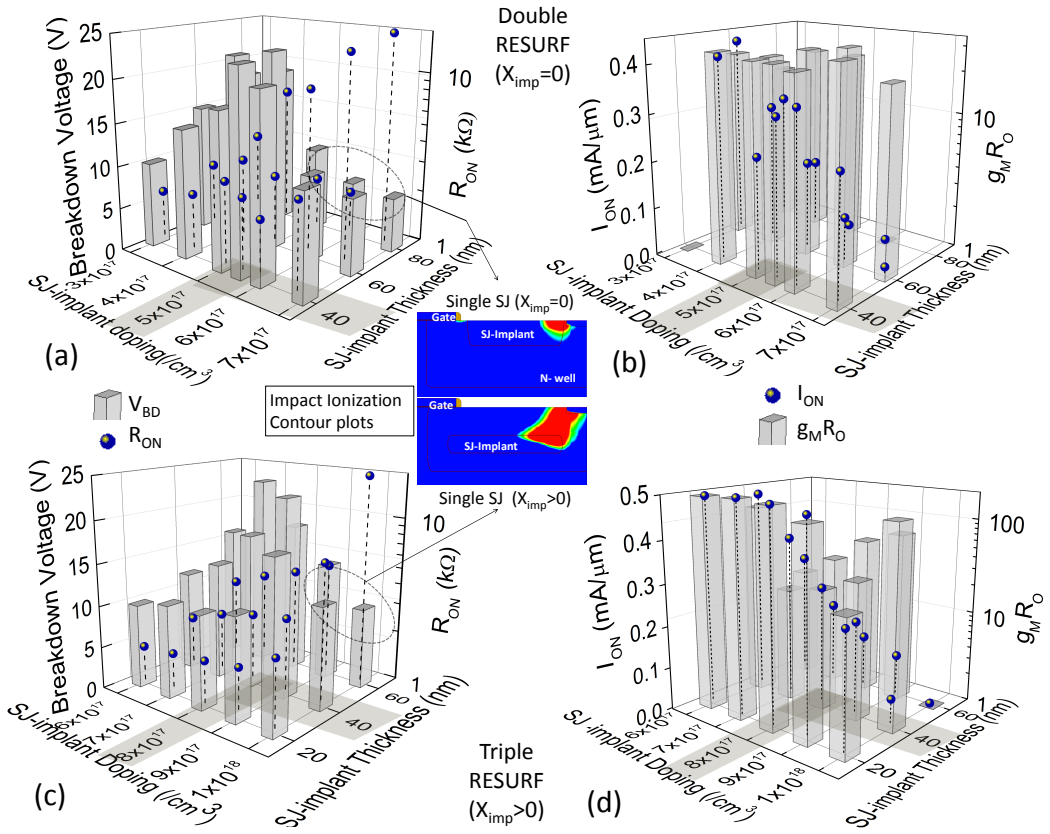


Figure 6.5: R_{ON}, V_{BD}, I_{ON}, $g_m.R_O$ vs. SJ doping and thickness for 2D SJ-DeMOS devices under study. On-state parameters are extracted at V_{GS}=1.8V and V_{DS}=6V, whereas breakdown voltage is extracted under off-state (V_{GS}=0V). (a)-(b) Single SJ with $X_{imp} = 0$ DeMOS, (c)-(d) Single SJ with $X_{imp} > 0$ DeMOS. The shaded regions depicts optimum trade-off.

of gate control over channel current modulation. This is an issue with SJ devices, due to reduced drift area available for carriers to flow, which increases the current density inside the n-well region at a given current. For Set-1 devices, it can be noted from Fig. 6.7 that single SJ DeMOS devices in Set-1 have 50% higher drift region doping compared to other designs, whereas it has 33% and 200% higher doping compared to Multiple SJ-DeMOS devices and conventional DeMOS device, respectively, in Set-2.

Fig. 6.8 (a) and (b) respectively show the devices with same R_{ON} (Set-1) and same V_{BD} (Set-2) as the conventional DeMOS device, obtained by individually tuning the N-drift doping concentration as obtained from Fig. 6.7. The figure of merit parameters evaluated in later sections is based on the physical parameters set in arriving at the R_{ON} and V_{BD} values in Fig. 6.8.

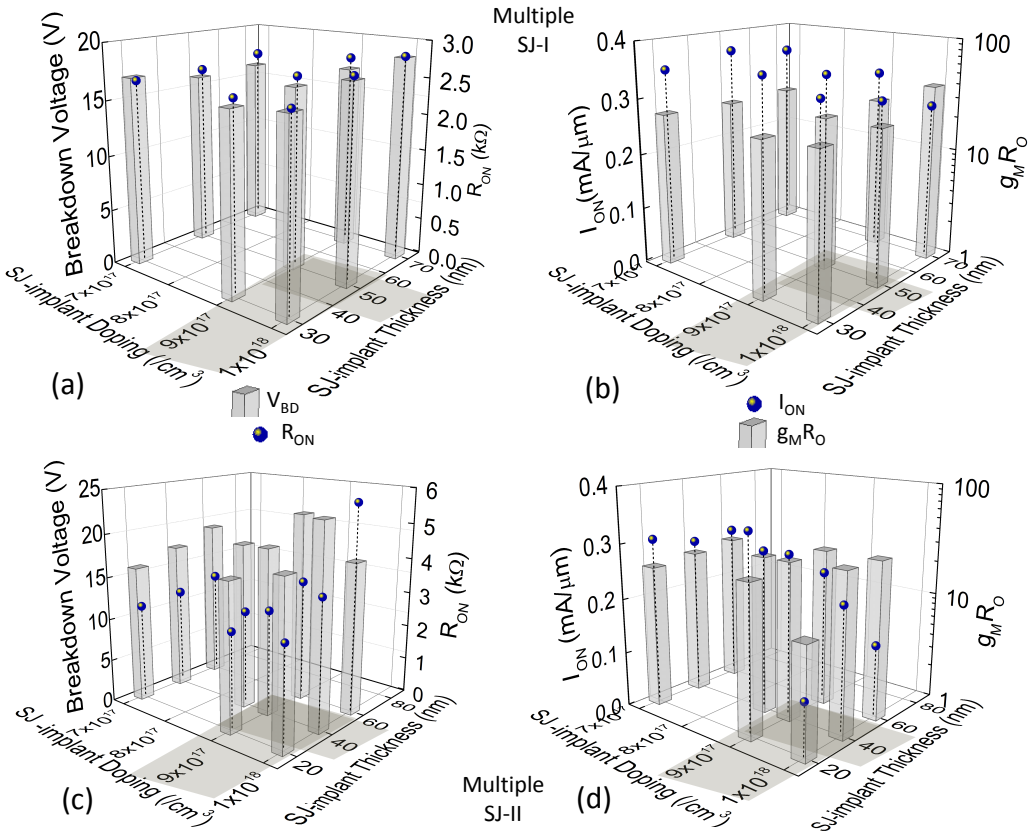


Figure 6.6: R_{ON}, V_{BD}, I_{ON}, $g_m.R_O$ vs. SJ doping and thickness for 3D SJ-DeMOS devices under study. On-state parameters are extracted at V_{GS}=1.8V and V_{DS}=6V, whereas breakdown voltage is extracted under off-state (V_{GS}=0V). (a)-(b) Multiple SJ DeMOS-I, (c)-(d) Multiple SJ DeMOS-II. The shaded regions depicts optimum trade-off.

Fig. 6.9 (a) & (b) show the transfer and output characteristics, respectively, of Set-1 devices. Similarly, transfer and output characteristics of Set-2 devices are depicted in Fig. 6.9 (c) & (d), respectively. For fixed on-resistance, single SJ with $X_{imp} = 0$ device offers significant performance improvement over single SJ with $X_{imp} > 0$ device. Single SJ with $X_{imp} = 0$ DeMOS offers 200% higher breakdown voltage at the cost of 15% reduction on on-current, when compared to conventional DeMOS device. It is worth highlighting that most of the devices suffer from quasi-saturation. Given that single SJ with $X_{imp} = 0$ DeMOS offers maximum improvement in breakdown voltage for a given on-resistance, the cost it has to pay in terms of onset of quasi-saturation at 10% lower gate voltage is not significant. Other devices don't seem to offer a better trade-off in terms of breakdown voltage and on-current for fixed on-resistance, which is due to early quasi-saturation noticed in Multiple SJ DeMOS-II and single SJ with

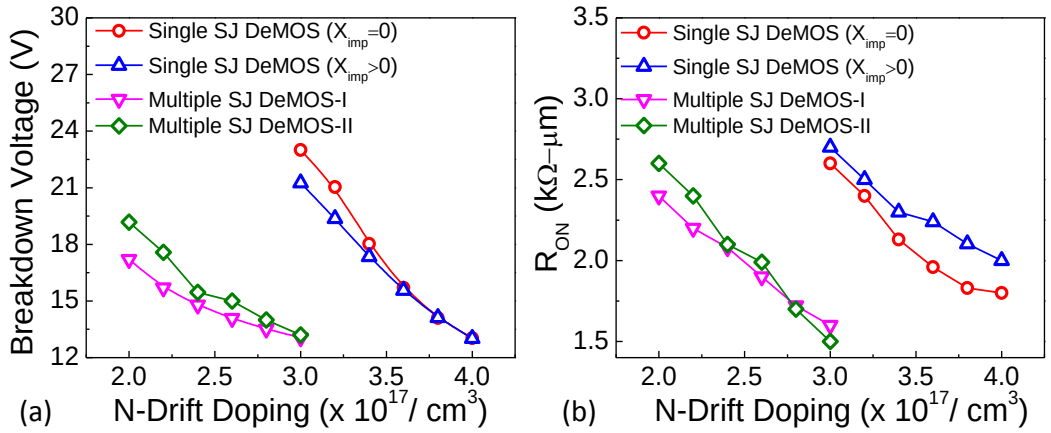


Figure 6.7: V_{BD} and R_{ON} plots as a function of n-well doping for various DeMOS devices under study. On-state parameters are extracted at V_{GS}=1.8V and V_{DS}=6V, whereas breakdown voltage was extracted under off-state (V_{GS}=0V).

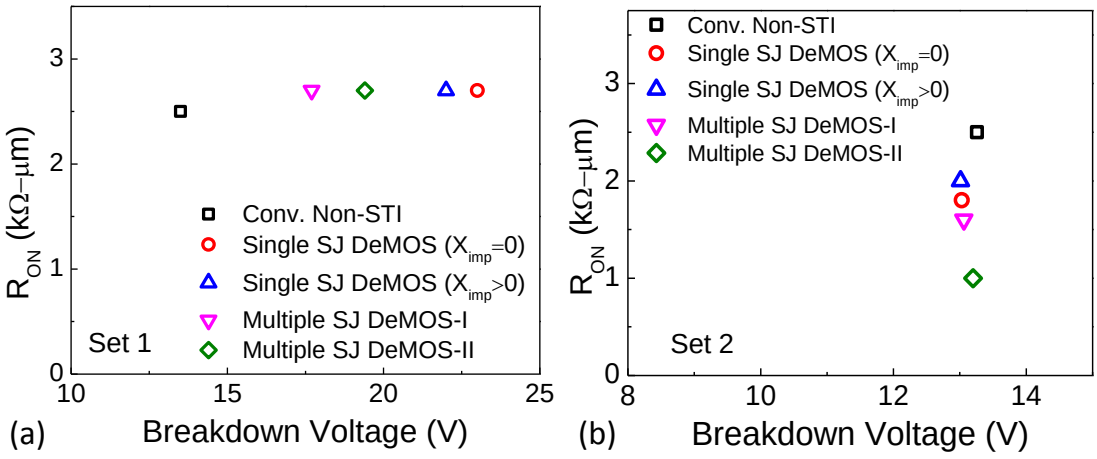


Figure 6.8: V_{BD} vs. R_{ON} trade-off of various DeMOS devices in following two sets: (a) Set-1 consists of devices with fixed on-resistance and (b) Set-2 has devices with fixed breakdown voltage. Note: All the devices compared here have same footprint.

$X_{imp} = 0$ DeMOS. For fixed breakdown voltage case, SJ designs clearly outperform the conventional design. Except single SJ with $X_{imp} > 0$ DeMOS, other designs offer 50% higher on-current when compared to conventional designs, due to delayed quasi-saturation. Multiple SJ devices have a marginal quasi-saturation at higher gate voltage, which in the case of single SJ device is completely missing. This is attributed to an increased n-well doping window for SJ devices.

Transconductance (g_m) and Miller capacitance (C_{GD}) are the key parameters to assess analog and RF capability of DeMOS devices. Fig. 6.10 (a) shows that among

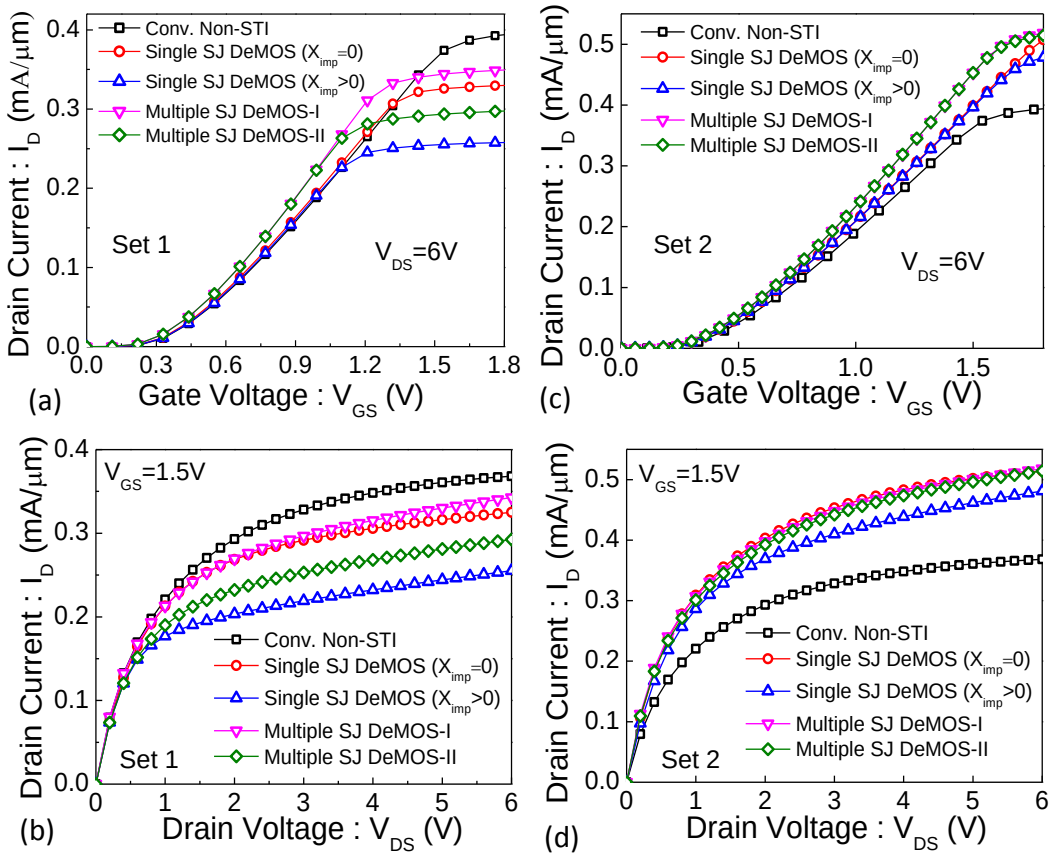


Figure 6.9: (a), (c) Simulated drain current (I_D) vs. gate voltage (V_G) characteristics and (b), (d) drain current vs. drain voltage (V_{DS}) characteristics of (a), (b) Set-1 and (c), (d) Set-2 devices. I_D-V_G characteristics are extracted at V_{DS}=6V, whereas I_D-V_D characteristics are extracted at V_G=1.8V.

Set-1 devices Multiple SJ devices offer maximum g_m, however attributed to an early quasi-saturation, the g_m falls dramatically at 33% lower gate voltage compared to conventional device. This seriously lowers the maximum gate swing allowed, which limits it's uses for large signal power RF applications. Furthermore, single SJ devices don't offer g_m improvement; whereas causes a loss of 15% in the maximum allowed gate swing due to early quasi-saturation. Fig. 6.10 (b) shows that single SJ devices of Set-1 significantly adds to non-linearity in feedback/Miller capacitance, at higher gate voltage, compared to Multiple SJ and conventional devices. This is attributed to the non-linearity in the field distribution at gate edge, at higher currents, in single SJ devices. Moreover, an interesting trend can be observed, device having lower onset of quasi-saturation has least Miller capacitance. Fig. 6.10 (c) shows that among the devices in Set-2, Multiple SJ devices offer maximum g_m, while they suffer from a lower

gate voltage swing due to relatively an early quasi-saturation compared to single SJ with $X_{imp} = 0$ DeMOS. Single SJ with $X_{imp} = 0$ DeMOS device has same g_m as compared to the conventional device and single SJ with $X_{imp} > 0$ DeMOS, however it offers maximum gate swing, which in case of conventional device and single SJ with $X_{imp} > 0$ DeMOS is the least. Therefore single SJ with $X_{imp} = 0$ DeMOS device allows maximum input voltage swing, which is a desirable parameter for power RF applications. Finally, Fig. 6.10 (d) shows that single SJ with $X_{imp} = 0$ DeMOS has highest Miller capacitance and non-linearity at higher gate voltage compared to other devices.

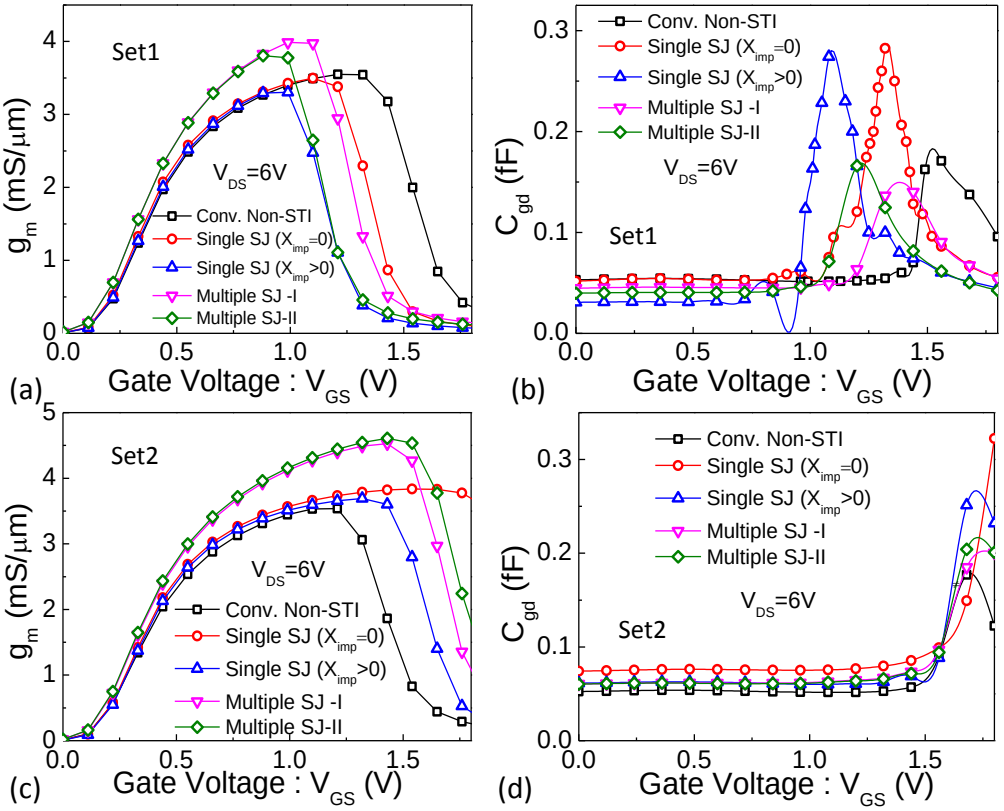


Figure 6.10: (a), (c) Transconductance (g_m) vs. gate voltage (V_G) characteristics and (b), (d) Miller capacitance (C_{GD}) vs. gate voltage (V_G) characteristics of (a), (b) Set-1 and (c), (d) Set-2 devices. Both the characteristics were extracted at V_{DS}=6V.

Fig. 6.11 shows output resistance and intrinsic transistor gain for both (a) Set-1 and (b) Set-2 devices. Fig. 6.11 (a) depicts that for fixed on-resistance single SJ with $X_{imp} > 0$ DeMOS, which has close to the maximum junction breakdown voltage in this set, offers maximum output conductance and intrinsic gain, which however falls below

the other devices as soon as quasi-saturation is triggered. On the other hand, single SJ with $X_{imp} = 0$ DeMOS with maximum breakdown voltage and conventional device with minimum breakdown voltage offer the least output conductance and intrinsic gain. Multiple SJ devices, which falls between single SJ and conventional devices, in terms of breakdown voltage, offers a moderate intrinsic gain and output conductance. These trends hint the role of drift region field engineering while designing device for maximizing transistor gain and output resistance, which however require further investigations. Fig. 6.11 (b) depicts that for fixed breakdown voltage single SJ with $X_{imp} = 0$ DeMOS offers the least output conductance and intrinsic gain, however offers maximum input swing. Other devices offers very similar R_O and $g_m R_O$ performance; however shows a roll-off as soon as quasi-saturation is triggered. Moreover, the extent of roll-off is also found to be same as strength of quasi-saturation.

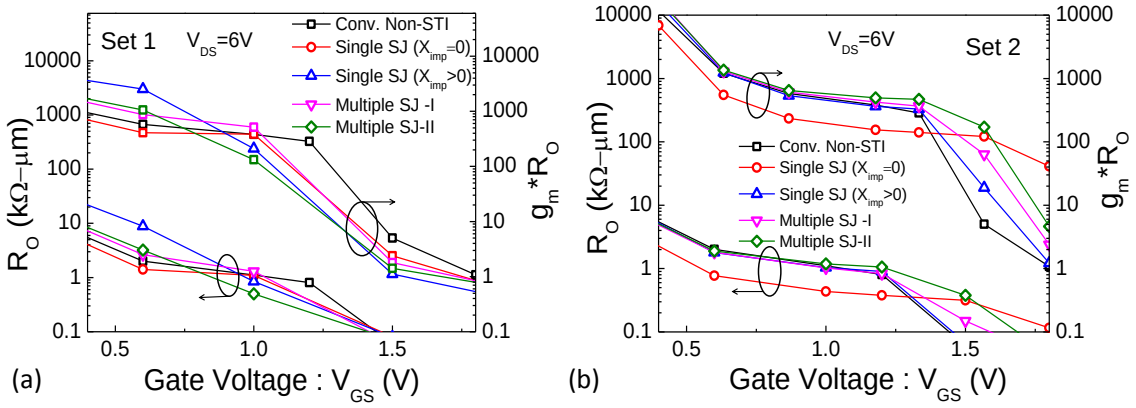


Figure 6.11: Output resistance (R_o) and intrinsic gain ($g_m R_o$) of devices in (a) Set-1 and (b) Set-2.

Fig. 6.12 shows cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) of both Set-1 and Set-2 devices. In principle this figure shows an overall manifestation of trends of Fig. 6.9 - Fig. 6.11. Fig. 6.12 (a) and (b) shows that conventional device, which suffers the least from quasi-saturation effect, offers the maximum f_t and f_{max}, even when all the devices in this set have same on-resistance. This is attributed to longer drift length of Superjunction devices and early quasi-saturation effect. On the other hand, Fig. 6.12 (c) and (d) shows that Superjunction devices outperform the conventional device when the design is for fixed breakdown voltage. Interestingly single SJ with $X_{imp} > 0$ DeMOS offers higher f_{max}, whereas single SJ with $X_{imp} = 0$ DeMOS has maximum cut-off frequency. This is attributed to lower Miller capacitance and higher intrinsic gain of single SJ with $X_{imp} > 0$ DeMOS compared to single SJ

with $X_{imp} = 0$ DeMOS.

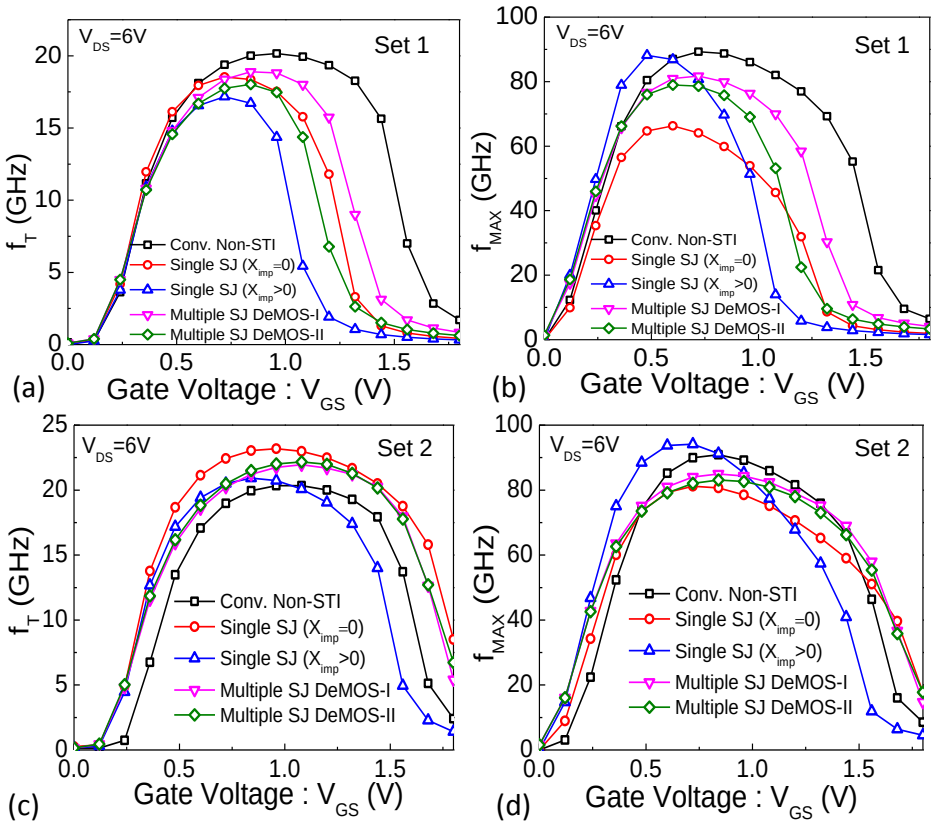


Figure 6.12: (a), (c) Transistor cut-off frequency (f_t) vs. gate voltage (V_G) characteristics and (b), (d) maximum oscillation frequency (f_{max}) vs. gate voltage (V_G) characteristics of (a), (b) Set-1 and (c), (d) Set-2 devices. Both the characteristics are extracted at V_{DS}=6V.

Table 6.1 gives a comparison of performance parameters of this work with other recently published data of sub-micron LDMOS/DeMOS devices.

6.4 HCI/ESD Reliability and SOA

Beside quasi saturation, reliability issues like off-state Hot Carrier Injection(HCI) Varghese *et al.* (2007), SOA Hower (2002) and ESD Shrivastava and Gossner (2012) are extremely critical issues and strongly depend on device design. In this section we study and compare HCI, SOA and ESD reliability behavior of various SJ DeMOS devices using 3D TCAD.

6.4.1 Hot Carrier Reliability

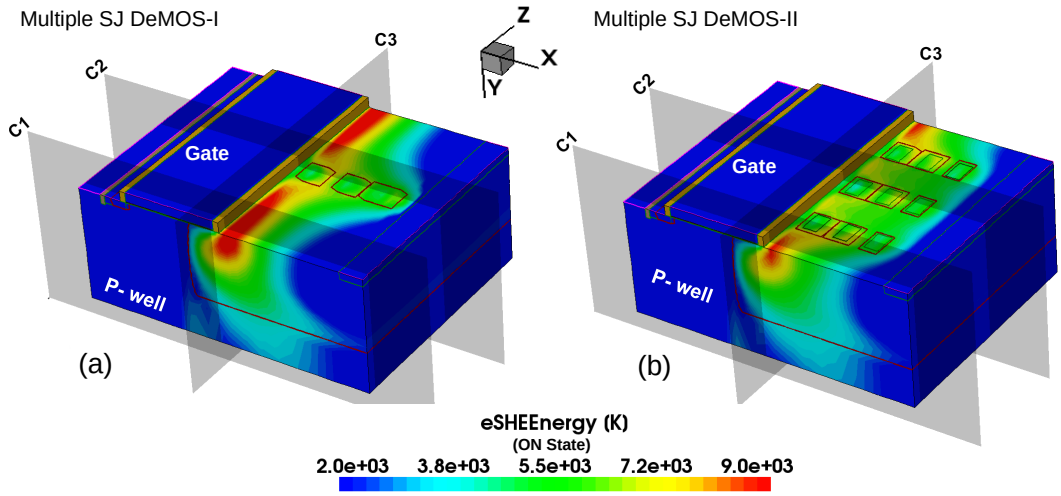


Figure 6.13: 3D contour depicting hot electron energy distribution across (a) Multiple SJ-I and (b) Multiple SJ-II devices.

HCI reliability of various DeMOS devices is studied using Spherical Harmonic Expansion (SHE) of Boltzmann transport equation, which allows extraction of hot carrier profile and hot carrier induced interface/bulk trap density and is well established method for hot carrier studies and relative comparisons Gnudi *et al.* (1992). However, it is worth highlighting that it is an indirect approach to study hot carrier behavior and is not used here for life time predictions. For on-state HCI investigations all devices are biased at a gate voltage, which offers maximum substrate current and drain voltage close to avalanche breakdown Mistry and Doyle (1995), Koike and Tatsuuma (2002). For off-state analysis, gate and source are grounded, whereas drain is biased close to junction breakdown voltage. Fig. 6.14 compares hot electron (a,c) and hot hole (b,d) profiles of various Superjunction devices from Set-1 under on- (a-b) and off- (c-d) states. Figure shows that single SJ DeMOS devices, both with $X_{imp} = 0$ and $X_{imp} > 0$ (double & triple RESURF), have considerably lower electron and hole energy, both in the on- and off-states, when compared to conventional DeMOS device. In case of Multiple SJ-I and Multiple SJ-II, carrier energy is found to be significantly lower along and around the p-implant SJ region (along C_2 in Fig. 6.13), whereas the same between two implant islands (along C_1 in Fig. 6.13) is found to be close to conventional device. Similar trends can be found from generated interface traps as depicted in Fig. 6.15 (a) and (b). Among all Superjunction devices, single SJ devices

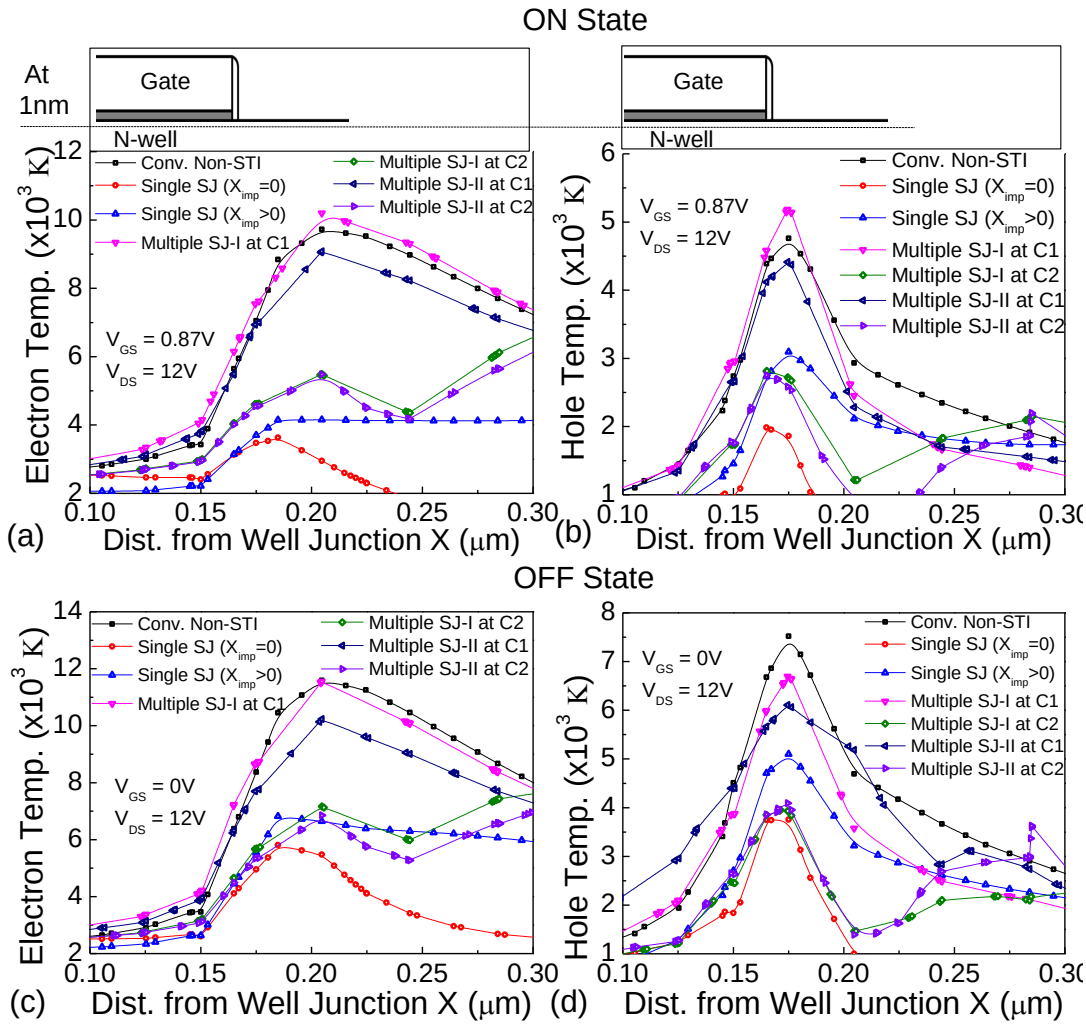


Figure 6.14: Hot carrier energy profile of various Set-1 devices, as a function of lateral distance, extracted at 1nm away from SiO_2/Si interface. (a) Hot electron and (b) hot hole profiles under on-state. (c) Hot electron and (d) hot hole profiles under off-state.

are found to be the most reliable. Among Multiple SJ-I and SJ-II, the latter having higher number of p-implant SJ islands shows lower hot carrier energy and generated interface trap density compared to the Multiple SJ-I. This is further clarified in Fig. 6.15 (c) and (d), which depicts interface trap concentration along the width of Multiple SJ DeMOS devices. Clearly the interface trap generation, both in on- and off-state is minimum in the region in and around Superjunction islands. However, the same in regions away from SJ islands approaches interface trap concentration equivalent to conventional device. This behavior is attributed to presence of depletion under the

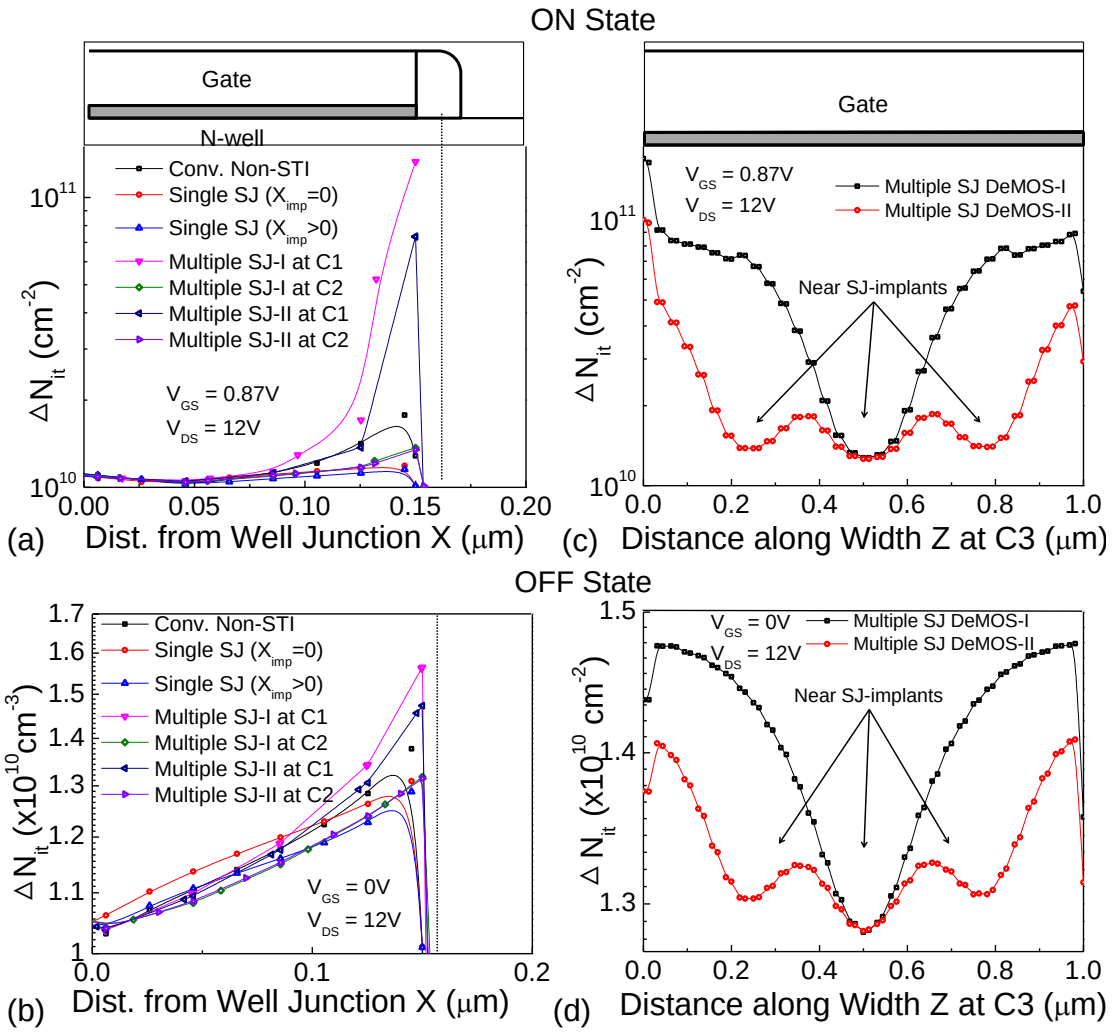


Figure 6.15: Interface trap concentration along the channel and drift length under (a) on- and (b) off-state. Interface trap concentration along the device width under (c) on- and (d) off-state.

gate edge around p-implant SJ islands, which however vanishes while moving away from these islands. Presence of wider depletion mitigates hot carrier generation. Overall, trends from Multiple SJ device indicate a need for an optimization strategy for the placement of p-islands with design parameters like island doping, depth and pitch to suppress hot carrier generation without sacrificing performance. Broadly similar trends are found for devices in Set-2 as depicted in Fig. 6.16 and Fig. 6.17. Therefore, from HCI point of view, a slower rate of degradation i.e., N_{it} being lower, would be a preferred choice for device's long term reliability.

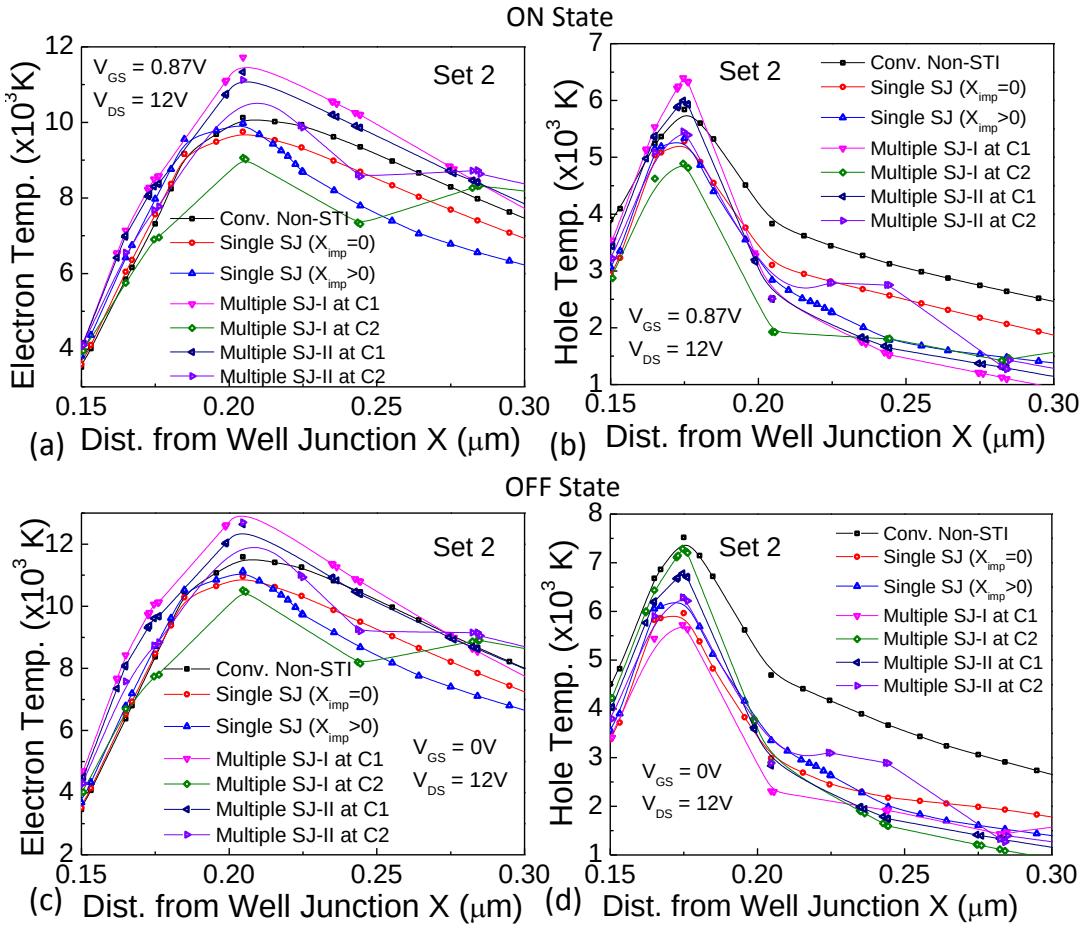


Figure 6.16: Hot carrier energy profile of various Set-2 devices, as a function of lateral distance, extracted at 1nm away from SiO_2/Si interface. (a) Hot electron and (b) hot hole profiles under on-state. (c) Hot electron and (d) hot hole profiles under off-state.

6.4.2 Safe Operating Area

Fig. 6.18 shows simulated SOA boundary of conventional and Superjunction DeMOS devices. SOA boundary represents the safe I-V margin of device under circuit operations (inset in Fig. 6.18(b)). In principle, there are three different ways in which SOA boundary is extracted, (i) thermal SOA: by stressing the device using steady state (few 10s of millisecond long) pulses, which results in purely thermal failure; (ii) electrical SOA: by stressing the device using sub-10ns long pulses, which mitigates self heating and causes devices failure purely due to electrical instabilities; and (iii) electrothermal SOA: by stressing the device using 100ns - 500ns long pulses, which accounts for both thermal and electrical aspects and causes device to fail due to electro-thermal insta-

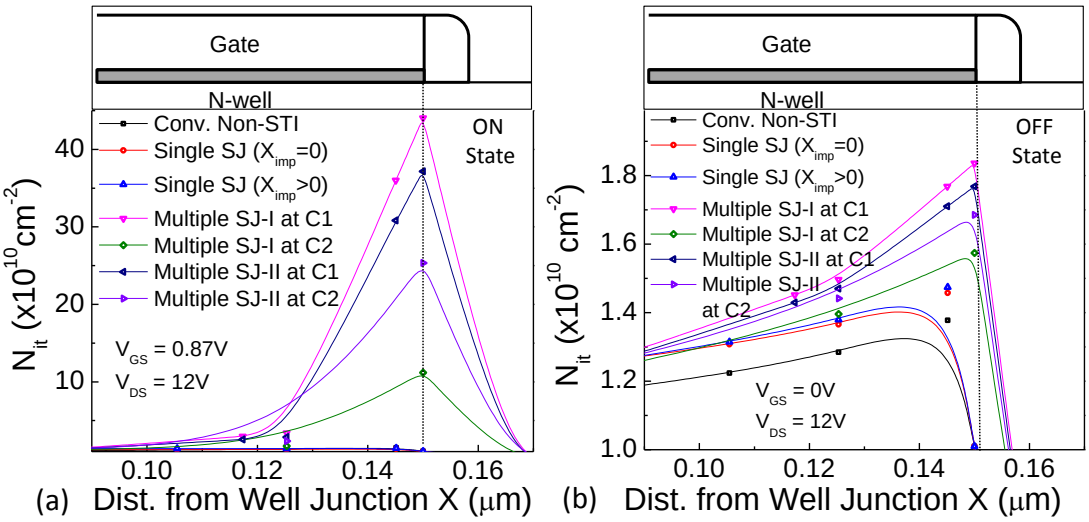


Figure 6.17: Interface trap concentration along the channel and drift length of various devices in Set-2 under (a) on- and (b) off-state.

bilities Shrivastava and Gossner (2012). From real world application point of view, in this work, electrothermal SOA is studied and compared. Fig. 6.18 shows that among Set-1 devices, with fixed on-resistance, except Multiple SJ-I, all other devices offer similar SOA boundary. Multiple SJ-I device offers relatively better SOA, albeit a marginal improvement over others. This is attributed to fixed on-resistance of the devices. It is worth highlighting that SOA boundary is defined by I-V required for filamentary failure in DeMOS devices, which is due to charge modulation and is directly related to drift region doping profile Shrivastava *et al.* (2010*a*). Fixed on-resistance designs keep the current density more or less unchanged in the drift region, which leads to unchanged SOA boundary. On the other hand, Set-2 devices having fixed breakdown voltage, show consistent improvement in SOA boundary while moving from conventional design to Multiple SJ and then single SJ implant design. In this case the conventional device with highest on-resistance for a given breakdown voltage offers an inferior SOA boundary compared to single SJ device with a least on-resistance. These trends also show that Superjunction implant based device not only improves the R_{ON} *vs.* V_{BD} trade-off, but also results in an extended SOA boundary.

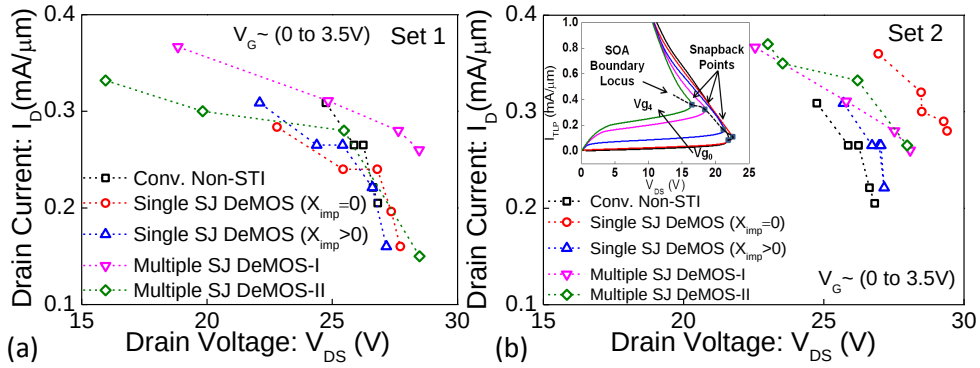


Figure 6.18: Simulated safe operating area boundary of conventional as well as various Superjunction DeMOS devices in (a) Set-1 and (b) Set-2, extracted using 3D electro-thermal TCAD based pulse I-V Simulations with 100ns pulse width.

6.4.3 ESD Reliability

ESD reliability of DeMOS devices has been studied extensively in the past Shrivastava and Gossner (2012), Shrivastava *et al.* (2009). DeMOS devices under ESD condition fail due to electrical or electro-thermal instability triggered by space charge modulation. This is often related to drift region profile, conduction current density and background doping. As soon as mobile electrons exceed the background doping, space charge modulation takes place, which forms destructive filament leading to catastrophic damage. Transmission line pulsing (TLP) is a technique used in the literature for the IV-characterization of electrostatic discharge (ESD) reliability of a device. Fig. 6.19 shows Transmission Line Pulse (TLP) I-V characteristics of (a) Set-1 and (b) Set-2 devices. Among Set-1 devices single SJ and Multiple SJ-II devices, due to restricted flow of current, leads to early failure when compared to conventional device. However, Multiple SJ-I device, due to relaxed p-implant placement, takes advantage of both the conventional design as well as Superjunction region. It gives maximum failure current (failure current per unit width) while offering higher breakdown voltage compared to the conventional design. On the other hand, among Set-2 devices, all Superjunction designs offer 10% - 20% higher failure current compared to conventional design. This is attributed to higher drift region doping allowed in Superjunction designs for a given breakdown voltage. Higher background doping shifts the onset of space charge modulation, thereby improves the failure current. Fig. 6.20 confirms that failure in all Superjunction designs, like conventional DeMOS device, is expected to be due to an early filament formation, which leads to sharp increase in lattice temperature with

respect to time and catastrophic failure.

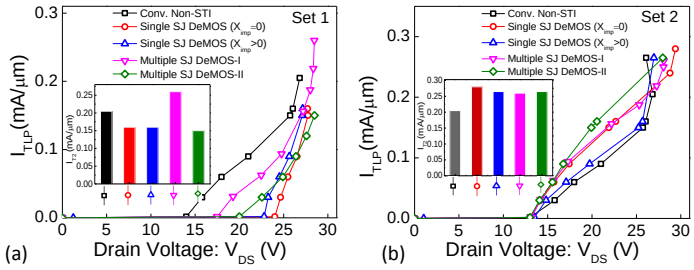


Figure 6.19: Simulated TLP characteristics of conventional and Superjunction DeMOS devices of (a) Set-1 and (b) Set-2 under study. Inset shows failure current (It2) of various devices.

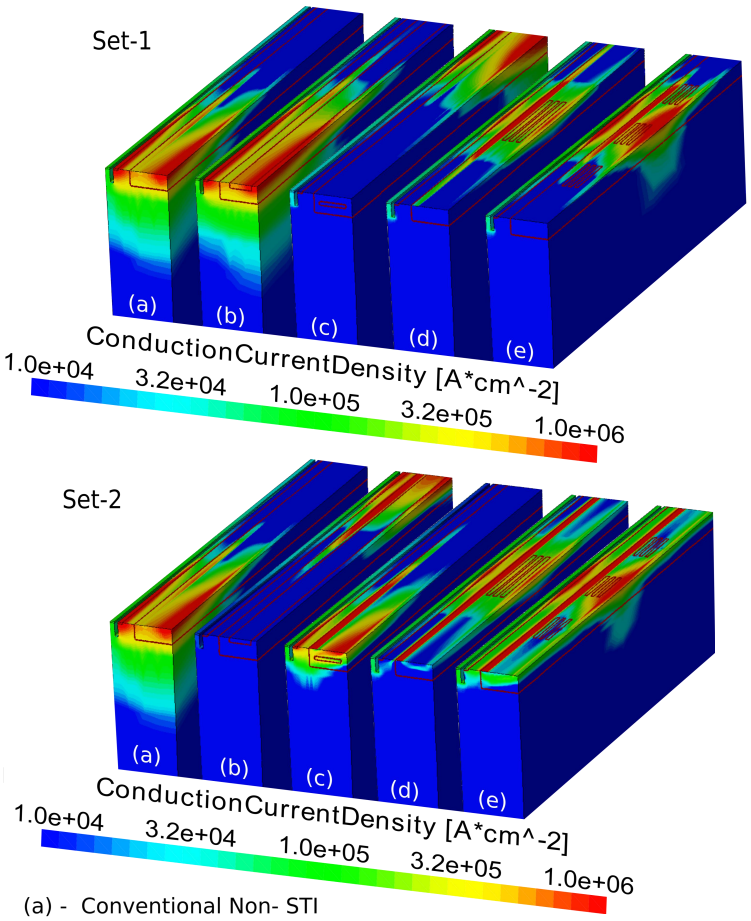


Figure 6.20: Conduction current density across various devices at current close to ESD failure point (It2), extracted using 3D TCAD simulations, for devices in Set-1 and Set-2.

Table 6.1: Comparison of different electrical parameters of the devices from this work with published data for advanced SoC Applications

Works	**Technology Platform**	I_{OFF}	t_{OX}	V_T	g_M	I_{ON} **at** V_G/V_D	R_{ONSp}	V_{BD}	f_T	f_{max}	C_{GG}
Moscatelli and Contiero and Galbiati and Raffaglio (2004)	0.18μm	<1pA/μm	-	0.65V	200mS/mm	450mA/mm at 3.3V/10V	2.8Ω-mm	15V	18GHz	-	-
Mohapatra *et al.* (2006)	0.13μm $L_G = 0.35\mu$m $L_{Drift} = 0.8\mu$m	<1pA/μm	-	0.95V	27mS/mm	380μA/μm at 3V/10V	4.7Ω-mm	27V	21GHz	-	-
Xiao *et al.* (2009)	0.18μm $L_G = 0.4\mu$m $L_{Drift} = 0.6\mu$m	-	-	0.4V	-	400μA/μm at 2V/14V	6Ω-mm	15V	18GHz	27GHz	-
T. Yan and H. Liao and Y. Z. Xiong and R. Zeng and J. Shi and R. Huang (2006)	0.18μm $L_G = 0.5\mu$m	14.5pA/μm	-	-	-	500μA/μm at 3.5V/10V	3.8Ω-mm	11.6V	18GHz	30GHz	-
Sonsky *et al.* (2008)	65nm	1.5pA/μm	-	0.82V	-	350μA/μm at 2.5V/5V	3.2m$\Omega - mm^2$	18V	30GHz	50GHz	-
Mai *et al.* (2009)	0.13μm $L_G = 0.35\mu$m $L_{Drift} = 0.6\mu$m	5pA/μm	-	0.8V	-	500μA/μm at 3.3V/15V	4.2Ω-mm	19V	25GHz	55GHz	-
Bianchi *et al.* (2009)	65nm $L_G = 0.25\mu$m	30fA/μm	3nm	-	-	400μA/μm at 1.8V/6V	3m$\Omega - mm^2$	13V	25.3GHz	-	3.04fF/μm
Shrivastava *et al.* (2010*a*)	$L_G = 0.42\mu$m $L_{Drift} = 0.48\mu$m	1nA/μm	-	0.3V	3.2mS/μm	590μA/μm at 1.8V/8V	5.5$\Omega - mm$	23V	-	-	13fF/μm
Gupta *et al.* (2015)	$L_G = 0.42\mu$m $L_{Drift} = 0.48\mu$m	1nA/μm	-	-	-	350μA/μm at 2V/5V	6$\Omega - mm$	≈18V	19GHz	50GHz	26pF/μm
This work Conventional device	**65nm** $L_G = 0.25\mu$**m** $L_{Drift} = 0.7\mu$**m**	**10pA/μm**	**5nm**	**0.4V**	**3.5mS/μm**	**400μA/μm at 1.8V/6V**	**2.5**$m\Omega - mm^2$	**13V**	**20GHz**	**85GHz**	**2.7fF/μm**
This work Single SJ with $X_{imp} = 0$ DeMOS	**65nm** $L_G = 0.25\mu$**m** $L_{Drift} = 0.7\mu$**m**	**10pA/μm**	**5nm**	**0.4V**	**3.46mS/μm**	**330μA/μm at 1.8V/6V**	**2.4**$m\Omega - mm^2$	**23V**	**19GHz**	**72GHz**	**2.7fF/μm**
This work Single SJ with $X_{imp} > 0$ DeMOS	**65nm** $L_G = 0.25\mu$**m** $L_{Drift} = 0.7\mu$**m**	**10pA/μm**	**5nm**	**0.4V**	**3.3mS/μm**	**262μA/μm at 1.8V/6V**	**2.7**$m\Omega - mm^2$	**21V**	**17.7GHz**	**89GHz**	**2.5fF/μm**
This work Multiple RESURF-I	**65nm** $L_G = 0.25\mu$**m** $L_{Drift} = 0.7\mu$**m**	**10pA/μm**	**5nm**	**0.42V**	**3.76mS/μm**	**354μA/μm at 1.8V/6V**	**2.6**$m\Omega - mm^2$	**17V**	**18.7GHz**	**80GHz**	**2.4fF/μm**
This work Multiple RESURF-II	**65nm** $L_G = 0.25\mu$**m** $L_{Drift} = 0.7\mu$**m**	**10pA/μm**	**5nm**	**0.42V**	**3.82mS/μm**	**306μA/μm at 1.8V/6V**	**2.7**$m\Omega - mm^2$	**19V**	**17.7GHz**	**79GHz**	**2.3fF/μm**

Chapter 7

Drain Extended FinFETs

Due to rapid technology scaling and its implications, the planar bulk MOS devices are being replaced by FinFETs (tri-gate device) as these have become more popular below 20-nm gate lengths. Moreover, FinFET-like devices are found to be the best suited option for system-on-a-chip (SoC) applications, which is indeed reported as the key requirement to reduce cost, size, and power while enjoying a better performance in the technologies below the 20-nm node Chen *et al.* (2017), Singh *et al.* (2014), Miyashita *et al.* (2015). Jan *et al.* (2009) and Jan *et al.* (2012) highlight the design specifications for sub-micron high voltage I/O devices, Huang *et al.* (2007) Matsudai *et al.* (2010) Mohapatra *et al.* (2006) and Toulon *et al.* (2011) discuss the design aspects of technology below 0.13μm and 0.18μm, and specify the operating voltage in the range 0.8-1.2V as low voltage and 3.3-5V as high voltage Shrivastava *et al.* (2012). Due to the availability of cost-efficient planar CMOS devices in various voltage classes, SoC implementation is not an impossible goal. However, the same is not true for FinFET technology, due to implementation challenges of HV devices.

7.0.4 SOI DeFinFETs

The conventional drain extension results in lowered breakdown characteristics since there is only single lateral junction in channel-drift region. One of the common technologies that is used in the FinFET devices is Silion On Insulator (SOI). The structure in Fig. 7.1 shows the schematic of SOI DeFinFET device. The device sustains high voltage upto 5-7V (Fig. 7.2). But this also leads to degradation of R_{ON}. The reason being that electron velocity saturates in the drain extended region before reaching

Table 7.1: Dimentional specification of the DeFinFET structures

Dimension parameter	Values nm
t_{OX}	1nm
L_{Fin}	75nm
$L_{Fin-Drift}$	160nm
W_{Fin}	15nm
X_{Fin}	60nm
X_{BOX}	300nm

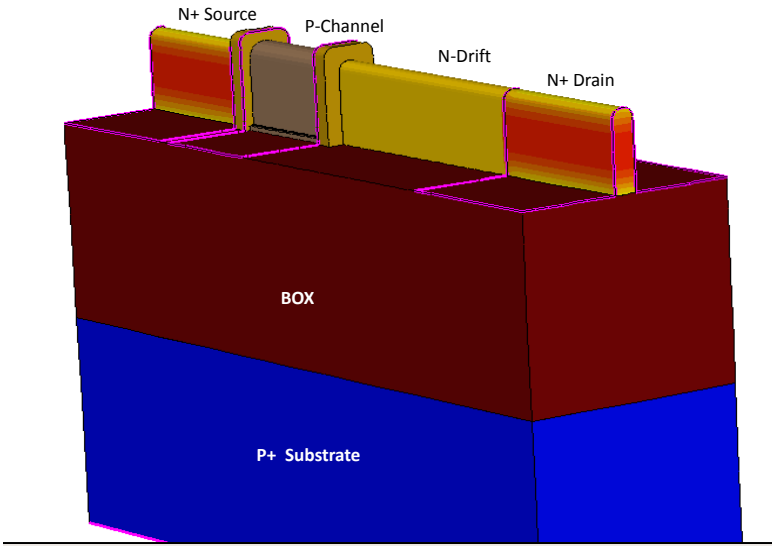


Figure 7.1: Schematics of SOI based DeFinFET

the drain terminal. This can be observed in the I-V characteristics (Fig. 7.3(a)) and transconductance g_m plots (Fig. 7.3(b)). The current saturates beyond a gate voltage of 0.75V.

7.0.5 P-stop implant in DeFinFETs

The structure in Fig. 7.4 shows the schematic of a p-stop implanted DeFinFET device. It can be observed that there are no vertical junctions in the SOI DeFinFETs. This restricts the V_{BD}-R_{ON} ratio improvements when compared with SJ DeMOS devices. To improve the breakdown characteristics, the device structure needs to be altered.

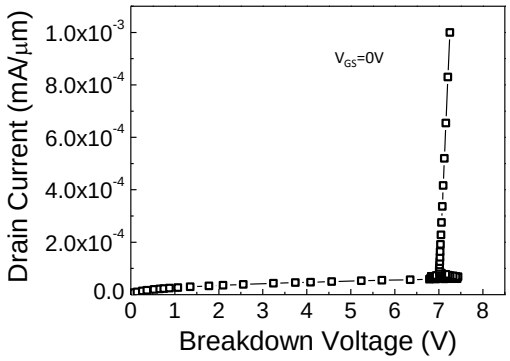


Figure 7.2: Breakdown characteristics of an SOI DeFinFET simulated at V_{GS}=0V.

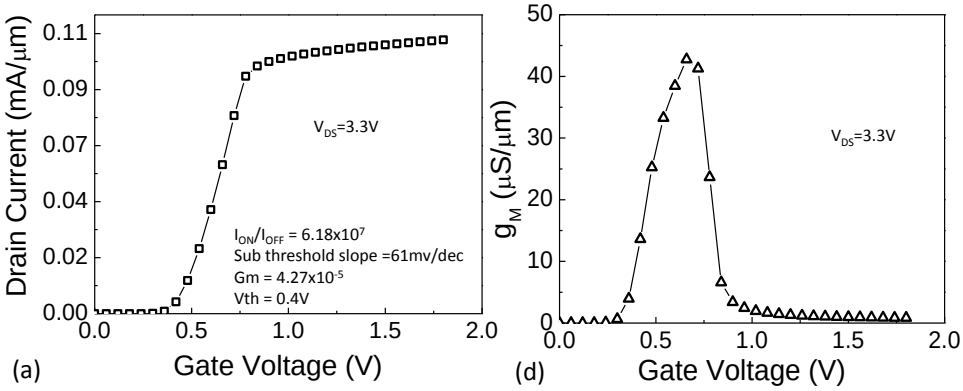


Figure 7.3: DC characteristics of SOI DeFinFET (a) I_D -V_G simulated at V_{DS}=3.3V (b) Transconductance characteristics vs. gate voltage at V_{DS}=3.3V

Instead of SOI based structure, the device structure is modified by introducing the vertical junction underneath the drift region. By implanting a p-region, below the fin-channel and extending upto fin-drift region, a vertical junction is created. This leads to termination of field lines with the drift-p region vertically.

The implanted p-region serves two purposes. Firstly, the underneath the p-region acts as an effective p-stop implant. This reduces source-drain interaction which in effect increases the immunity towards short-channel effects. Secondly, since the vertical junction is present right below the drift region, an improvement in the breakdown characteristics will be observed. The breakdown voltage range increases to 8-9V from 6-7V (SOI device case) (Fig. 7.5). As expected, the breakdown characteristics are dependent on the p-stop doping. Increase in the p-stop doping concentration increases the breakdown voltage (Fig. 7.7). DC characteristics of the device are shown in Fig.

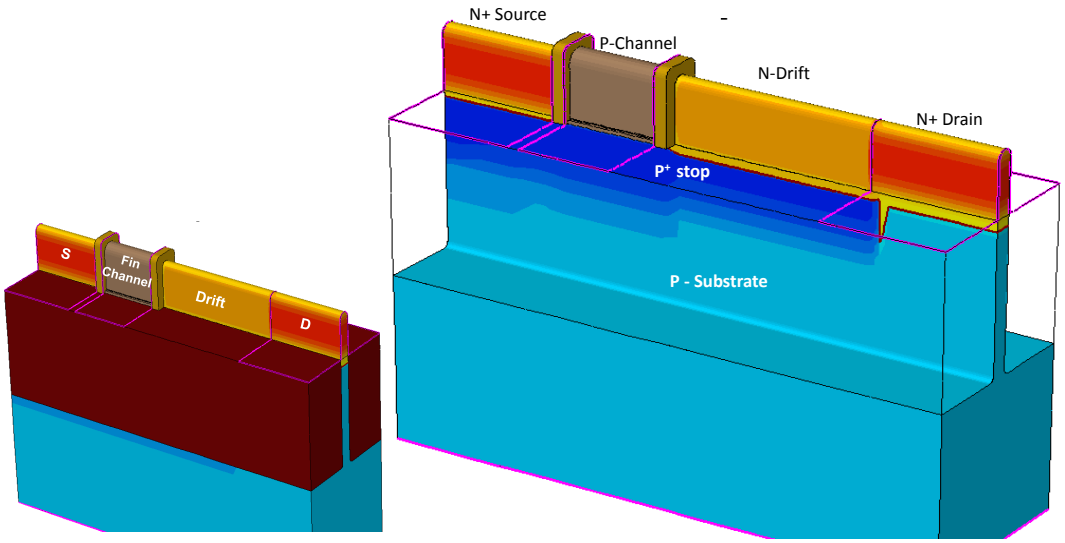


Figure 7.4: Schematics of p-stop implanted DeFinFET.

7.6(a)-(b)).

7.0.6 Well doped DeFinFETs

One of the major issues with the SOI based and p-stop based structures is that these devices undergo quasi-saturation resulting in degraded R_{ON}. This can be observed from the individual I-V characteristics in Fig. 7.3 and 7.6. Even though the breakdown characteristics are good enough to sustain high voltages, the device looses its on-state performance due to quasi-saturation mode operation. So, one of the ways to eliminate

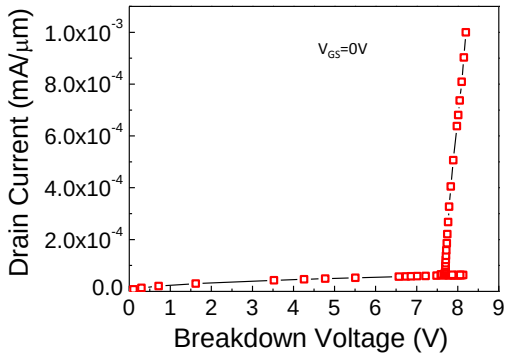


Figure 7.5: Breakdown characteristics of the p-stop implanted DeFinFET simulated at V_{GS}=0V.

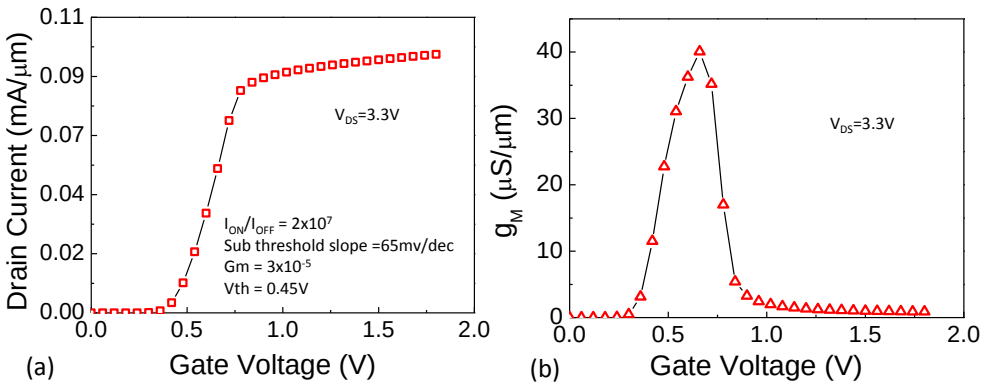


Figure 7.6: DC characteristics of p-stop implanted DeFinFET (a) I_D -V_G simulated at V_{DS}=3.3V (b) Transconductance characteristics vs. gate voltage at V_{DS}=3.3V

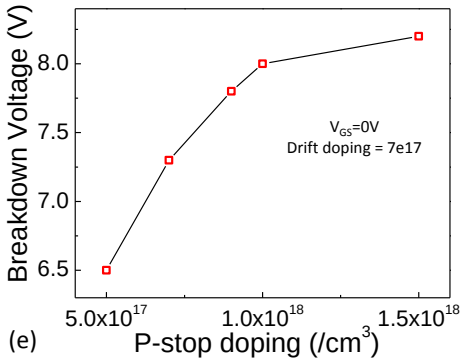


Figure 7.7: Variation of breakdown characteristics as a function of p-stop doping. Breakdown characteristics simulated at V_{GS}=0V

the quasi-saturation is to delay the onset of quasi-saturation mode.

This is possible if the doping concentration of the substrate well is increased. The structure in Fig. 7.8 shows the schematic of a well doped DeFinFET device. By doping the well with n-type, the majority carriers will have larger area for conduction in addition to fin-drift region. Further, since the total current density depends on large n-type region, the device R_{ON} decreases to very low value. As a matter of fact, the on-current increases to higher value signaling the delay in the onset of quasi-saturation even beyond 0.6V V_{GS} (Fig. 7.10(a)). Also as an effect, transconductance (g_m) roll-off is delayed (Fig. 7.10(b)). But inherently, it is observed that the breakdown voltage is reduced below 6V, and does not meet the expected design requirements (see Fig. 7.11).

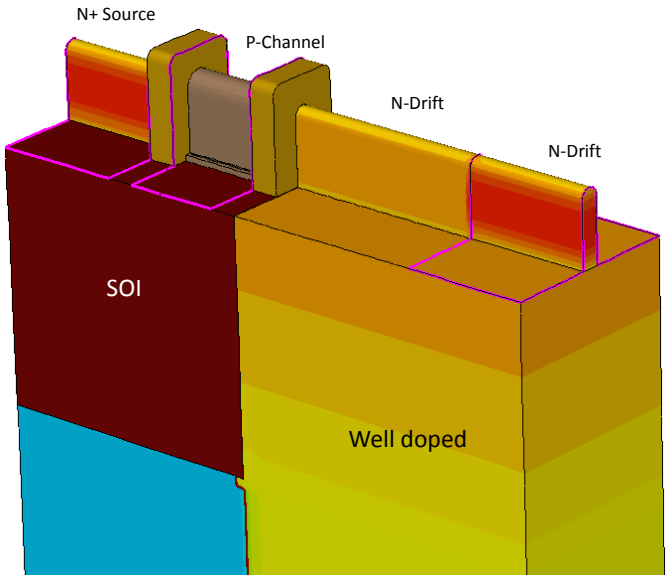


Figure 7.8: Schematics of well doped implanted DeFinFET.

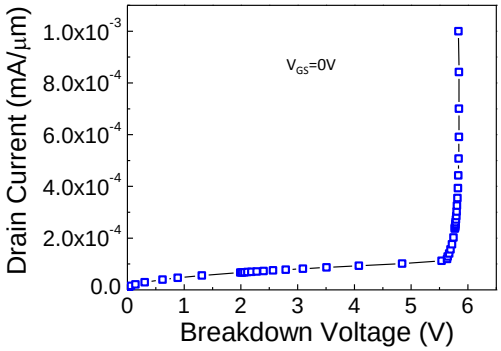


Figure 7.9: Breakdown characteristics of the well doped DeFinFET simulated at V_{GS}=0V.

7.0.7 Well doped P-implanted DeFinFETs

In an effort to improve the device performance by eliminating the quasi-saturation mode, the breakdown characteristics are severely degraded. To restore the device breakdown characteristics to the conventional SOI based DeFinFET, a vertical p-n junction in the fin-drift region is introduced using a p-implant as shown in Fig. 7.12. By a proper choice of doping concentration and the hight of the p-implant, it is possible to enhance the breakdown characteristics without adversely affecting the quasi-saturation mode. With this modification, the breakdown characteristics are seen

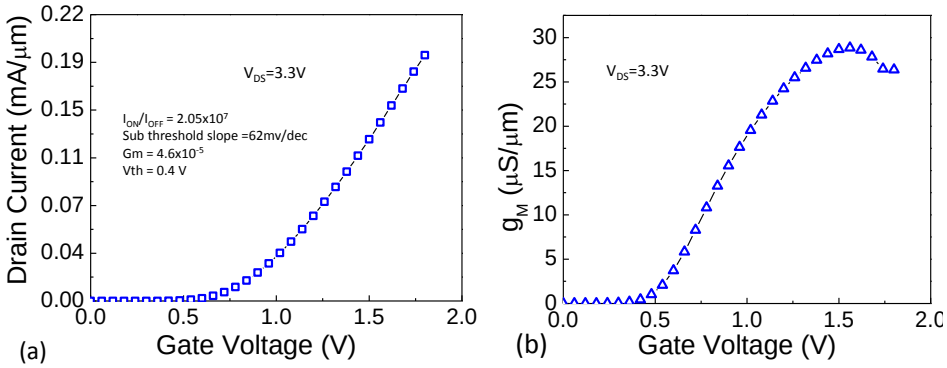


Figure 7.10: DC characteristics of well doped DeFinFET (a) I_D -V_G simulated at V_{DS}=3.3V (b) Transconductance characteristics vs gate voltage at V_{DS}=3.3V

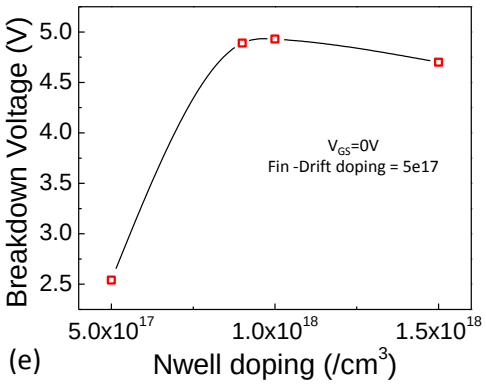


Figure 7.11: Variation of breakdown characteristics as a function of well doping. Breakdown characteristics simulated at V_{GS}=0V

to improve to 7-9V (Fig. 7.13) without altering the device performance metrics. In effect, the device breakdown voltage improves with p-implant doping, but without undergoing any quasi-saturation effect.

7.1 Analog performance of FinFET devices

In this section, we discuss the DC characteristics and analog performance metrics of the four FinFET structures described above. The devices are simulated for a gate voltage (V_{GS}) sweep of 0 to 1.8V keeping the drain voltage (V_{DS}) at 3.3V. With the device dimensions in table 7.1 above, Fig. 7.15 shows the I_D-V_G and I_D-V_D characteristics of these devices. Threshold voltage V_T is observed to be higher for well doped devices, and I_{OFF} is observed to be in pico-ampere (pA) region for all the

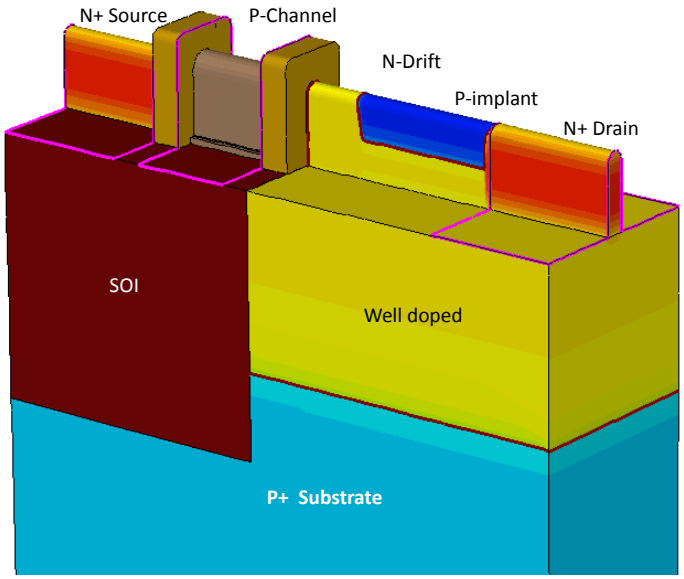


Figure 7.12: Schematics of well doped p-implanted DeFinFET.

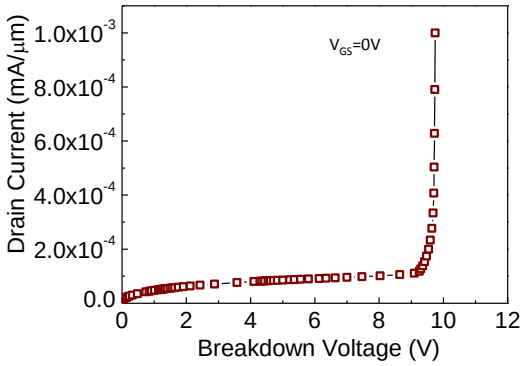


Figure 7.13: Breakdown characteristics of the well doped p-implanted DeFinFET simulated at V_{GS}=0V.

devices (Fig. 7.15).

7.1.1 Transconductance - g_m

The analog performance factors such as transconductance (g_m) and gate-to-drain capacitance (C_{GD}) are as much important as the breakdown characteristics. Thinner t_{OX} always improves the transconductance. On the contrary, thicker oxide will yield an increased threshold voltage but also helps to improve the breakdown voltage in the gate-overlap region. Transconductance depends linearly on maximum gate overdrive.

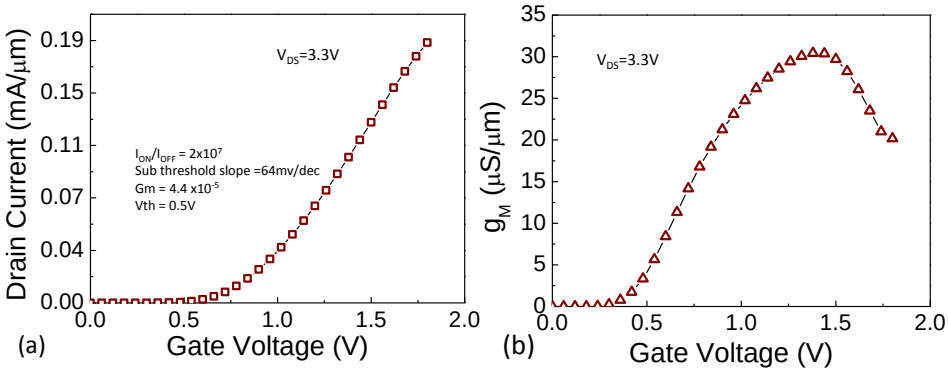
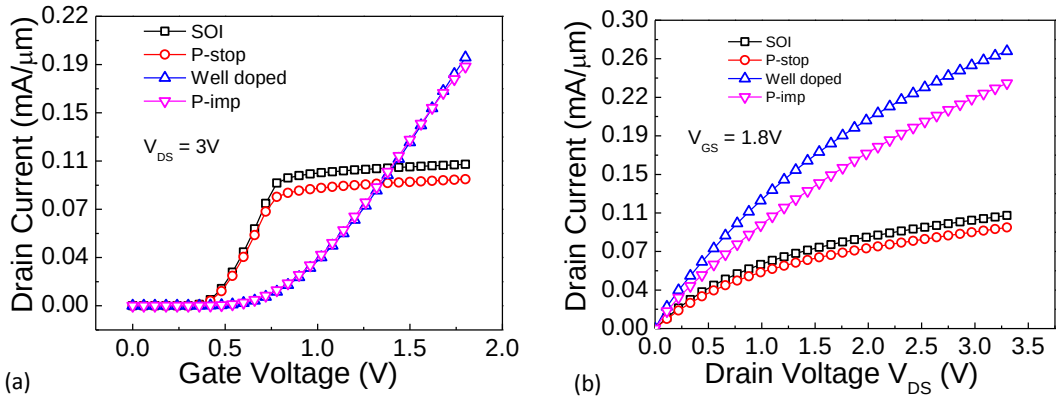


Figure 7.14: DC characteristics of well doped p-implanted DeFinFET (a) I_D -V_G simulated at V_{DS}=3.3V (b) Transconductance characteristics vs gate voltage at V_{DS}=3.3V



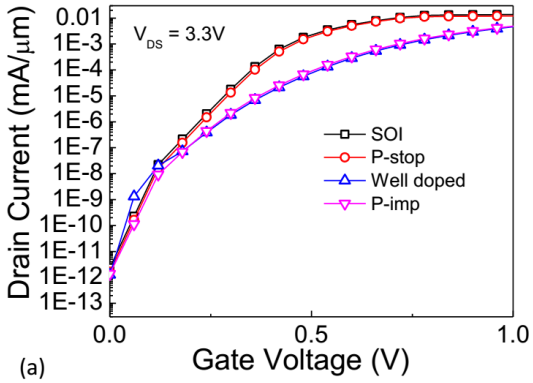


Figure 7.15: DC Characteristics (a)I_D -V_G simulated at V_{DS}=3.3V (b) I_D -V_D simulated at V_{GS}=1.8V and (c) Subthreshold characteristics of all the four devices

Fig. 7.16 shows the g_m-V_{GS} graph at a maximum drain voltage of 3.3V (EOT=1nm). It can be seen that the well doped devices show better current characteristics than SOI

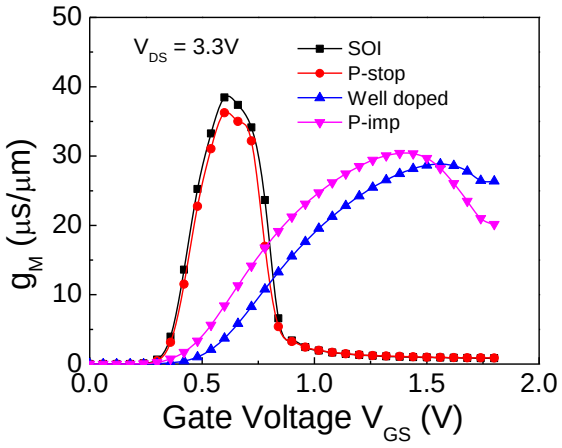


Figure 7.16: Plot of g_m vs. V_{GS} simulated for V_{DS}=3.3V for all the four devices

and p-stop devices. The well doped devices extend the onset of quasi-saturation characteristics (Fig. 7.15). This is also verified by the transconductance characteristics in Fig. 7.16. The g_m is seen to be rolling off rapidly at the early stages (V_{GS} ≈0.6V) for SOI and p-stop devices as the devices enter into quasi-saturation.

7.1.2 Capacitance C_{GG} and C_{GD}

In this section, we discuss the gate capacitance (C_{GG}: total gate capacitance) and drain capacitance (C_{GD}: gate to drain capacitance) of the device.

1) Gate Capacitance: Fig. 7.17(a) shows the total gate capacitance as a function of gate voltage for V_{DS}=3.3V. For $V_{GS} > 0$V, the gate capacitance increases due to increase in carrier flow, as expected. Also, C_{GD} starts increasing due to increased coupling of drain-gate terminals beyond 1.5V V_{GS} (Fig 7.17(b). It can be seen that C_{GG} is slightly higher for SOI and p-stop devices, whereas the C_{GD} and C_{DD} capacitances are higher for well doped devices since the well doped devices have larger n-doped regions (in terms of area including the n-doped regions below drift region). The feedback capacitance C_{GD} is the parameter which plays an important role in determining large signal performance and linearity (bias dependency) of the device. Fig.7.17(b) shows the gate to drain capacitance C_{GD} for on-state.

2) Off-state Drain Capacitance: At V_{DS}=0V C_{GD} has many intrinsic capacitive components which include gate-drain overlap capacitance in series with depletion capacitance and gate-drain coupling capacitance. As the drain potential is increased from 0V, the coupling between the drain and the gate is reduced. Decrease in this

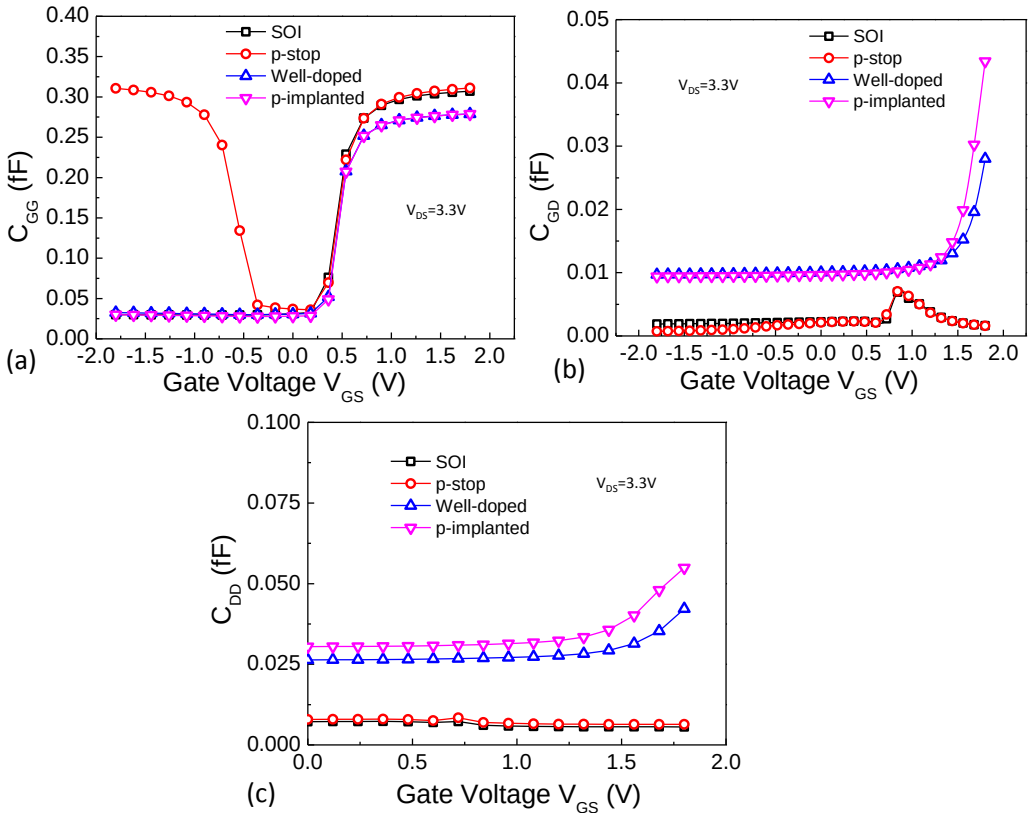


Figure 7.17: Gate and drain capacitances vs. gate voltage V_{GS} taken at V_{DS}=3.3V (a) Total gate capacitance (b) Miller capacitance (c) Total drain capacitance of all the four devices

component of the capacitance reduces the overall capacitance as the drain voltage is increased. Fig.7.18 shows the gate-drain capacitance as a function of V_{GS}.

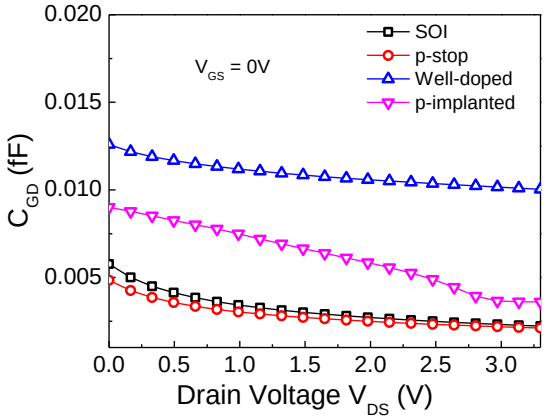


Figure 7.18: (b) Miller capacitance vs. V_{GS} taken at V_{DS}=0V.

7.1.3 Gain, f_T, f_{max}

Fig. 7.19 shows the intrinsic gain $g_m r_O$ for all the devices. For larger values of gate-overdrive there is a degradation in the transconductance and output resistance, hence $g_m r_O$ is reduced significantly. Since the g_m falls abruptly beyond 0.65V, it can be observed that there is an abrupt transition in the intrinsic gain for SOI and p-stop devices when compared to the well doped devices.

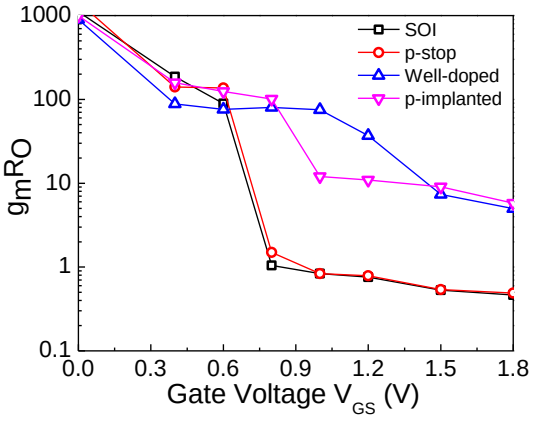


Figure 7.19: Intrinsic gain ($g_m r_O$) as a function of V_{GS}

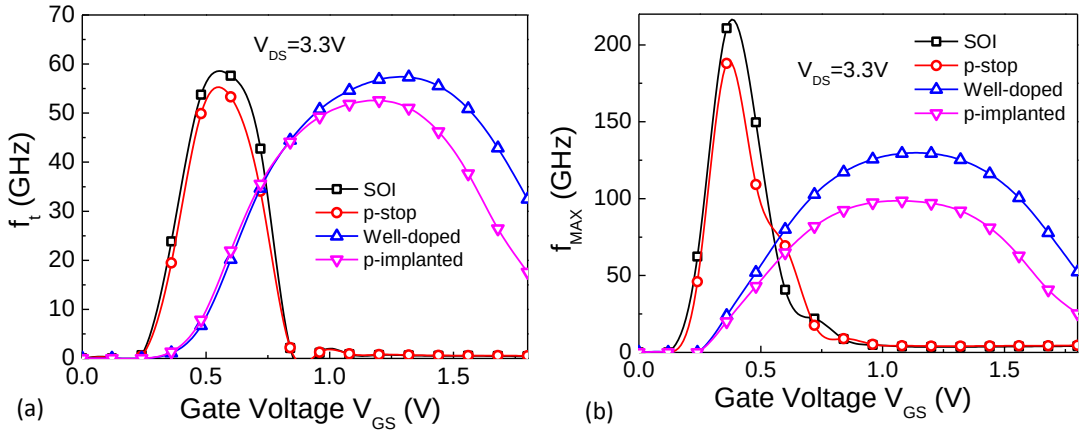


Figure 7.20: Frequency parameters (a) f_T and (b) f_{max} vs. V_{GS}

f_T and f_{max} parameters define the RF performance of the devices. The cut-off frequency f_T is the frequency when the current gain is unity, which is extracted by extrapolating the current gain $|h_{21}|$. Fig. 7.20(a) shows f_T as a function of V_{GS} for a fixed drain voltage of 3.3V. f_{max} is the maximum oscillation frequency at unity

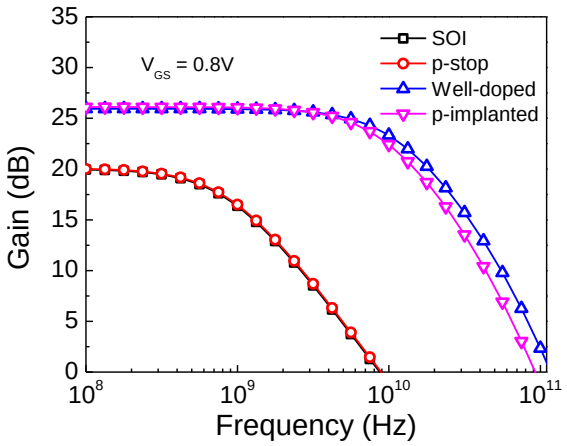


Figure 7.21: Maximum unilateral gain as a function of frequency

power gain obtained by extrapolating Maximum Unilateral Gain (MUG). Fig. 7.20(b) shows f_{max} for a fixed drain bias of 3.3V. f_T depends on the transconductance and fin drift-length of the device. Since the fin-length is constant for all the devices and also the gate capacitance does not show much variation, f_T depends only on g_m. f_{max} is the frequency that gives the intrinsic switching speed which depends on high output resistance and input resistance. Maximum unilateral gain (MUG) is shown in Fig. 7.21. The gain starts falling after 1GHz. As shown in the graph, the unilateral gain is higher for the well doped devices.

7.2 Reliability - Hot Carrier Injection Study

Hot carrier behavior is one of the major measures of degradation mechanism. Hence it is important to discuss these aspects for long term reliability. The highly energized carriers create interface states by breaking the Si-H bonds (Hot carrier injection) at the interface of $Si - SiO_2$. Hot carrier distribution is extracted using Spherical Harmonics Expansion (SHE) method. SHE method solves the microscopic carrier energy distribution function expanding the Boltzmann transport equation into spherical harmonics. Fig. 7.22 and 7.23 show the hot electron and hot hole (SHE) energy profiles for on- and off-states. The profiles are extracted after transient simulation for $V_D = 6V$ $V_{GS} = 0.65V$. It is seen that the energy of hot holes is higher in well doped devices as carrier flow and the current distribution is higher in well doped devices.

To understand the SHE energy profiles, the interface trap concentration is mea-

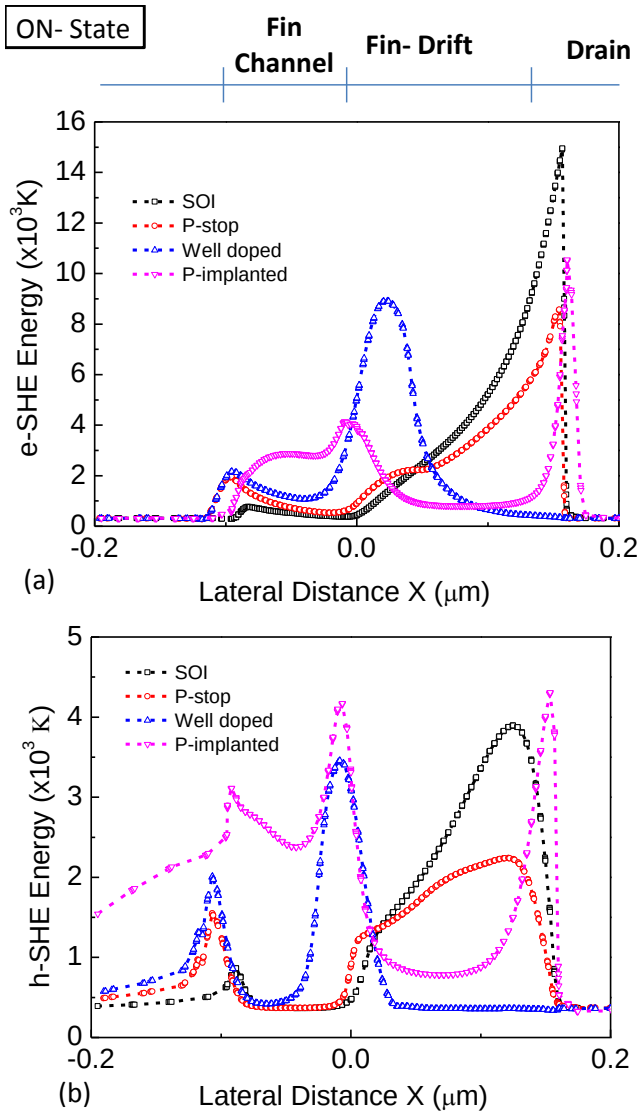


Figure 7.22: Hot carrier energy profiles taken along the lateral distance for on-states (a) electron SHE energy (b) hole SHE energy

sured along the X-axis. The effect of higher field as seen by the SHE energy profiles manifests as higher carrier energy and it is a function of n-well doping. This high field energizes more carriers which in turn manifests as hot electrons and hot holes. The result of hot electrons and hot holes is the increased interface trap concentration, whose location coincides with the SHE energy profile (Fig. 7.24).

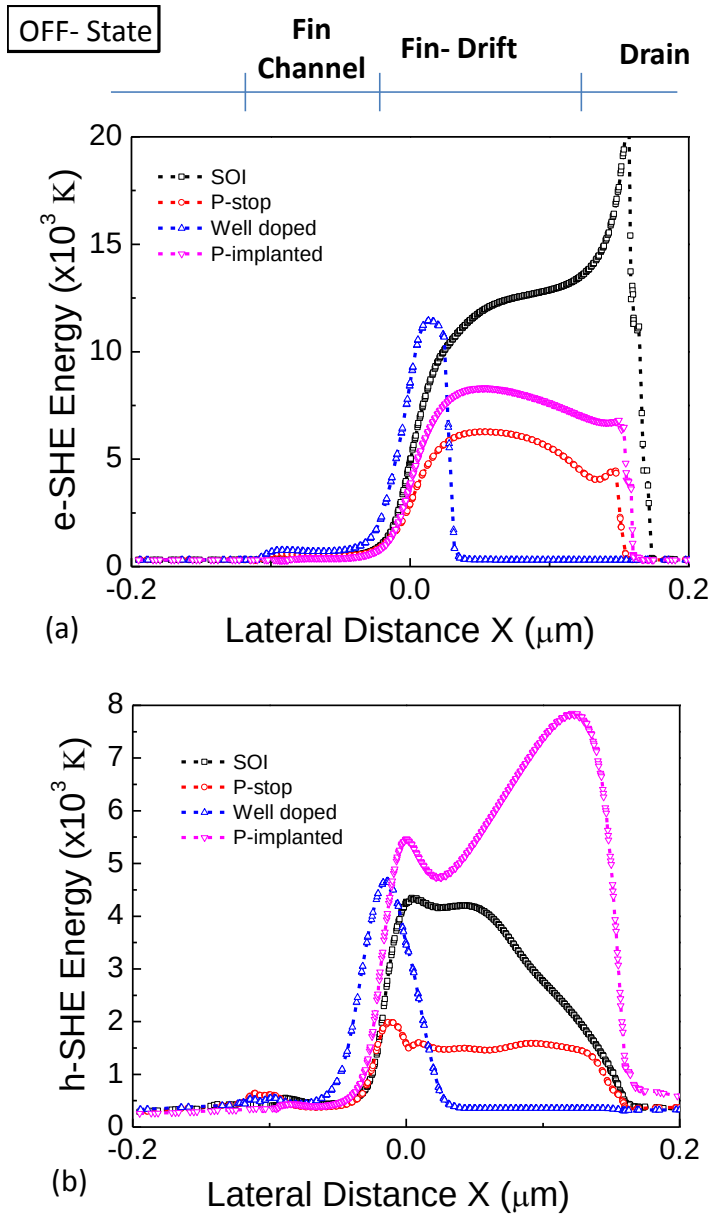


Figure 7.23: Hot carrier energy profiles taken along the lateral distance for off-states (a) electron SHE energy (b) hole SHE energy

7.3 Well doped Multi-fin stuctures

Fig. 7.25 shows the multi-fin structured well doped DeFinFETs with and without p-implants. As seen from the figures, the number of fins is set to three. The device is simulated for a gate voltage (V_{GS}) sweep of 0 to 1.8V keeping the drain voltage (V_{DS}) at 3.3V. By increasing the number of fins from 1 to 3, it is seen that the drain current

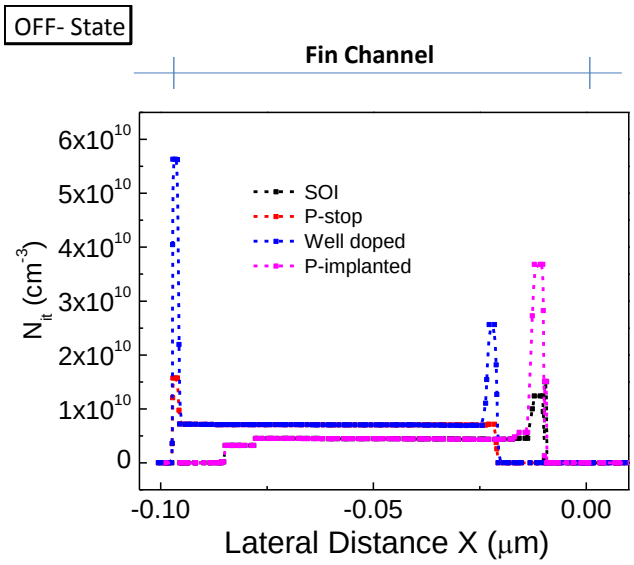


Figure 7.24: Interface trap concentration along the lateral distance

increases and the on-resistance decreases without affecting the breakdown voltage of the device.

7.4 Conclusion

This chapter presents four different high voltage FinFET device structures suitable for SoC applications and their relative performance characteristics are compared.

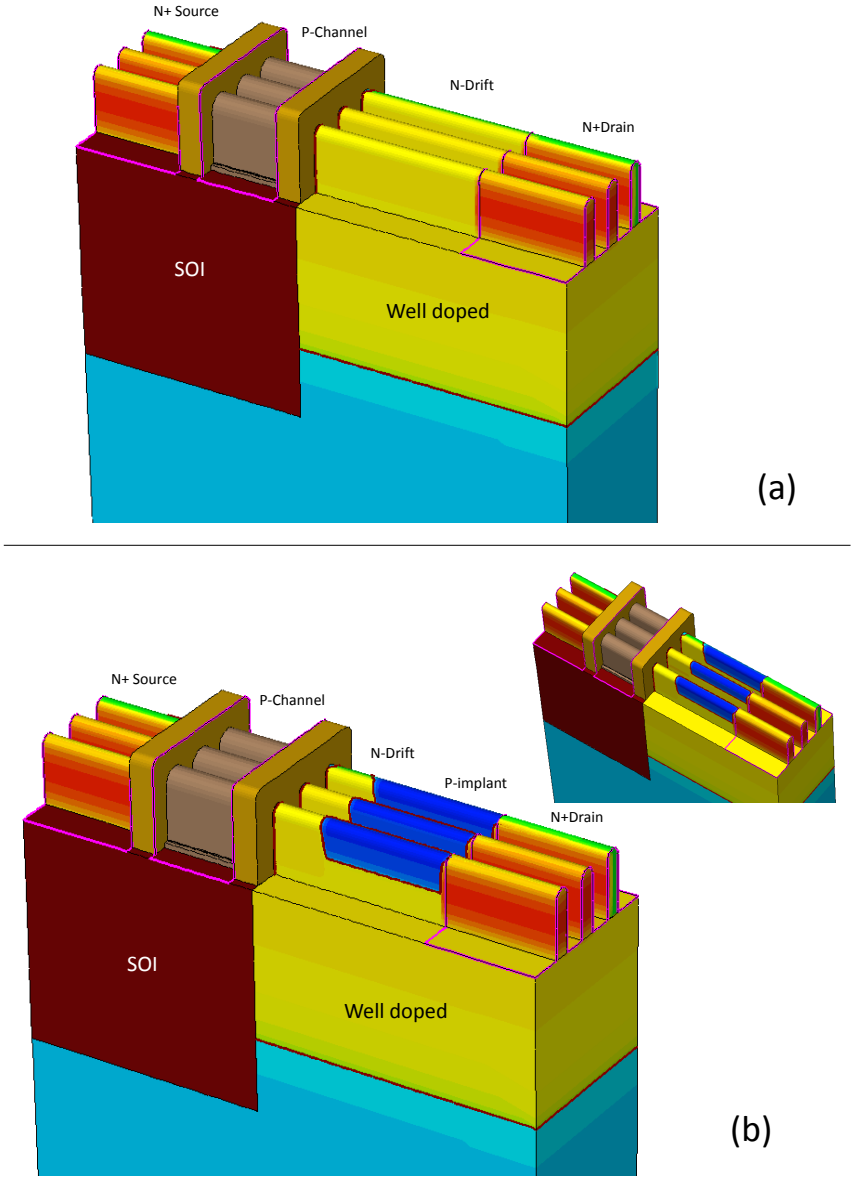


Figure 7.25: Schematics of well doped Multi-fins DeFinFET structures.

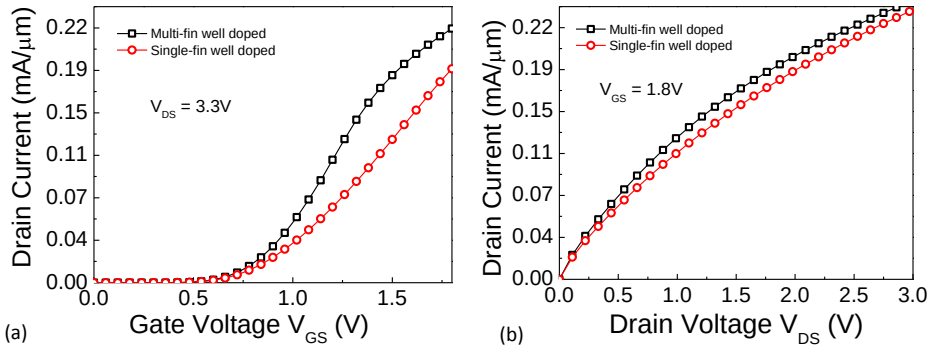


Figure 7.26: I-V Characteristics of multi-fins well doped structure (a)I_D -V_G simulated at V_{DS}=3.3V (b) I_D -V_D simulated at V_{GS}=1.8V.

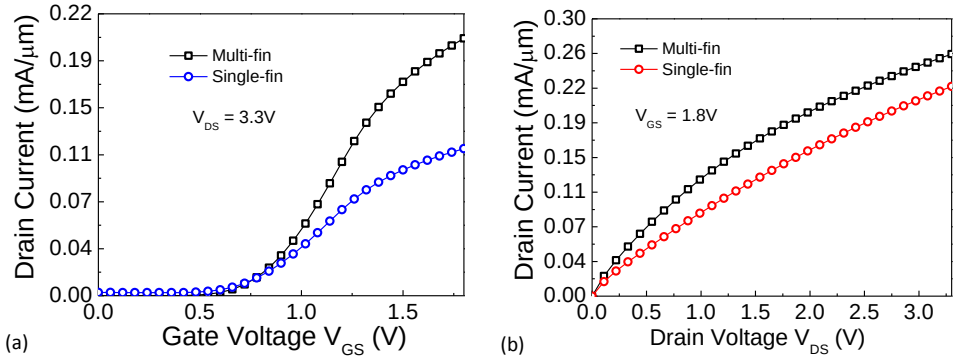


Figure 7.27: I-V Characteristics of multi-fins well doped p-implanted structure (a)I_D -V_G simulated at V_{DS}=3.3V (b) I_D -V_D simulated at V_{GS}=1.8V.

Chapter 8

Conclusions and Future Scope

This work gives a comprehensive insight in the direction of design for performance as well as reliability of superjunction (SJ) DeMOS devices. Incorporating SJ-implants in the drift region and a careful tuning of the implant length, thickness, position and doping concentration results in,

- Higher breakdown voltage, V_{BD} of 23V for double RESURF device, V_{BD} of 21V for triple RESURF device, and a V_{BD} of 19V for multiple RESURF devices. This is an improvement of 50%-80% over the conventional device with an R_{ON} of $\approx 2.5k\Omega$.

SJ-DeMOS devices, for optimum p-implant doping and implant depth allows electric field to share between well junction and implant region. Independent of SJ concept, the peak field across the SJ devices is found to be lower compared to conventional device. This makes SJ devices superior in terms of on-resistance vs. breakdown voltage trade-off. It is found that a proper tuning of the p-implant in a superjunction device results in improving the breakdown voltage by 2× without affecting the on-resistance or resulted in reducing the on-resistance by 2.5× without decreasing the breakdown voltage. Moreover, for fixed on-resistance, SJ technique delays the onset of quasi-saturation and therefore improves analog and RF performance when compared to conventional DeMOS device. In terms of hot carrier reliability, single SJ DeMOS devices, both with $X_{imp} = 0$ and $X_{imp} > 0$ (double and triple RESURF DeMOS devices) have considerably lower electron and hole energy, both in the on- and off-state, when compared to conventional DeMOS device. Multiple SJ devices are found to be in between Single SJ and conventional devices. In Multiple SJ devices, hot

carrier generation and interface trap generation, both in on- and off-state is minimum in the region in and around superjunction islands. However, moving away from SJ islands, the trap generation rate approaches the conventional devices. Overall, trends from Multiple SJ device indicate a need for an optimization strategy for the placement of SJ islands with design parameters like island doping, depth and pitch to suppress hot carrier generation without sacrificing performance. Finally, it is found that the superjunction implant based devices not only improve the R_{ON} *vs.* V_{BD} trade-off, but also result in an extended SOA boundary and 10% - 20% higher ESD failure current compared to conventional design. This is attributed to higher drift region doping allowed in superjunction designs for a given breakdown voltage. ESD failure in all superjunction devices, like conventional DeMOS device, is found to be due to filament formation.

Finally the high voltage DeFinFET structures are proposed and simulated for sub-micron high voltage applications. Four different structures, namely, SOI based, p-stop based and well doped with & without p-implant, are discussed. SOI based and p-stop based structures have inferior on-state performance due to quasi-saturation mode. However, well doped have superior on-state performance. The simulation results of well doped structures show,

- Improved Breakdown voltage of V_{BD}=8-9V compared to the conventional DeFinFET devices (V_{BD}=3V).
- Higher I_{ON}/I_{OFF} ratio upto 10^8, overcoming the quasi-saturation effect.

8.1 Future Scope

Although silicon MOS technology has dominated power electronics, the performance limits of silicon devices is starting to become a serious issue, especially long term reliability of power MOSFETs. With a limited reliability perspective, this work focuses on the modification of super-junction parameters and makes a relative comparison of different devices viz-a‘-viz interface trap generation and hot carrier energy near $Si - SiO_2$ interface. The life time reliability simulations and its effect on the V_t shifts that largely affects the performance merits, have not been covered in this work. Thus life-time reliability of power MOSFETs and its improvement is a potential area of separate research work. This also implies that study on the use of new materials

is imperative to satisfy the future requirements of high performance power devices. Wide bandgap semiconductors, such as Silicon Carbide and Galium Nitride, recently gained much attention as novel power devices with certain advantages over silicon in terms of higher critical field, mobility and operating temperature. However several issues including process, reliability, interconnection and packaging need to be solved before these new materials will enjoy a reasonable market share. Therefore, despite the limitations of silicon as a semiconductor material, it still has plenty of thrust until the wide bandgap materials become popular.

On the other hand, when it comes to integration on single chip, silicon still stands out as a major candidate for advanced SoC applications that intrinsically demands integration of low-high voltage functionalities and power electronics for on-chip power management in hand held devices. Hence DeFinFETs, the next potential nano-power FETs could be another major area for exploration, where the research studies have just begun.

More recently, compound semiconductors have become the focus of research as semiconductor engineers have strived to get to the next better device, both in terms of high current density and high breakdown voltage. The bulk of the development has been for applications such as radio frequency (RF) power transistors, light emitting diodes (LEDs) and high voltage power supplies. GaN power devices are in news as it is reported that they offer high power densities with high breakdown voltages, in excess of 1000 - 1500 Volts, as discrete devices. However, very large scale integration of nano-scale heterostructures of AlGaN/GaN is still a challenge due to may process related issues. There is lot of scope for research in the design and integration of nano-scale GaN devices with traditional CMOS technology to achieve efficient, low power chips with high breakdown voltages.

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