# DESIGN OF LOW POWER SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER

Thesis

Submitted in partial fulfillment of the requirements for the degree of

**DOCTOR OF PHILOSOPHY**

by

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Dedicated to my beloved parents

# DECLARATION

I hereby ***declare*** that the Research Thesis entitled **DESIGN OF LOW POWER SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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# CERTIFICATE

This is to certify that the Research Thesis entitled **DESIGN OF LOW POWER SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER** submitted by **JAGADISH D. N.** (Reg. No. 110656EC11F02) as the record of the research work carried out by him, is accepted as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

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# Abstract

Battery operated electronic devices are severely constrained by power dissipation and voltage. Portable devices, in particular, medical implants and wireless sensors insist on smaller die size. Analog-to-digital converter (ADC) interfaces the real analog signal to the digital domain. Being the key component in these integrated circuits, ADC's design has to meet the said constraints. This thesis addresses the design challenges, strategies and circuit techniques of ultra-low-power and area efficient SAR ADCs.

In the said applications, since the conversion speed requirements are in the range of few Hz to MHz, a successive approximation register (SAR) ADC seems to be most appropriate. SAR ADCs are usually implemented using binary weighted capacitors. The ADC at medium-to-high resolution is limited by capacitor mismatch, which eventually is the bottleneck. The size of a capacitor array in itself is an indicator of power and area performance of the SAR ADC.

As a first step towards minimizing power dissipation, capacitor matching is improved by having nonbinary weighted capacitors. Second, efforts are made to remove the dependency of power dissipation on capacitor array. Third, parasitics and thermal noise affecting conversion accuracy are suitably addressed. The said strategies are infused in the proposed two novel SAR ADC architectures. To demonstrate the efficacy, a 9 bit 100 kS/s 1 V dual capacitor array SAR ADC and an 8 bit 780 kS/s $\pm$0.35 V switched capacitor based SAR ADC are implemented in CMOS 90 nm technology node. The performances are verified through simulation of layout extracted netlist. Respective figure-of-merit and core area of the implemented dual capacitor array SAR ADC are 14.5 fJ/c-s and 0.00371 $mm^2$. The same, for the case of switched capacitor based SAR ADC are 11.39 fJ/c-s and 0.00145 $mm^2$. Further, the switched capacitor based SAR ADC gels well into $\Delta\Sigma$ modulator loop and its usefulness in noise shaping is verified by simulation of the modelled ADC.



**Keywords:** SAR ADC; Low power ADC; Area efficient ADC; Nonbinary capacitor array; Switched capacitor; multi-bit SAR quantizer.

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# Abbreviations

| | |
|---|---|
| **ADC** | Analog-to-Digital Converter |
| **ASIC** | Application Specific Integrated Circuit |
| **BWCA** | Binary Weighted Capacitor Array |
| **CA** | Capacitor Array |
| **CMOS** | Complementary Metal Oxide Semiconductor |
| **CMRR** | Common Mode Rejection Ratio |
| **CR** | Charge Redistribution |
| **DAC** | Digital-to-Analog Converter |
| **DC** | Direct current |
| **DEM** | Dynamic Element Matching |
| **DFF** | D-type Flip Flop |
| **DNL** | Differential Nonlinearity |
| **DR** | Dynamic Range |
| **ENoB** | Effective Number of Bits |
| **FFT** | Fast Fourier Transform |
| **FoM** | Figure of Merit |
| **IC** | Integrated Circuit |
| **INL** | Integral Nonlinearity |
| **LSB** | Least Significant Bit |
| **MOM** | Metal Oxide Metal |
| **MSB** | Most Significant Bit |
| **NMOS** | N-channel Metal Oxide Semiconductor |
| **NTF** | Noise Transfer Function |
| **OSR** | Over-Sampling Ratio |
| **OTA** | Operational Transconductance Amplifier |
| **PMOS** | P-channel Metal Oxide Semiconductor |
| **PSRR** | Power Supply Rejection Ratio |
| **PVT** | Process, Supply voltage and Temperature |
| **RMS** | Root Mean Square |
| **SAR** | Successive Approximation Register |
| **SoC** | System-on-Chip |
| **SC** | Switched Capacitor |
| **SFDR** | Spurious-Free Dynamic Range |
| **SNDR** | Signal-to-Noise-and-Distortion Ratio |
| **SNR** | Signal-to-Noise Ratio |
| **SQNR** | Signal-to-Quantization Noise Ratio |
| **UGB** | Unity Gain Bandwidth |
| **UMC** | United Microelectronics Corporation |

# Chapter 1

# INTRODUCTION

## 1.1 MOTIVATION

Over the years processing a signal in digital domain has been attractive for a variety of reasons. Digital signals are more immune to noise than their analog counterparts. Processing of digital signals could be dynamically controlled and the information is often stored or transferred. Advances in semiconductor technology have led to the growth of digital signal processors by providing easy, accurate, economical and power efficient solutions. An analog-to-digital converter (ADC) converts an analog continuous signal to its discrete digital equivalent. ADCs are ubiquitous in digital signal processing applications as they form the interface between real world analog and digital domain. Portability and ultra low power consumption features of electronic gadgets are the demanding assets in the field of battery operated biomedical (Yoo and Hoof, 2011, Rodriguez-Perez et al., 2014, Tao and Lian, 2015) and wireless sensors (Harikumar et al., 2016). The gadgets are typically powered by small batteries or by scavenging energy from non-conventional sources. Such gadgets usually have system-on-chip (SoC) design. In order to prolong the battery discharge time, the integrated circuit (IC) should consume low power. Medical implants are highly desirable to possess lower chip surface area, to prevent surgical damage and get access to the small size biomedical information source, in addition to low power dissipation requirement. Lower chip surface area for wireless sensor nodes would enable cost effective solutions; in other words, would increase the reliability of sensor network by having more number

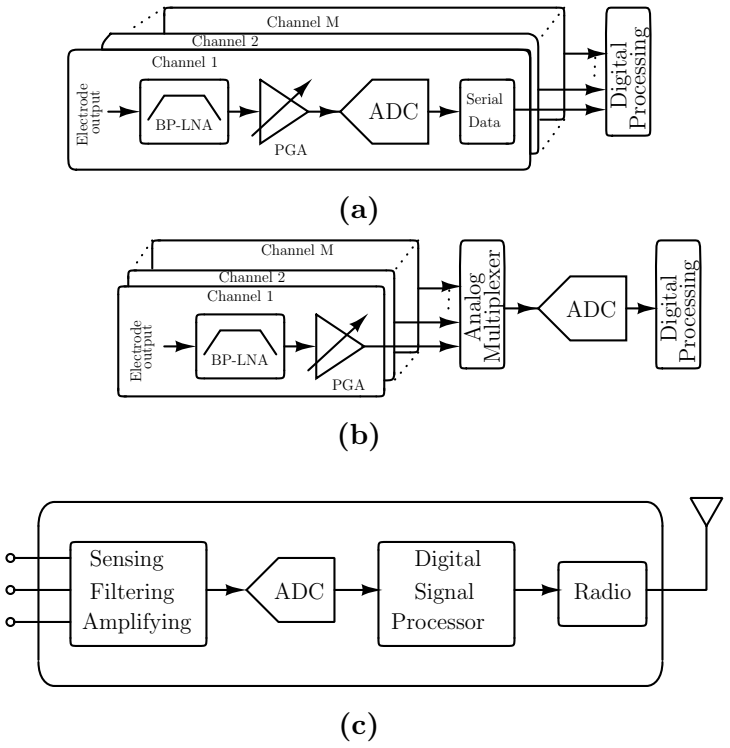



**Figure 1.1:** Block diagram of example ASICs (a) Neural recording interface IC with ADC per channel (b) Neural recording interface IC time multiplexed ADC (c) wireless sensor node.

of sensors deployed for the given cost.

Figure 1.1a and Figure 1.1b show simplified block diagrams of a neural recording interface IC (Rodriguez-Perez et al., 2014). The electrodes fetch bioelectric signals that have dynamic range between tens of micro volt to hundreds of milli volts. A bandpass low noise amplifier (BP-LNA) selects the signal of interest. Programmable gain amplifier (PGA) provides necessary gain to accomplish higher dynamic range. A 1.2 V 8-bit ADC per channel samples the signal at 90 KS/s and the serial output bits are fed to the digital processor in Figure 1.1a. The pitch of neural recording multi-electrode arrays is typically 200 - 400 $\mu$m in width. The ADC occupy around 25% of the pitch area. The overall dissipation of multi-electrode array should not exceed a few milli watts of power to avoid damages in the brain tissue. ADC is the vital component in these systems greatly influencing power dissipation and chip area. The ADC is thus constrained to dissipate not more than few $\mu$W of power per channel. Alternatively, analog signals are routed and switched to a high speed ADC

via a multiplexer. Here the ADC is time multiplexed between the channels and the arrangement is as shown in Figure 1.1b.

A wireless sensor could have its input sampling frequency from a few Hz to MHz range. A sub-nano watt 8-bit 1 KS/s ADC is reportedly used in Harikumar et al. (2016), while van Elzakker et al. (2010) reports to use 1.9 $\mu$W 10-bit 1 MS/s ADC. The core area occupied by these ADCs are in range of 0.01 to 0.02 $mm^2$.

As discussed above, the applications of biomedical and wireless sensor network impose constraints on ADC to be low power, low chip area, medium resolution and sampling speed ranging from few KS/s to few MS/s. ADCs of hearing-aid implants demand high resolution at low sampling speed (Chandrakasan et al., 2008). Such requirements of high resolution are catered by oversampled noise shaping ADCs.

The CMOS technology and supply voltage scaling favour digital components on a chip, leading to enhancement in power and speed performance. The power consumption in the digital circuits reduces quadratically with the supply voltage and this is inspiring the industry to move towards low supply voltage regime. As a result, the SoC specifications are formulated to uphold merits of low supply voltage. However, it is demanding tedious effort by designers to have both digital and analog components co-exist. Designers are hence motivated to replace analog blocks with digital counterparts whenever possible. Nevertheless, usage of more analog blocks in the design leads to reduced chip area.

Selection of an architecture for ADC is utmost important. ADCs presented at IEEE International Solid State Circuit Conference (ISSCC), from 1997 to 2016, reveals successive approximation register (SAR) ADC is the most preferred architecture due to low power consumption and area requirement (Murmann, 2016). The SAR ADCs show excellent power performance at medium resolution and low-to-medium speed range (refer Figure 1.2a and b). The area performance is excellent as can be seen from Figure 1.2c. Finally, the plot of area vs figure-of-merit (FoM) shown in Figure 1.2d reveals that SAR ADCs are area and power efficient. Another competitive ADC architecture is the delta-sigma ($\Delta\Sigma$), much preferable for higher resolution needs.

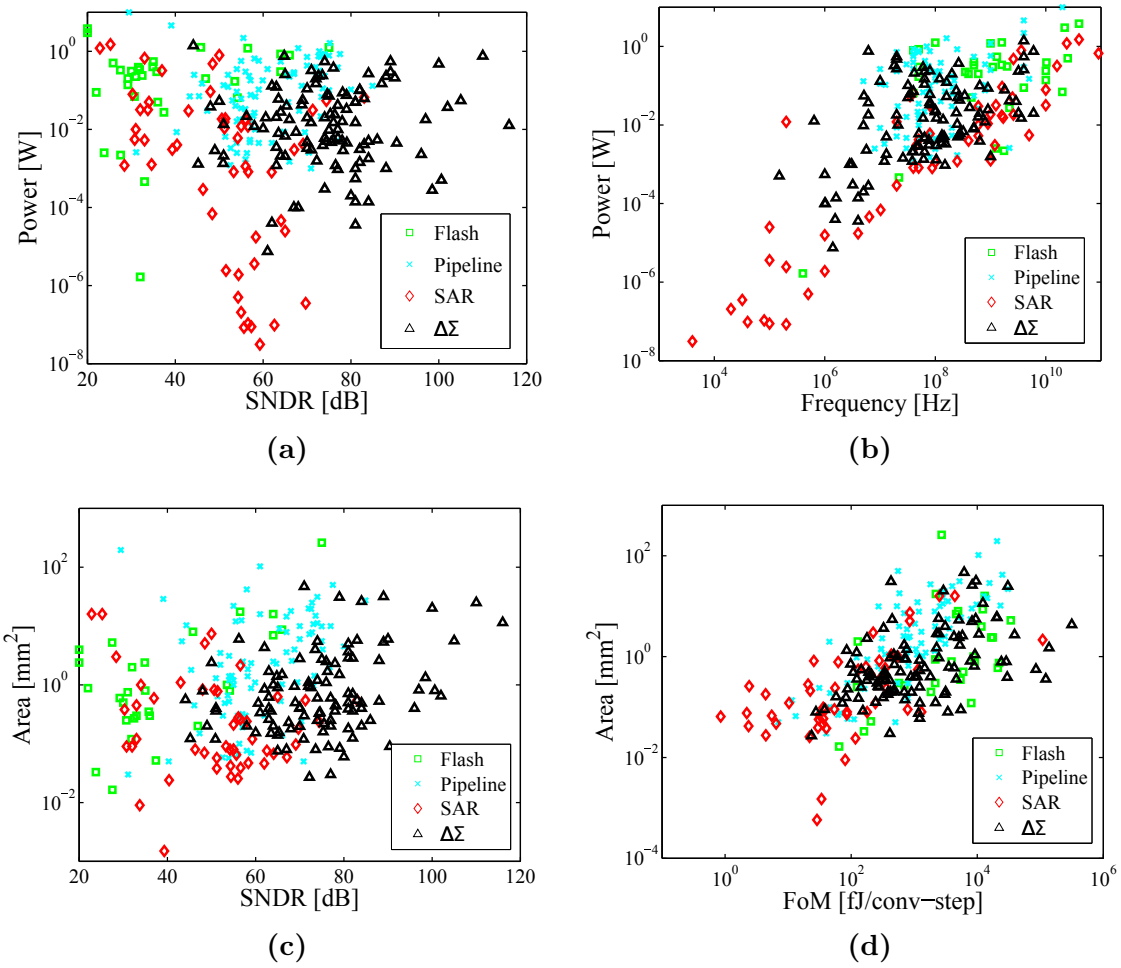



**Figure 1.2:** Performance plots of published ADCs in ISSCC (a) power vs SNDR (b) power vs Nyquist frequency (c) area vs SNDR (d) area vs FoM.

## 1.2 RESEARCH GAP

### 1.2.1 Challenges

Capacitor charge redistribution (CR) based SAR ADC was introduced and pioneered by McCreary and Gray (1975). The architecture is simple and executes binary search algorithm. The ADC comprises a digital to analog converter (DAC) realized by binary weighted capacitor array (BWCA), a comparator and a control logic block. The architecture is easily scalable, both in terms of technology and supply voltage, and is insensitive to parasitics. Size of the BWCA grows exponentially with resolution.

Thereby the voltage settling time increases. Usage of reference buffers is reported in Craninckx and Van der Plas (2007) to allow fast settling of voltage in the capacitor array (CA). This inevitably trades speed for power. Power consumption of ADC with low resolution is bounded by digital switching power; whereas, the capacitor mismatch is the bound for medium-to-high resolution. Several refinements have been brought into the CR SAR ADC, in terms of BWCA switching algorithm and DAC structure. Energy efficient switching methods are reported in Sanyal and Sun (2013). The area and power performances are however limited by capacitor mismatch of the array. Assuming a standard deviation of $\sigma_u$ from the unit capacitance $C_u$, the worst-case standard deviation of differential nonlinearity (DNL) for BWCA of an N-bit ADC is given as (Wakimoto et al., 2011)(derivation provided in subsection 2.2.2)

$$\sigma_{DNL,max} = \sqrt{2^N - 1}\left(\frac{\sigma_u}{C_u}\right)\text{LSB} \tag{1.1}$$

For the matching requirement, the unit capacitor size has to be large enough. This leads to a larger CA size. Capacitors are custom designed in Harpe et al. (2011) to achieve a lower size unit capacitor with good matching performance. Doing so, the power consumption due to the CA is reduced, whereas the area occupied by the CA still remain unaltered due to reduced capacitance density. Dynamic element matching (DEM) technique (Galton, 2010) reduces capacitor mismatch effect, but incurs additional hardware and switching losses. Main DAC circuit is split into two sub-DAC circuits in Yee et al. (1979). The sub-DACs are thereafter connected via a coupling capacitor. An extension of the array splitting technique results in C-2C ladder architecture. The refined DAC structures show a reduction in power consumption and capacitor area, however compromising on linearity due to the presence of parasitics at interconnecting nodes. Increased interconnect parasitics at lower technology nodes make routing of a large number of capacitors a challenge. Hence BWCA based SAR ADCs are area inefficient.

On the other hand, non-BWCA based SAR ADCs constituting unit sized capacitors show a good matching performance. These ADCs adopt passive sharing of charge between capacitors to generate DAC equivalent voltage. Voltage buffers are used for tracking the DAC equivalent in Kamalinejad et al. (2011) rendering the design power inefficient. Unit capacitors are serially connected in Gopal and Baghini (2010) to achieve DAC equivalent, but accuracy is lost due to switch and capacitor

bottom-plate parasitics. Switch parasitics again degrade linearity despite the usage of a large number of unit capacitors and conversion clock cycles in Chen et al. (2010). In general, the performance of these ADCs is limited by parasitics and hence requires a unit capacitor of a larger value. The chip area and total energy consumption of these ADCs would thus increase. Therefore, these architectures would be concluded as inadequate for implementation of area and energy efficient SAR ADC.

Switched capacitor (SC) integrator based SAR ADCs in Zheng et al. (1999) make use of very few unit capacitors. These ADCs operate in three phases, taking 50% additional conversion time in comparison to the conventional SAR ADC. Even though mismatch performance is good, other serious issues to be addressed are thermal noise and voltage dependent parasitics. As with most of the charge integration based ADCs, the thermal noise decides the lower bound on unit capacitance value. Obtaining a good signal to noise ratio (SNR) is challenging with low supply voltage.

To sum it up, making a choice to work with non-BWCA designers could move away from capacitor mismatch limited architecture (performance dictated by foundry technology) to parasitic and noise limited architecture. The challenge lies in coming up with ADC architectures, comprising nonbinary weighted capacitors, to meet low power consumption and low chip area despite the presence of parasitics and noise. The designed ADC should operate at low supply voltage.

Again, charge leakage at lower frequencies introduces distortion (Zhang et al., 2012). Mere oversampling of the input yields 3 dB rise in SNR for every twofold increase in oversampling ratio (OSR). However, with an oversampling scheme, the shaping of the noise will far more increase the SNR. It is desirable to have multi-bit quantizer in a $\Delta\Sigma$ modulator for following reasons: First, high resolution $\Delta\Sigma$ modulators possessing multi-bit quantizer are more stable when compared with single-bit quantizer (Schreier and Temes, 2005). The quantization error arising out of a multi-bit quantizer is smaller when compared to that of a single-bit quantizer. Second, for a given OSR and loop filter order, $\Delta\Sigma$ modulators having multi-bit quantizer yield higher SNR. Amongst various multi-bit quantizers, SAR quantizers are preferred due to their energy efficiency and simplicity in architecture. The quantizer and feedback may share the same capacitive DAC array. A typical SAR quantizer fetches 6 dB/clock cycle (due to 1 bit/cycle), whereas single-bit quantizer will fetch 9 dB for every twofold increase in OSR. Higher order loop filter calls for more active elements leading to large power dissipation. However, non trival issues arise while using

multi-bit quantizer. The feedback DAC nonlinearity impacts the performance of the modulator. While the multi-bit quantizer is multicycle, the output of the quantizer is valid only after all the quantizer bits are obtained. If the modulator loop is allowed to update in every clock cycle, the input to the quantizer will change before the conversion, thus scoring low on stability. As a precautionary measure, the quantizer input voltage is allowed to under go change only on successful conversion by the quantizer. A mechanism has to be put in place to break the modulator loop when the quantizer is engaged in conversion.

Chen et al. (2013) have demonstrated quantization noise shaping using integrator charge residue of an SC based SAR ADC. However, the technique is limited to first order alone. Therefore, it is challenging to design a high resolution ADC with a low power consumption.

Recently, Harpe et al. (2014) have presented an attractive low power and area-efficient SAR ADC. The architecture is based on BWCA. To reduce power consumption custom unit capacitors of small size is made use. The DAC uses dithering technique, wherein a known noise is added to the capacitive DAC and the ADC output is averaged for precision enhancement. The comparator offset voltage and even order harmonics are lowered by chopper technique usage at both input and output terminals of comparator. Finally, a data-driven noise reduction technique lowers quantization noise by means of voting mechanism. All the said improvements come at the cost of oversampling and additional circuit overhead, which could be reasonably well for high resolution requirements, but might not be much desirable for medium resolution.

### 1.2.2 Strategies Adopted

Following are the strategies adopted while designing the ADCs.

- As a first step towards achieving low power dissipation, unit capacitors are made use in the ADC designs. The size of unit capacitors are in a range comfortable to achieve good matching and require no reference buffers.

- Secondly, binary fractions of supply voltage is achieved by passive sharing of charge between unit capacitors (refer Figure 1.3a). Two unit capacitors are initially precharged to voltages $v_1$ and $v_2$. With closure of switch, the charge is shared between capacitors to lead a voltage of $\frac{v_1+v_2}{2}$ across them. This process

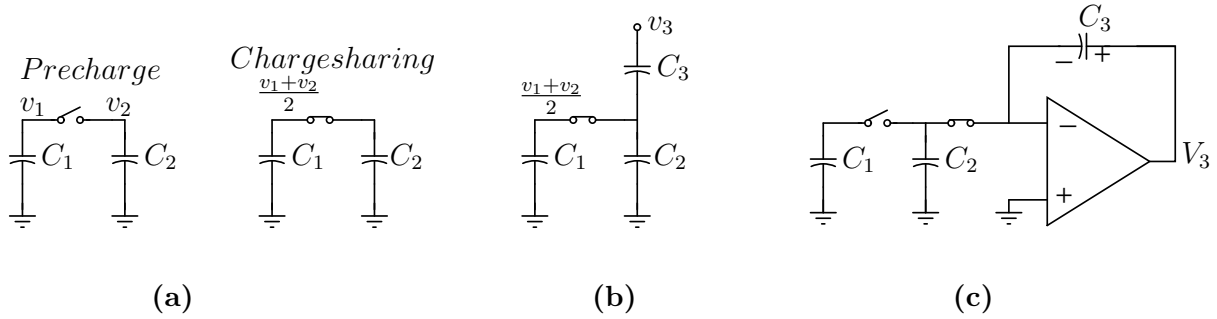



**Figure 1.3:** Strategies adopted (a) passive sharing (b) voltage addition by cascading of capacitors (c) voltage addition by active integration.

literally requires no energy from supply rails and hence able to disassociate power dissipation metric from DAC capacitor array. Though passive sharing of charge is power efficient, the sharing accuracy is limited by voltage dependent parasitics. Such parasitic variation is reduced by limiting voltage variations across the unit capacitors.

- Third, shared charges are utilized to realize DAC equivalent voltage, either by means of cascading of charge shared capacitors (refer Figure 1.3b) in the first ADC design and by means of active integration of shared charge (refer Figure 1.3c) in the second ADC design in this thesis. Former method leads to digital intensive control logic block, wherein the power dissipation could be brought down if technology scaling or low power digital design techniques are incorporated. The latter method requires an active element circuit (SC circuit) for integration of charge.

- The presence of amplifier circuit may appear to penalize the design by increasing power dissipation, however, transistors designed in sub-threshold region will keep the power consumption low. Since the ADC operates at low voltage level, the noise, mainly the input referred thermal noise of integrator, is a serious limiting entity. The gain of the integrator is reduced to half to attenuate the noise. Thus obtained low noise integrator becomes useful to trade ADC noise for further reduction of power consumption.

- The bandwidth of the ADC is extended by reducing switch ON state resistances. For this purpose, while inplementing the switches, the transistors threshold

voltage is brought down by means of slight forward bias of body terminals.

- For the demands of higher resolution at low sampling frequencies, the integrator based ADC can be used with oversampling scheme. The integrator charge residue, is preserved, sampled and fed back to realize quantization noise shaping by second order. The noise-shaping technique will thereafter realize a lowpass, bandpass and highpass $\Delta\Sigma$ ADC.

## 1.3 RESEARCH OBJECTIVES

In this research, the focus is towards exploring SAR ADC architectures with the usage of nonbinary weighted capacitors. The objective is to introduce novel architectures and switching methods to deliver low power consumption and area efficient SAR ADCs, with the number of conversion clock cycles remaining close to that of traditional. The proposed architectures are to have attributes of good capacitor matching, low noise and largely parasitic insensitive. The ADCs are to be designed and implemented at 90 nm technology node using UMC foundry library models. The laid out designs are to be extracted and characterized using simulations. The designs are to work satisfactorily under the presence of noise and for all process variations.

The neural recording interface IC (refer Figure 1.1a) demands the ADC to operate around 1 V supply voltage and 100 KS/s. For a medium resolution, the power requirement is few $\mu$W with core area demand in the range of 0.01 to 0.02 $mm^2$. A column parallel ADC shall be time multiplexed between 8 channels (refer Figure 1.1b). The sampling speed requirement will increase by 8x. The increased sampling rate dissipates relatively higher power. To restrict the power dissipation, the supply voltage is intended to a low value. The specifications of the proposed ADCs are summarized in Table 1.1.

**Table 1.1:** Specifications of proposed works

| Work | Supply voltage (volt) | Power ($\mu$W) | Resolution (bits) | Approx. speed (MS/s) | Technology |
|---|---|---|---|---|---|
| I | 1 | 1 | 8-9 | 0.1 | UMC 90 nm |
| II | 0.7 | 1 | 7-8 | 0.8 | |

## 1.4 CONTRIBUTION AND ORGANIZATION OF THESIS

The major contributions of this research work are summarized below:

- Dual CA based SAR ADC architecture is presented. Each CA comprise unit sized capacitors. The DAC equivalent voltage generation is largely parasitic insensitive. Complexity in the design is shifted to digital circuit blocks. An energy efficient switching algorithm is presented. A 9 bit 473 nW 0.1 MS/s SAR ADC is designed using 90 nm UMC library and works at a supply voltage of 1 V. The ADC core occupies an area of 0.00371 $mm^2$.

- SC integrator based SAR ADC architecture is presented. The architecture is largely parasitic insensitive and has low noise characteristics. The design constitutes unit sized capacitors. An efficient operational transconductance amplifier (OTA) is designed. Noise analysis of the architecture is carried out to verify the low noise attribute. An 8 bit 931 nW 0.78 MS/s SAR ADC is designed using 90 nm UMC library and works with a dual power supply voltage of $\pm$0.35 V. The ADC core occupies an area of 0.00145 $mm^2$.

- A noise shaping SAR ADC is proposed. The ADC uses an SC integrator. The inherent quantization error voltage storage ability of the SC integrator is exploited. A first and a second order delta-sigma modulator architectures using a single SC integrator are proposed. The behavioral model of the ADC is developed and functionality verified. The proposed ADCs are suitable for delivering higher resolutions at lower input frequencies.

The rest of this thesis is organized as follows. Chapter 2 introduces basics and accuracy performance of SAR and $\Delta\Sigma$ ADCs. In Chapters 3 and 4, two new SAR ADC architectures are presented: a 9 bit 473 nW 0.1 MS/s and an 8 bit 931 nW 0.78 MS/s SAR ADC in 90 nm CMOS. Chapter 5 proposes a noise-shaping technique using SAR ADC. Finally, the thesis is concluded in Chapter 6 listing scope for future work.

# Chapter 2

# THEORY

SAR ADCs are at the forefront in delivering high performance requirements. The growth in semiconductor technology and the portable electronics emphasize the need to study the ADC and its precision entities. In this chapter, the basics of conventional SAR ADC and its precision parameters are discussed. The performance metrics of the ADC, in general, are introduced. Recently SAR ADCs are being used within $\Delta\Sigma$ modulators to achieve high resolution. Hence $\Delta\Sigma$ modulator and the switched capacitor integrator, a circuit used in realization of many discrete time signal processing blocks, are studied towards the end.

## 2.1 SAR ADC

The basic functionality of a SAR ADC is very simple. Figure 2.1 shows the block diagram of the ADC. The sample-and-hold circuit samples the analog input signal $V_{in}$ to be converted and presents the same at one of the input terminals of the comparator. The SAR control logic module approximates the presented input voltage $V_{in}$ by successively comparing it with aggregated binary fractions of reference voltage, $V_{DAC}$. This voltage is in place due to an internal DAC and is updated after every comparison activity. During comparison, if $V_{in}$ is greater than $V_{DAC}$, the output of the comparator is a logic high, else it is logic low, and the same is communicated to SAR control logic module.

The module consists of an N bit register. The N bit register is initially set to

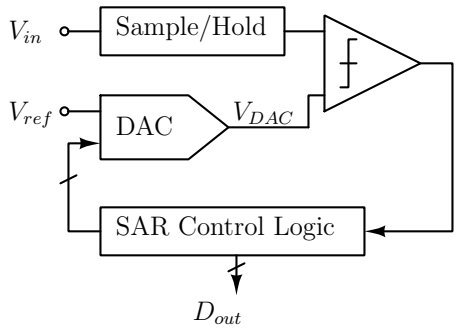



**Figure 2.1:** Block diagram of a SAR ADC.

midscale value, by setting the most significant bit (MSB) to logic high. After comparison, if comparator outputs a logic high, the assumption of having MSB as logic high is true, else MSB is reset. This step of assuming a bit and testing for the same is generally referred to as bit testing. Second most MSB is set to logic high in the next cycle and tested similarly. Conversion will be completed after all N bits are tested. This process of converting an analog signal to its digital equivalent is commonly known as binary search algorithm. Towards the end of conversion, voltage $V_{DAC}$ will be within a vicinity of 1 least significant bit (LSB) from voltage $V_{in}$. An N bit SAR ADC requires a minimum of N clock cycles.

Figure 2.2 shows voltage waveforms, wherein $V_{DAC}$ tracks $V_{in}$ for an example 4 bit ADC. The binary data resident in the register, towards the end of conversion cycle, represents the digital output of the ADC.

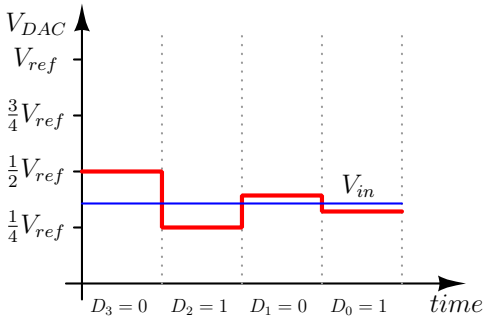



**Figure 2.2:** Voltage waveforms within a SAR ADC.

## 2.2 PRECISION CONSIDERATIONS

### 2.2.1 Sampling Circuit

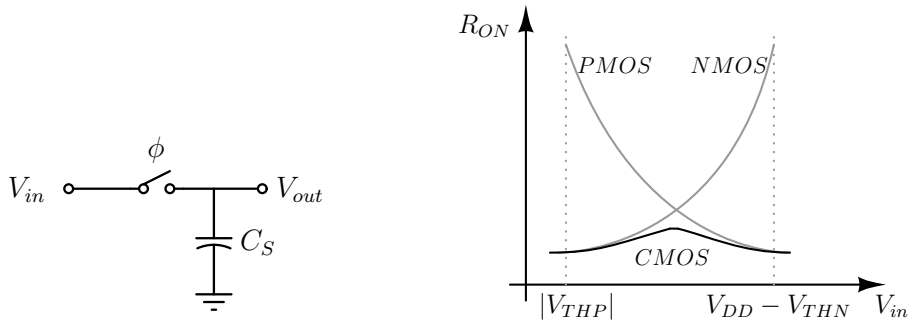



**Figure 2.3:** Sampling circuit: (a) Circuit diagram (b) Switch on-state resistance plot.

A basic sampling circuit constitutes a switch and a sample-and-hold capacitor $C_S$ as shown in Figure 2.3a. When the switch is closed during the $ON$ phase of clock $\phi$, the capacitor $C_s$ charges to voltage $V_{in}$ and the same is held at the output terminal when $\phi$ is lowered. The switch implementation using either PMOS or NMOS only transistor shows large variation in resistance with input voltage and also reduced input voltage range. CMOS implementation of the switch however overcomes these drawbacks. The on-state switch resistance $R_{ON}$ for various implementations is shown in Figure 2.3b. The circuit has finite track bandwidth $f_{3dB}$ due to finite value of circuit elements.

$$f_{3dB} = \frac{1}{2\pi R_{ON} C_S} \tag{2.1}$$

Considering the sampled voltage to settle with an error less than 1/2 LSB for an N bit resolution, the settling error voltage has to satisfy

$$e^{-t/R_{ON}C_S} < \frac{1}{2^{N+1}} \tag{2.2}$$

Assuming that a half-period sampling clock is being used, the sampling frequency $f_s$ and the track bandwidth are related as

$$f_{3dB} > \frac{(N+1)ln2}{\pi} f_s \tag{2.3}$$

Any effort to enhance track bandwidth by lowering component values aggravates switch induced errors, parasitic effects and thermal noise. The ON state resistance of the switch could be lowered by slight forward bias of the bulk-source pn junction. The threshold voltage due to the bias is given by

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{2.4}$$

$V_{TH0}$ is the threshold voltage of transistor when body-source pn junction is unbiased, $\gamma$ is body effect coefficient, $\phi_F$ is Fermi potential and $V_{SB}$ is source-body bias potential. $\gamma$ is positive for NMOS, but negative for PMOS. Potential $\phi_F$ is negative for NMOS, but positive for PMOS. From (2.4) it is clear that the threshold voltages of both NMOS and PMOS transistors could be lowered by forward biasing of body-source pn junctions. But under such bias, the bias voltage should be kept sufficiently low to ensure that the junction do not conduct.

As soon as the sampling switch is turned OFF, the conduction channel between source and drain of the transistor ceases. The charge in the channel will be split between the drain and source. The charge entering into sampling capacitor when switch is turned OFF, known as channel-charge injection, leads to an error voltage. The injected charge is linearly related to sampled input and threshold voltages, resulting in a gain error (the threshold voltage itself is nonlinearly related to input voltage due to equivalent source to bulk biasing, leading to distortions). Equal distribution of charge between source and drain is imprecise; in worst-case all charge may end at one node. In reality the fraction of charge that exits through the source and drain terminals is a relatively complex function of various parameters such as impedance seen at each

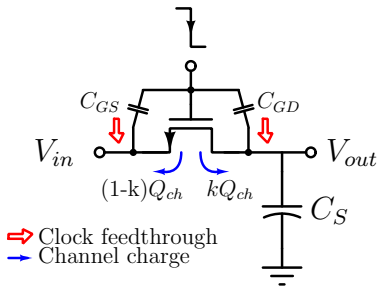



**Figure 2.4:** Switch induced errors.

terminal to ground and the transition time of the clock. No good rule of thumb. Simultaneously, during turning OFF of the switch, the gate voltage change is imposed on to the sampling capacitor by means of capacitor coupling between the two. This effect known as clock feedthrough and the channel-charge injection are illustrated in Figure 2.4. These switch induced error voltage could be together approximated for an NMOS and a PMOS switch as

$$\Delta V_N = -\frac{k_N W_N L_N C_{ox}(V_{DD} - V_{THN} - V_{in})}{C_S} - \frac{C_{GD,N}}{C_{GD,N} + C_S} V_{DD} \tag{2.5}$$

$$\Delta V_P = \frac{k_P W_P L_P C_{ox}(V_{in} - V_{THP})}{C_S} + \frac{C_{GD,P}}{C_{GD,P} + C_S} V_{DD} \tag{2.6}$$

where $k_N$ and $k_P$ are the fraction of channel-charge injected by respective NMOS and PMOS transistors on to the sampling capacitor, $C_{ox}$ is the unit gate oxide capacitance, $V_{THN}$ and $V_{THP}$ are the threshold voltages, and $C_{GD,N}$ and $C_{GD,P}$ are the gate drain overlap capacitance of NMOS and PMOS, respectively. In both (2.5) and (2.6), clock feedthrough component is represented as an offset error while channel-charge injection error voltage is signal dependent. A CMOS switch makes better effort to reduce the offset error voltage but not the signal dependent error to the fullest. The signal dependent error will cause conversion nonlinearity and hence either of techniques, such as bottom-plate sampling, bootstrapping and half-sized dummy transistor usage could be employed. Figure 2.5 shows the simpler circuits of bottom-plate sampling and NMOS transistor switch bootstrap. During phase $\phi$ the main switches are turned

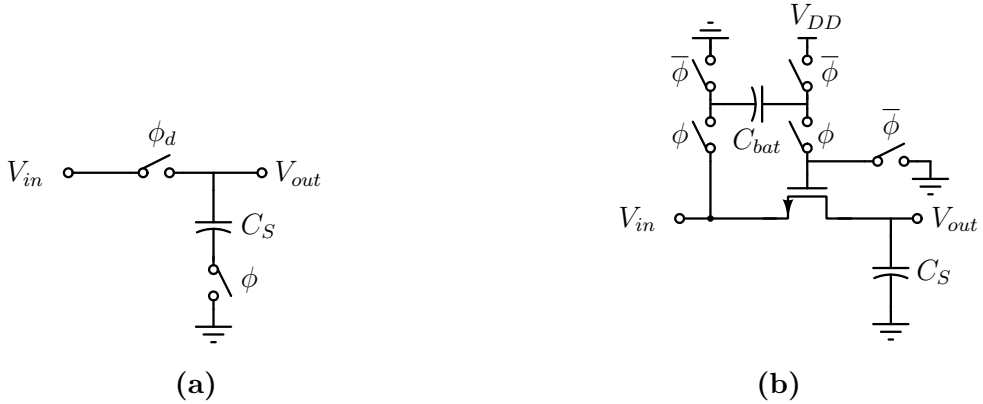



**Figure 2.5:** Input voltage sampling using (a) Bottom-plate circuit (b) NMOS bootstrap circuit.

ON. In case of bottom-plate sampling, the switch connected at the bottom plate of the capacitor $C_S$ is turned OFF before phase $\phi_d$ goes low. The injected channel charge to the capacitor is always constant. The capacitor $C_{bat}$ is precharge to the voltage $V_{DD}$. The gate-to-source voltage, $V_{GS}$, is equal $V_{DD}$ in case of bootstrap circuit. When the switch is turned OFF, the injected channel charge to the capacitor $C_S$ is constant In the absense of these sampling methods, it requires the sampling capacitor size to be increased to reduce the error voltage.

While the transistors are operated under weak inversion, the OFF-state current conduction leads to charge leakage. The leakage current for a transistor is expressed as Roy et al. (2003)

$$I_{leakage} = \mu_0 C_{OX} \frac{W}{L}(m-1)V_T^2 e^{\frac{V_{GS}-V_{TH}}{mV_T}}(1-e^{-\frac{V_{DS}}{V_T}}) \tag{2.7}$$

where $m$ is the subthreshold swing coefficient. (2.7) shows nonlinear relation between leakage current and the switch voltages, thereby introducing harmonic distortions. As a result, the leakage current limits the voltage accuracy of the capacitor. The relation is expressed as

$$I_{leakage} \leq C f_S k LSB \tag{2.8}$$

Here $k$ is the required accuracy as a fraction of LSB and $f_S$ is the sampling frequency.

In addition to sampling capacitor the output node has parasitic capacitors. These parasitics are due to gate-drain overlap and drain-body junction capacitance. When the switch is in off-state, the parasitic capacitance $c_p$ due to a transistor is given by

$$c_p = C_{GD} + C_j W L_D + 2C_{jsw}(W + L_D) \tag{2.9}$$

where $L_D$ is the length of the drain diffusion region and, $C_j$ and $C_{jsw}$ are the bottom and side-wall junction capacitances respectively. Figure 2.6 shows associated parasitics at the output node for various switch implementations. The parasitics are nonlinear and draws more attention if the sampled charge needs to be processed. Although CMOS switch offers larger parasitics than just a single transistor switch, the voltage dependency is reduced.

The ON-state resistance of the switch introduces thermal noise, whose power spectral density (PSD) is $4kTR_{ON}$, where $k$ is the Boltzmann constant and $T$ is the

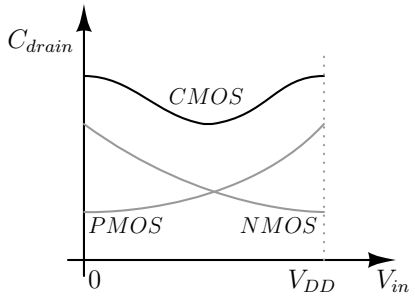



**Figure 2.6:** Switch parasitics.

absolute temperature. With the sampling circuit having finite bandwidth the thermal noise power is $kT/C_S$. As it is known, the quantization noise sets fundamental limit on linearity performance of the ADC. Assuming quantization noise to be white, wherein the error voltage range between $-\Delta/2$ to $+\Delta/2$, the quantization noise power for an N bit ADC with a full-scale voltage range of $V_{FS}$ is given by

$$\overline{V_q^2} = \int_{-\Delta/2}^{\Delta/2} \frac{1}{\Delta} e^2 de = \frac{V_{FS}^2}{12 \times 2^{2N}} \tag{2.10}$$

The thermal noise is usually considered equal to quantization noise and hence the total noise is increased by a factor of 2, thus reducing the performance from the ideal by 3 dB. The minimum size of sampling capacitor will thus be

$$C_S = 12kT \frac{2^{2N}}{V_{FS}^2} \tag{2.11}$$

Other sources that affect sampling accuracy are clock jitter and subthreshold leakage of charge. Clock jitter causes uncertainties in the time from sample mode to hold mode. The error is prominent in high frequency sampling circuits. Use of low leakage transistors offered by modern technology foundaries have been able to reduce subthreshold leakage of charge.

### 2.2.2 Capacitive DAC

Typically DAC circuit of a SAR ADC is implemented using capacitive elements. The reason being that the capacitors are easily fabricated with less mismatch er-

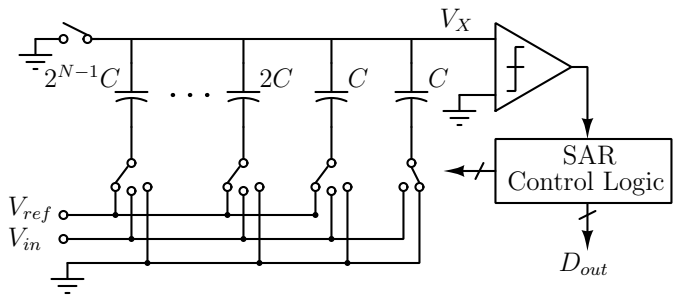



**Figure 2.7:** Circuit diagram of a typical CR SAR ADC.

rors and higher power efficiency than resistor counterparts. Figure 2.7 illustrates an N bit CR SAR ADC. A BWCA forms the capacitive DAC. It takes $2^N$ unit capacitors to realize the DAC. Bottom-plate input voltage sampling by DAC capacitors avoids requirement of a sample-and-hold capacitor. During the conversion, capacitor bottom-plates are switched accordingly. By following the binary search algorithm, the voltage $V_X$ could be written as

$$V_X = -V_{in} + V_{ref} \sum_{k=1}^{N} \frac{B_{N-k}}{2^k} \tag{2.12}$$

Here $B_{N-k}$ denotes $k^{th}$ bit value.

The unit capacitor, denoted by $C_u$, has to be small in order to minimize power consumption and area occupied by the DAC. The unit capacitor, is in general modelled as a combination of nominal capacitance $C_u$ and standard deviation $\sigma_u$. Due to the accumulation of the capacitor mismatch, the worst-case standard deviation of differential nonlinearity (DNL) and integral nonlinearity (INL) occur at the MSB code transition. The standard deviation of DNL is severe of two, and is expressed as (1.1). The derivation of (1.1) is as follows. Assume that all the bottom plate of capacitors are connected to the ground. The maximum DNL error occurs during the code transition from 011...1 to 100...0 at the midpoint where the number of capacitors (by size) that change their state is maximal. $V_X$ is the voltage at input terminal of comparator before the code transition and $V_X$ is that after the transition.

$$V_X = \frac{(2^{N-1} - 1)C}{2^N C} V_{ref} \tag{2.13}$$

$$V_X^{'} = \frac{2^{N-1}C}{2^N C} V_{ref} \tag{2.14}$$

The ideal difference in voltages

$$(V_X^{'} - V_X) = \frac{2^{N-1}C - (2^{N-1}-1)C}{2^N C} V_{ref} \tag{2.15}$$

Consider the capacitor $C = C_u + \Delta C_u$, where $C_u$ is the average unit capacitor and $\Delta C_u$ is the standard deviation. Each capacitor in the array consists of unit capacitors connected in parallel. When the number of unit capacitor connected in parallel is m, the average of the total capacitance is m$C_u$, whereas the standard deviation is $\sqrt{m}C_u$, assuming that they are not correlated. The standard deviation of LHS of (2.16) is

$$\sigma(V_X^{'} - V_X) = \frac{2^{N-1}C + \sqrt{2^{N-1}}\Delta C_u - (2^{N-1}-1)C - \sqrt{2^{N-1}-1}\Delta C_u}{2^N C + \sqrt{2^N}\Delta C_u} V_{ref} \tag{2.16}$$

From (2.15) and (2.16), the maximum standard deviation of DNL error voltage is

$$\sigma_{DNLmax} = \sigma(V_X^{'} - V_X) - (V_X^{'} - V_X) = \frac{\sqrt{2^{N-1}}\Delta C_u - \sqrt{2^{N-1}-1}\Delta C_u}{2^N C + \sqrt{2^N}\Delta C_u} V_{ref} \tag{2.17}$$

Assuming $2^N \gg \sqrt{2^N}$ and $LSB = V_{ref}/2^N$,

$$\sigma_{DNLmax} \approx \sqrt{2^N - 1}\sigma\Big(\frac{\Delta C_u}{C_u}\Big) LSB \approx \sqrt{2^N - 1}\Big(\frac{\sigma_u}{C_u}\Big) LSB \tag{2.18}$$

By following the analysis in Pelgrom et al. (1989), the standard deviation of capacitor mismatch between two capacitors is given by

$$\sigma\big(\frac{\Delta C_u}{C_u}\big) = \frac{K_\sigma}{\sqrt{A}} \tag{2.19}$$

where $K_\sigma$ is the matching coefficient and $A$ is the area occupied by the capacitor. With $K_C$ representing capacitor density, capacitor $C = K_C A$. Factor $\sigma_u/C_u$ is the standard deviation of capacitor mismatch due to single capacitor to its nominal value, which is $\sqrt{2}$ times smaller in value than that between two capacitors. Hence (2.19)

could be written as

$$\sqrt{2}\frac{\sigma_u}{C_u} = \frac{K_\sigma}{\sqrt{C_u/K_C}} \tag{2.20}$$

For a high yield, its is essential to have $3\sigma_{DNL,max} \leq \frac{1}{2}LSB$. This is to mean

$$3\sqrt{2^N - 1}\Big(\frac{\sigma_u}{C_u}\Big)LSB \leq \frac{1}{2}LSB \tag{2.21}$$

Using the result of (2.20),

$$3\sqrt{2^N - 1}\Big(\frac{K_\sigma}{\sqrt{2}\sqrt{C_u/K_C}}\Big) \leq \frac{1}{2} \tag{2.22}$$

Solving,

$$C_{u,min} = 18(2^N - 1)K_C K_\sigma^2 \tag{2.23}$$

From (2.11) and (2.23), it could be noticed that the total capacitance of DAC almost quadruples for every increase in resolution bit, for circumstances when the ADC is limited by either noise or capacitor mismatch. Table 2.1 shows an estimate of minimum value of total capacitance required for the DAC circuit.

Though mismatch limited capacitance requirement is large, architectural changes to the DAC could be done to reduce the total capacitance, such as using sub-DACs or DEM or dithering technique. The noise is however very much inherent and the minimum capacitance due to noise has to be met. Hence high resolution SAR ADCs

**Table 2.1:** Required Minimum Total DAC Capacitance Versus Resolution

| N | $C_{DAC}$ | | unit |
|---|---|---|---|
| | noise limited | mismatch limited | |
| 8 | 3 | 235 | fF |
| 9 | 13 | 941 | fF |
| 10 | 52 | 3,771 | fF |
| 11 | 208 | 15,090 | fF |
| 12 | 833 | 60,380 | fF |

$K_C = 2\ fF/mm^2$, $K_\sigma = 1\%\ \mu m$ and $V_{FS} = 1\ V$

are noise limited. Contrastingly, low resolution SAR ADCs are mismatch limited (mismatch between capacitors is dictated by foundry technology). The minimum size of unit capacitance is thus
$C_{u,min}$ = max (capacitance due to noise, mismatch limitation).

### 2.2.3 Comparator

Comparator is a critical entity in the ADC architecture. It compares the instantaneous value of two analog inputs and generates a binary output accordingly. A straightforward approach in making a comparator is to design a high gain differential amplifier with single-ended large swing output. These kind of comparators are called open-loop comparators and a such circuit is shown in Figure 2.8. A high resolution

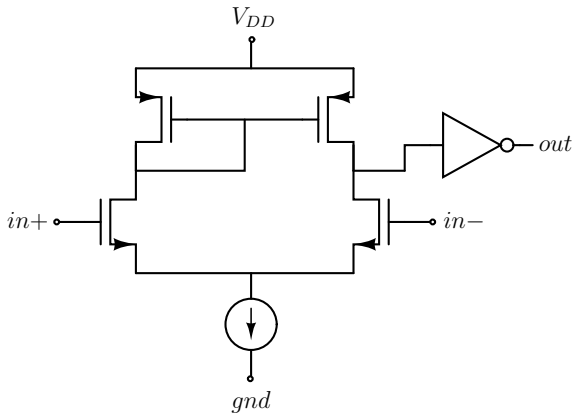



**Figure 2.8:** Circuit diagram of a open loop comparator.

comparator demands high gain amplifier. But, a single stage amplifier could only achieve this only on losing the bandwidth. To overcome this a multistage amplifier shall be used. An uncompensated two stage OTA is a good example of such comparator. The comparator also consume large amount of power. A more common way is to employ a latched comparator, as shown in Figure 2.9. Latch-only comparators make use of the combination of amplification and positive feedback. They operate in discrete-time domain rather than continuous-time domain. They operate in two phases. In the reset phase, the comparator tracks the inputs; in the regeneration phase, the positive feedback starts to work and the comparator generates a digital output based on the applied differential voltage. They are faster compared to open

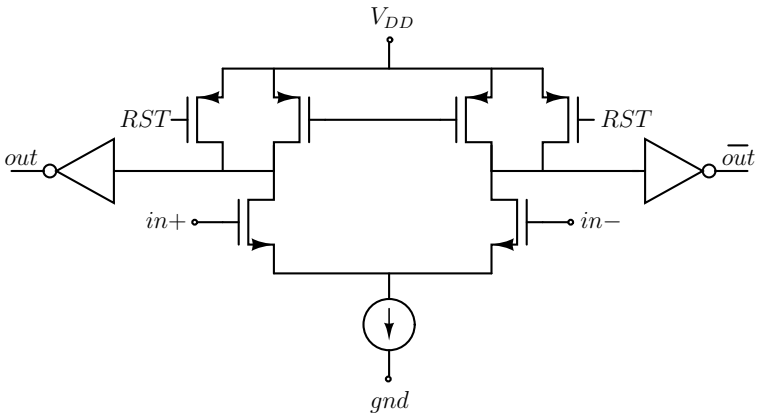



**Figure 2.9:** Circuit diagram of a latch-only comparator.

loop comparators. The speed of operation is directly proportional to the bias current of the latch and therefore power consumption. Moreover, due to the mismatch of the transistors in the latch, high input referred offset voltage directly adds to the total ADC offset. The offset could be minimized by allowing a pre-amplifier in front of the regenerative latch. A more power efficient approach is to design a dynamic latched comparator, shown in Figure 2.10, which only consumes the power during regeneration phase.

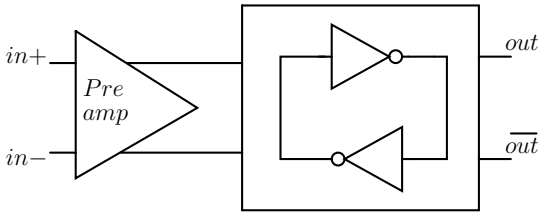



**Figure 2.10:** Circuit diagram of a dynamic latch comparator.

Several factors are to be considered while designing comparators. Overall gain has to be large to resolve small differential input voltages. A high gain regenerative latch offers a higher bandwidth, but along with it comes a large offset voltage and dynamic power consumption. A pre-amplifier with relatively large gain may help to reduce offset and input referred noise. Further more, the offset of the pre-amplifier could be reduced by employing a chopper circuit, at both input and output terminals of the comparator (Harpe et al., 2014). In addition, the chopper circuit eliminates

all the even order harmonics. The large voltage transitions at its output terminals introduce unwanted noise at the pre-amplifier input terminals due to gate capacitor coupling, known as kickback noise. The input common mode range of the comparator is desirable to be large to have linear performance characteristics. Additionally, The comparison by the comparator could be repeated several times for a given input in order to reduce the quantization noise of the ADC. The quantization noise gets averaged out to provide an improved SNR.

Dynamic latch based comparators are often used in recent SAR ADC for their higher energy efficieny at moderate resolution. Figure 2.11 shows a dynamic two stage latch based comparator (van Elzakker et al., 2010). The comparator has sep-

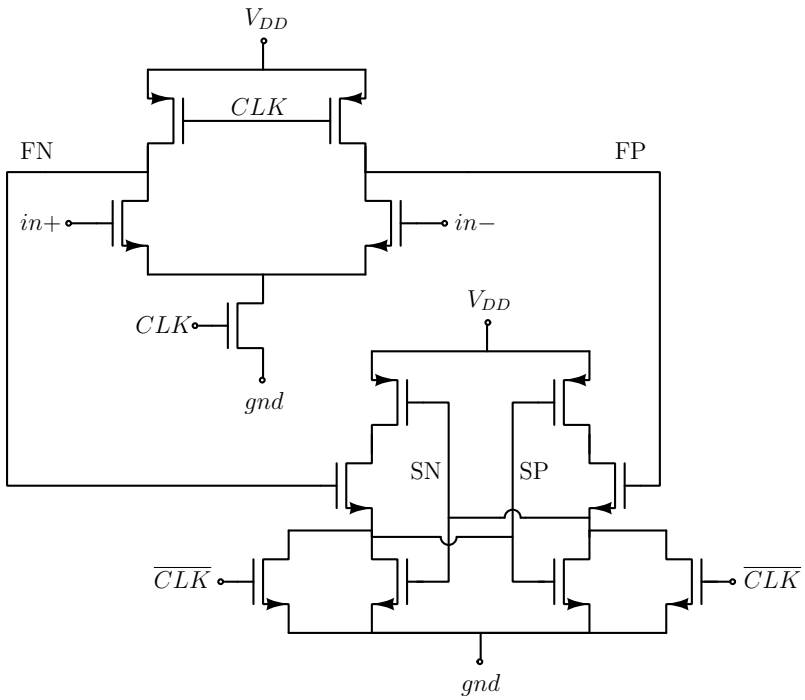



**Figure 2.11:** Circuit diagram of a dynamic two-stage comparator.

arate input gain stage and output latch stage. The architecture overcomes strong dependency between speed and input referred offset voltage, under low supply voltage constraint. Along with high input voltage range, the first stage provides sufficient gain to reduce power dissipation and, input referred offset and noise from the output stage. The output stage focusses to meet speed requirement by drawing required amount of current from supply rails.

Prior to comparison, the PMOS transistors of the first stage precharges the differential output node parasitics to voltage $V_{DD}$. As soon as the clock transits from low to high, the parasitics discharge, while the NMOS input transistors change their operating region from saturation to triode. The common mode ouput voltage, at $FN$ and $FP$, starts to move towards $gnd$. When the common mode voltage drops below PMOS threshold voltage, the second stage starts to further amplify the difference of inputs. As the common mode ouput voltage, at $SN$ and $SP$, drifts towards $V_{DD}$, the regeneration mechanism takes over to provide rail-to-rail outputs. The plot of voltage at different nodes of the comparator is shown in Figure 2.12.

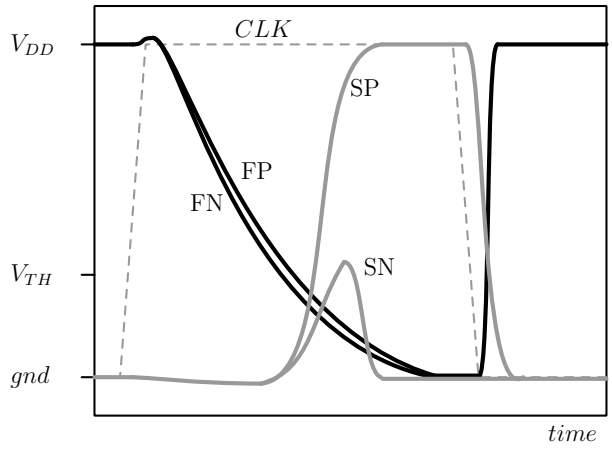



**Figure 2.12:** Plot of voltage waveforms of the comparator.

Assuming $g_m$ as the transconductance of input transistors of first stage, $C_F$ as the capacitance at nodes $FN$ and $FP$, and $t$ as the time period during which transistors are in saturation, an expression for gain of the first stage of the comparator could be written as,

$$A_V = -\frac{g_m t}{C_F} \tag{2.24}$$

Major part of the thermal noise contribution is due to input transistors of the first stage and the same for comparator designed in sub-micron technology is given as (van Elzakker et al., 2010)

$$\overline{V_n^2} \approx \sqrt{\frac{8kT}{C_F}\Big(\frac{V_{thermal}}{V_{TH}}\Big)} \tag{2.25}$$

The equation suggests to have large discharge capacitor $C_F$ at nodes FN and FP to minimize thermal noise. However, high gain is much desirable to achieve required

resolution and at the same time reduce offset voltage.

The differential output voltage is related to input differential voltage as

$$V_{od} = A_V V_{id} e^{\frac{\tau}{t}} \tag{2.26}$$

where $\tau$ is $C_F/g_{m,INV}$.

Defining a voltage $V_{eff}$ as the effective discharge node voltage during latch regeneration operation, $g_m = I_D/V_{eff}$. Regeneration time $t_{reg}$ is then

$$t_{reg} = \frac{V_{eff} C_F}{I_D} \ln \frac{V_{DD}}{A_V V_{id}} \tag{2.27}$$

The regenerative charge per step in conversion is thus

$$Q_{C,reg-s} = 2V_{eff} C_F \ln \frac{V_{DD}}{A_V V_{id}} \tag{2.28}$$

Assuming that $V_{id}$ is distributed evenly between 0 to binary fraction of $V_{ref}$, denoted by $V_m$, the average charge per step is

$$\frac{1}{V_m} \int_0^{V_m} Q_{C,reg-s} dV_{id} = 2V_{eff} C_F \Big( \ln \frac{V_{DD}}{A_V V_m} + 1 \Big) \tag{2.29}$$

Hence the charge of N conversion steps is

$$Q_{C,reg} = \sum_{k=1}^{N} \Big( 2V_{eff} C_F \Big( \ln \frac{V_{DD}}{A_V (V_{ref}/2^k)} + 1 \Big) \Big) \tag{2.30}$$

With substitution,

$$Q_{C,reg} = 2V_{eff} C_F \Big( N \ln \frac{V_{DD}}{A_V V_{ref}} + \frac{N(N+1)}{2} \ln 2 + N \Big) \tag{2.31}$$

The charge during reset operation, $Q_{rst}$ is $C_F V_{DD}$. The total energy consumption of comparator is thereby given as

$$E_{comp} = N V_{DD} Q_{rst} + V_{DD} Q_{reg} \tag{2.32}$$

On substitution,

$$E_{comp} = NC_F V_{DD}^2 + 2V_{DD}V_{eff}C_F\Big(N\ln\frac{V_{DD}}{A_V V_{ref}} + \frac{N(N+1)}{2}\ln 2 + N\Big) \qquad (2.33)$$

Assuming that the discharge capacitor size is thermal noise limited, the expression for computation of $C_F$ will be

$$C_F = 12kT\frac{2^{2N}}{V_{FS}^2} \qquad (2.34)$$

## 2.3 PERFORMANCE METRICS

### 2.3.1 Dynamic range

The dynamic range (DR) is the ratio between the maximum input signal to the minimum input signal level, that is detectable at the ADC output, within a specified frequency band.

The signal-to-noise ratio (SNR) is the ratio between signal power and noise power within a specified frequency band. The SNR is usually a function of the input signal level and more often the measured peak SNR is announced. The signal-to-quantization noise ratio (SQNR) is the ratio between signal power and quantization noise power within a specified frequency band. The maximum SQNR for an N bit ideal ADC is given as

$$SQNR = 6.02 \times N + 1.76 \quad dB$$

### 2.3.2 Linearity measures

#### 2.3.2.1 Dynamic

The signal-to-noise-and-distortion ratio (SNDR) is the ratio between signal power and noise and distortion power within a specified frequency band. The SNDR is reported in the same way as the SNR and will be slightly lower in comparison.

Spurious-free dynamic range (SFDR) is the ratio between signal power and the largest in-band spurious/distortion frequency component.

Harmonic distortion (HD) is the ratio between signal power and the specific harmonic distortion component. The most important is third-order harmonic distortion.

The total harmonic distortion (THD) is the ratio between signal power and the sum of total distortion power at harmonic frequencies.

Effective number of bits (ENoB) is the resolution obtained by the ADC. It is basically maximum SNDR expressed in terms of bits and is related as

$$ENoB = (SNDR - 1.76)/6.02$$

#### 2.3.2.2 Static

The dynamic-nonlinearity (DNL) error is defined as the maximum deviation from one LSB between two consecutive quantization levels, over the entire ADC transfer function. A DNL error specification of less than or equal to 1 LSB guarantees a monotonic transfer function with no missing codes.

The integral nonlinearity (INL) error is defined as the maximum deviation of the ADC transfer function from the best-fit line.

### 2.3.3 Efficiency

The figure-of-merit (FoM) expresses the power efficiency of the converter. For a Nyquist rate ADC, it is expressed as

$$FoM = \frac{Total\ ADC\ power}{min\{f_s, 2 \times effective\ resolution\ BW\} \times 2^{ENoB}}$$

Area efficiency (AE) merit of an ADC is computed as (Xu et al., 2012)

$$AE = \frac{Core\ area}{2^{ENoB}}$$

## 2.4 $\Delta\Sigma$ ADC

A band limited signal could be reconstructed back when its sampling frequency is atleast twice the bandwidth. The ratio between sampling frequency and twice the signal bandwidth, known as oversampling ratio (OSR), is usually $2-3$ for a regular

ADC to make anti-alias filter feasible. By oversampling a signal, the quantization noise is spread over a broad frequency range and hence reduces quantization noise density. The quantization noise floor could be written as

$$\rho(f) = \sqrt{\frac{\overline{V_q^2}}{f_s/2}} \tag{2.35}$$

where $f_s$ is the sampling frequency. The inband noise is therefore

$$\overline{V_q^2}_{,inband} = \int_0^{f_b} \rho^2(f)df = \frac{\Delta^2}{12 \times OSR} = \frac{\overline{V_q^2}}{OSR} \tag{2.36}$$

The SQNR improvement of $10\log_{10} OSR$ dB is achieved due to oversampling technique. To have a high SQNR, the sampling frequency has to be very large in comparison to signal bandwidth. On the other hand, a $\Delta\Sigma$ ADC oversamples the signal and shapes out the inband quantization noise. Thus the inband SQNR will be lower when compared to mere oversampling of the signal.

Figure 2.13 shows an architecture of a $\Delta\Sigma$ ADC. The modulator constitutes a coarse quantizer, a DAC and a loop filter. Whenever an input signal is sampled, the output of quantizer (represented by $B$ bits) is fedback to the input via DAC. The error voltage $V_{err}$ is integrated by the loop filter. The modulator output is filtered using a decimation filter that provides $N$ bits of resolution. The $\Delta\Sigma$ ADC architecture is attractive due to their robustness against nonlinearities of components in the forward path of the modulator loop and ease of implementation. When $B$ is chosen as 1, the entire ADC implemention is much simplified. A 1 bit DAC is truly ideal and so is the feedback path of modulator.

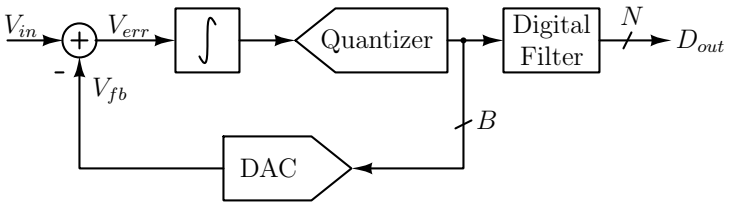



**Figure 2.13:** Architecture of a $\Delta\Sigma$ ADC.

### 2.4.1 Modulator transfer function

The modulator constitutes a nonlinear module, in the form of quantizer, and hence the analysis is quite complex. However, it is easier to arrive at a transfer function when the modulator is represented in Z-domain. For simplicity, a first order low-pass $\Delta\Sigma$ modulator topology is shown in Figure 2.14. $E$ represents the quantization

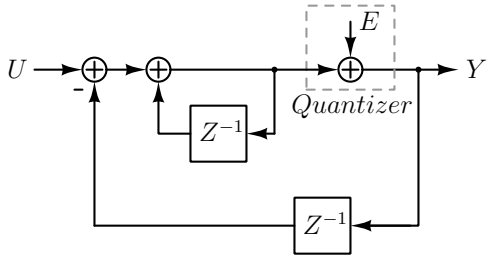



**Figure 2.14:** First order $\Delta\Sigma$ modulator topology.

noise injection to the quantizer, that is assumed linear. Following signal flow graph reduction method, the modulator output is expressed as

$$Y(Z) = U(Z) + (1 - Z^{-1})E(Z) \tag{2.37}$$

The output has two components; a signal transfer function (STF) equal to unity and a noise transfer function (NTF) equal to $[1 - Z^{-1}]$. The signal component is unaltered, whereas the noise is highpass filtered due to presence of the NTF zero at the DC frequency. The inband SQNR is thereby enhanced.

The quantizer in the first order modulator may well be replaced by a copy of modulator itself. In doing so, the NTF order doubles. By recursively replacing the quantizer with modulator a higher order NTF is formed.

$$NTF(Z) = [1 - Z^{-1}]^L \tag{2.38}$$

where $L$ is the NTF order. The frequency response is

$$NTF(f) = \left[2\sin\left(\pi\frac{f}{f_s}\right)\right]^L \tag{2.39}$$

The inband noise power could be written as

$$\overline{V_q^2}_{,inband} = \int_0^{f_b} \rho^2(f) NTF^2 df = \int_0^{f_b} \frac{\Delta^2}{6f_s} \Big[2\sin(\pi \frac{f}{f_s})\Big]^{2L} df \tag{2.40}$$

For a large value of OSR, $\sin(\pi \frac{f}{f_s}) \approx \pi \frac{f}{f_s}$. With that

$$\overline{V_q^2}_{,inband} \approx \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)} \Big[\frac{2f_b}{f_s}\Big]^{2L+1} \approx \overline{V_q^2} \frac{\pi^{2L}}{(2L+1)} \frac{1}{OSR^{2L+1}} \tag{2.41}$$

For a sinusoidal input with a normalized full scale range of -1 to +1, the maximum signal power is $\frac{1}{2}$ and $\Delta = 2/(2^B - 1)$. Therefore the maximum achievable SQNR is given by

$$SQNR_{max} \approx \frac{3}{2} \frac{(2L+1)}{\pi^{2L}} [2^B - 1]^2 OSR^{2L+1} \tag{2.42}$$

When expressed in decibel,

$$SQNR_{max} \approx 10\log_{10}\left(\frac{\frac{3}{2}(2L+1)OSR^{2L+1}}{\pi^{2L}}\right) + 6.02 \times B \tag{2.43}$$

Equation (2.43) leaves three constraints on SQNR, those being, OSR, L and B. Doubling of OSR for a first order modulator gives a 9 dB improvement and for a second order it is 15 dB. An increment by one in modulator order provides a 6 dB improvement. A high OSR with fixed sampling frequency limits the signal bandwidth and a higher modulation order renders the ADC unstable. As a compromise to these issues modulator with a multi-bit quantizer is a better option. SQNR comparison between modulators possessing a single bit versus a multi-bit SAR quantizer is illustrated with the help of graphs shown in Figure 2.15.

The straight line plots show a slope of 9 dB and 15 dB per octave sampling frequency respectively for first and second order modulator having a single bit quantizer, wherein the SQNR enhancement is due to increasing OSR (in this case, the number of clock cycles represented on the x-axis is a direct indicator of the OSR). The other family of curves are obtained by incrementing the quantizer bits, starting from 2 and way up to 12, while the OSR is fixed for each curve at 2, 4 and 8 respectively. The SAR quantizer is assumed to take 1 cycle/bit, due to which the modulator will take conversion clock cycles proportional to quantizer bits, though the OSR is fixed.

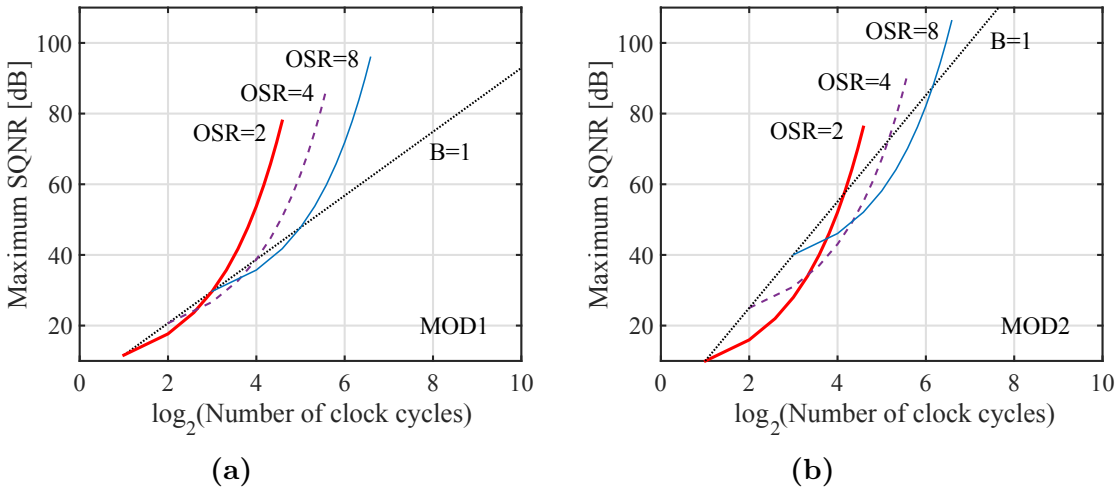



**Figure 2.15:** SQNR comparison between single bit Vs multi-bit SAR quantizer in a $\Delta\Sigma$ modulator for (a) first order and (b) second order.

The plots clearly show that the multi-bit quantizer (low to medium resolution) outperforms single bit quantizer when modulator order is one. However, it takes the quantizer to be of medium resolution and above while the order is two. A multi-bit asynchronous SAR quantizer would fetch much dividends. As a drawback, the DAC now inevitably is multi-bit and the nonlinearity arising out due to the DAC needs to be addressed.

#### 2.4.1.1 Bandpass and Highpass ADCs

A lowpass $\Delta\Sigma$ modulator is converted to a bandpass modulator by replacing the integrator with a resonator. This is equivalent to $Z^{-1} \mapsto -Z^{-2}$ mapping in the Z-domain. Mapping the same in (2.37), the transfer function of the bandpass $\Delta\Sigma$ will be

$$Y(Z) = U(Z) + (1 + Z^{-2})E(Z) \tag{2.44}$$

The NTF now has zeros located at $\pm f_s/4$ instead of the DC frequency and thus the quantization noise is shaped away from the vicinity of $f_s/4$.

A highpass modulator could also be similarly realized by mapping $Z^{-1} \mapsto Z^{-2}$ in (2.37). The transfer function of the highpass modulator will be

$$Y(Z) = U(Z) + (1 - Z^{-2})E(Z) \tag{2.45}$$

The NTF zeroes of the highpass modulator will be located at $f_s/2$ and at DC as well. Quantization noise in the region of half the sampling frequency and DC will be shaped away. Nonetheless the noise shaping at $f_s/2$ is attractive indeed and utilized as highpass $\Delta\Sigma$ modulator. The differences between lowpass, bandpass and highpass modulators are further illustrated in Figure 2.16 and Figure 2.17. Compared to lowpass modulator, other modulators have the advantage of overcoming low frequency noise, such as flicker noise, amplifier offset and clock feedthrough. The bandpass and highpass modulators require double the NTF order for the same noise attenuation as achieved by lowpass. The maximum SQNR for a $2L^{th}$ order ADC is given by

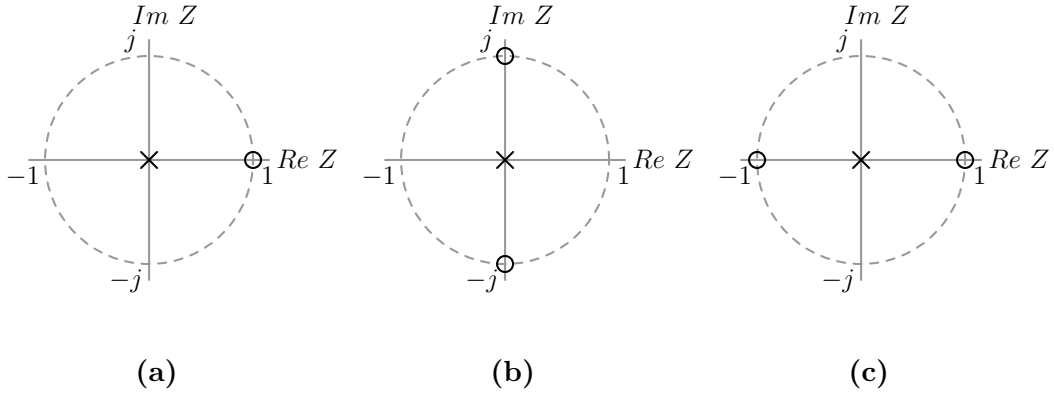



**Figure 2.16:** Pole-Zero plot of the $\Delta\Sigma$ modulator: (a) Lowpass (b) Bandpass and (c) Highpass.

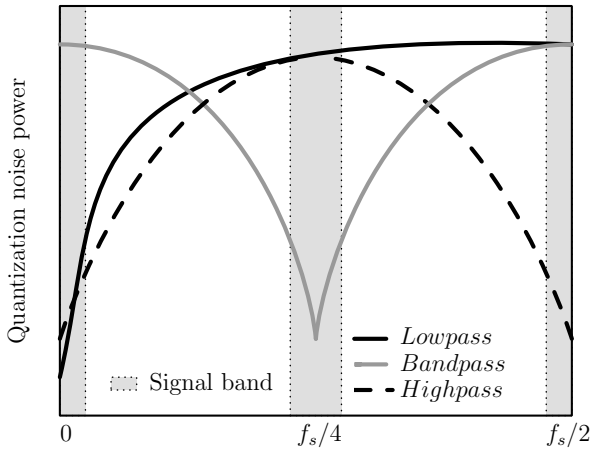



**Figure 2.17:** Quantization noise shaping in $\Delta\Sigma$ modulator.

$$SQNR_{max} \approx 10\log_{10}\left(\frac{\frac{3}{2}(2L+1)OSR^{2L+1}}{\pi^{2L}}\right) + 6.02 \times (B-1) \tag{2.46}$$

## 2.5 SC INTEGRATOR

A SC circuit is often the key element in realization of discrete time signal processing block. The circuit provides accurate voltage gain and integration by switching a sampled capacitor onto an amplifier with a feedback capacitor.

Figure 2.18 shows a simple SC integrator circuit. Charge is sampled onto capacitor $C_1$ during phase $\phi$ and later integrated onto capacitor $C_2$ during $\overline{\phi}$, as illustrated in Figure 2.19. For simplicity the parasitics are not shown. The equivalent average current flowing through $C_1$ is equal to $f_s C_1 V_{in}$. The equivalent resistance $R_{eq}$ is therefore $1/C_1 f_s$. At the end of phase $\overline{\phi}$

$$V_o(n) = V_o(n-1) - \frac{C_1}{C_2}V_{in}(n-1)$$

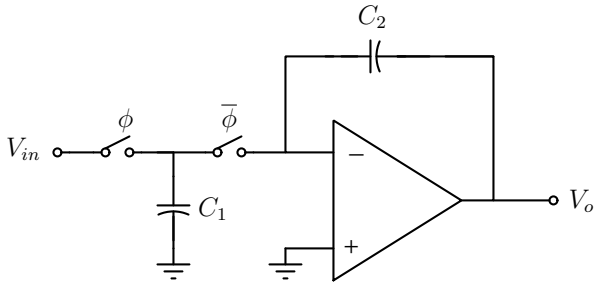


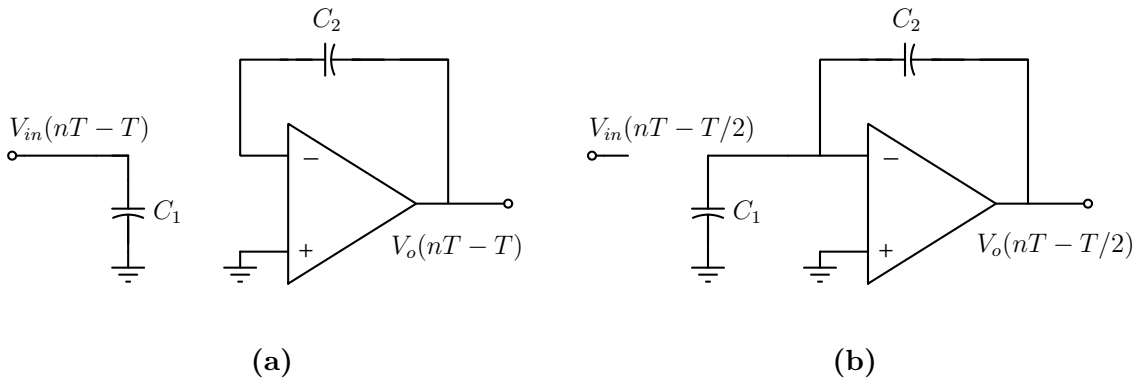

**Figure 2.18:** SC integrator.

Taking Z transformation, the transfer function $H(Z)$ is Allen and Holberg (2002)

$$H(Z) = -\frac{C_1}{C_2}\Big(\frac{1}{Z-1}\Big) = -\frac{C_1}{C_2}\Big(\frac{Z^{-\frac{1}{2}}}{Z^{\frac{1}{2}} - Z^{-\frac{1}{2}}}\Big)$$

Substituting $Z = e^{j\omega T}$ and T being the sampling clock period,

$$H_I(e^{j\omega T}) = -\Big(\frac{C_1}{C_2}\frac{1}{j\omega T}\Big)\Big(\frac{\omega T/2}{\sin(\omega T/2)}\Big)e^{j\omega T/2} \tag{2.47}$$




**(a)** **(b)**

**Figure 2.19:** Integrator circuit operation during (a) $\phi$ phase and (b) during $\overline{\phi}$ phase.

is the ideal transfer function. Since the capacitors could be well matched, the integrator gain is highly accurate. In the presence of finite gain $A_V$, when similarly derived, the actual transfer function is

$$H_a(e^{j\omega T}) = \frac{H_I(e^{j\omega T})}{1 - \frac{1}{A_V}\left(1 + \frac{C_1}{2C_2}\right) - j\left(\frac{C_1/C_2}{2A_V \tan(\omega T/2)}\right)} \tag{2.48}$$

and thus the gain deviation from that of the ideal transfer function gain, defined as gain error, is expressed as

$$gain\ error\ =\ \frac{1}{A_V}\left(1 + \frac{C_1}{2C_2}\right) \tag{2.49}$$

Unity gain frequency and slew rate sets the maximum clocking frequency. In general, the unity gain frequency is set to be 5 times or higher than sampling clock frequency. The nonidealities that could originate in these circuits are due to amplifier finite gain and offset voltage. A large DC gain sets the accuracy of charge transfer and hence the transfer function. Presence of offset reduces the signal swing of the integrator, due to which the DR reduces. The offset has to be sampled and nullified to improve DR.

# Chapter 3

# DUAL UNIT CAPACITOR ARRAY BASED SAR ADC

A SAR ADC with nonbinary weighted dual CA SAR ADC architecture is proposed. In an effort to minimize power dissipation, the CAs adopt passive sharing of charge between capacitors to generate DAC equivalent voltage. In fact, the voltage is generated as a relative difference between output node potential of the two CAs. The binary search algorithm is able to deliver conversion speeds close to the conventional SAR ADC. However, the algorithm is adhoc in nature, and hence the complexity and power dissipation of the ADC are shifted to the control logic. This is conceived as an advantage as the technology and voltage scaling would only benefit the ADC. In this chapter, a low power and area-efficient ADC is targeted. A 0.47 $\mu$W 9 bit 100 kS/s 1 V SAR ADC based on nonbinary weighted dual CA is designed and implemented in a 90 nm CMOS process. The ADC has a small area footprint of size 0.00371 $mm^2$. The ENoB is 8.35 and a FoM of 14.5 fJ/c-s is achieved. The performance of the ADC is validated by simulation.

## 3.1 CONCEPT

Consider two capacitors, $C_{S1}$ and $C_{S2}$, connected to a voltage comparator as shown in Figure 3.1a. The capacitors are charged to input voltages $V_{ip}$ and $V_{im}$. To start with the conversion, a comparison of the input voltages yields the MSB bit. For finding

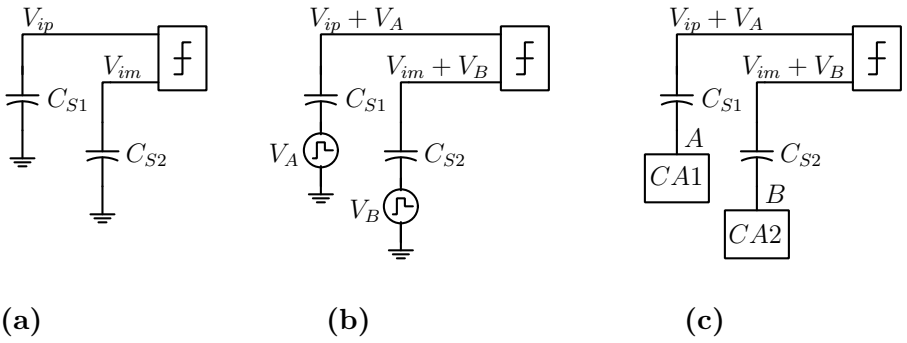



**Figure 3.1:** Illustration of conversion using dual CA. (a) MSB conversion (b) Conversion of remaining bits (c) CAs replacing voltage sources.

the remainder of the conversion bits in subsequent clock cycles, a DAC voltage has to be generated and the same has to be subtracted from the differential input voltage. The net voltage across input terminals of the comparator, say $V_X$, during the $n^{th}$ conversion clock cycle could be expressed as

$$V_X(n) = V_{ip} - V_{im} - V_{DAC}(n) \tag{3.1}$$

As a strategy to realize (3.1), consider placing two voltage sources $V_A$ and $V_B$ below the bottom plates of capacitors as shown in Figure 3.1b. The difference in the source voltages forms the necessary $V_{DAC}$ voltage. Since this voltage is relative, more combination of source voltages of $V_A$ and $V_B$ exists for a given $V_{DAC}$ voltage. For example, if a $V_{DAC}$ of $\frac{V_{DD}}{4}$ is needed, then the sources may have combination of either $(\frac{V_{DD}}{4}, gnd)$ or $(\frac{V_{DD}}{2}, \frac{V_{DD}}{4})$ or many such other possibilities. As an alternative to the voltage sources, circuits that passively share charge between unit capacitors could be used. Figure 3.1c shows the voltage sources being replaced by CA circuits. Each CA houses a few unit capacitors and perform passive sharing of charge between them. The freedom of selection of voltage pairs provides an opportunity to perform conversion along low energy dissipation path without sacrificing speed.

### 3.1.1 Generalized CA

To facilitate efficient switching, parallel operations within CA are supported. Other than sharing of charge between two capacitors, the other capacitors in the CA could

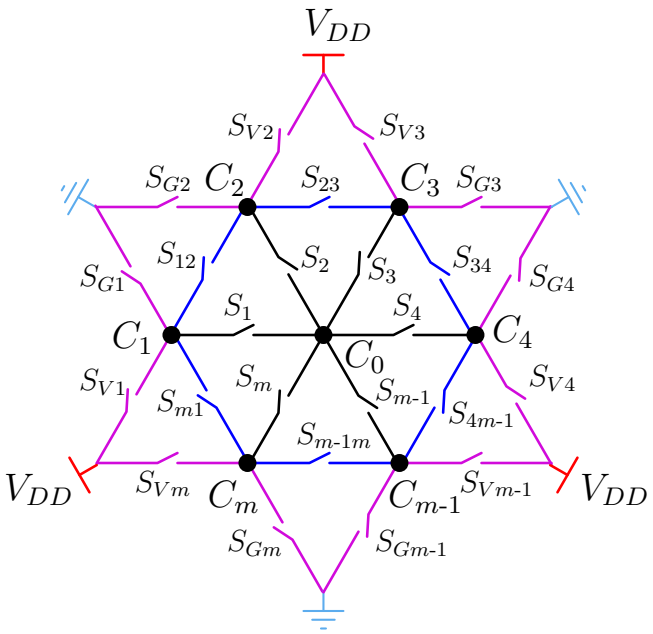



**Figure 3.2:** Generalized architecture of the CA (Capacitor top plates shown as nodes).

involve in either sharing of charge, or charging of full scale reference voltage $V_{FS}$ or discharging to *gnd* voltage. Due to this, both the CA switching energy and the number of clock cycles needed for conversion reduce. Figure 3.2 shows the generalized architecture of CA (Bottom plates of all the unit sized capacitor are assumed to be connected to *gnd*). Central capacitor $C_0$, whose node potential forms the output voltage of CA, connects to peripheral capacitors $(C_1, C_2...C_m)$ through switches $(S_1, S_2...S_m)$. The adjacent peripheral capacitors are connected via switches $S_{ij}$, where $i \neq j$. All capacitors have access to $V_{DD}$ and *gnd* with the help of switches $S_V$ and $S_G$ (not shown for central capacitor). The parasitic at every capacitor top plate is desirably kept small and exclusively made equal so as to reduce its impact during sharing of charge.

## 3.2 ADC ARCHITECTURE

The ADC architecture is shown in Figure 3.3. The capacitor arrays CA1 and CA2 of the ADC are connected to the two terminals of the comparator through respective sample and hold capacitor. The comparator output drives the control logic block, which further controls the switch positions of CAs. With differential inputs, the full

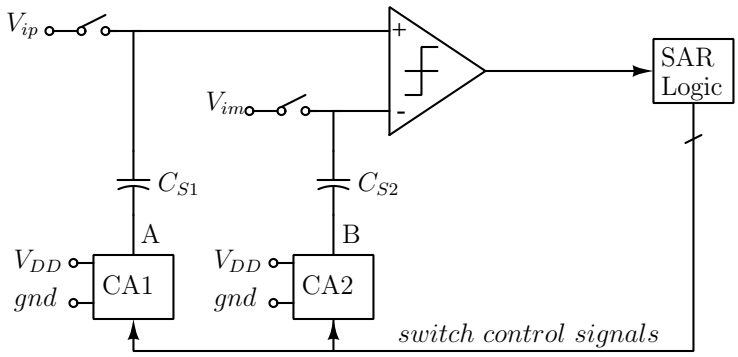



**Figure 3.3:** Architecture of the SAR ADC.

scale voltage $V_{FS}$ seen across the comparator inputs is twice the $V_{DD}$.

### 3.2.1 Illustration

For the purpose of understanding, resolution of 3 bits is considered. The ADC architecture for the same is shown in Figure 3.4, wherein CA components are elaborated. Each CA would comprise three unit capacitors. The conversion completes in 3 clock cycles. The normalized settled voltage across the capacitors and position of relevant switches at these clock cycles is illustrated in Figure 3.5. The nodes $A$ and $B$ respectively represent the output nodes of CA1 and CA2. The output node voltage of every CA is serially added to the respective sample and hold capacitor voltage. The

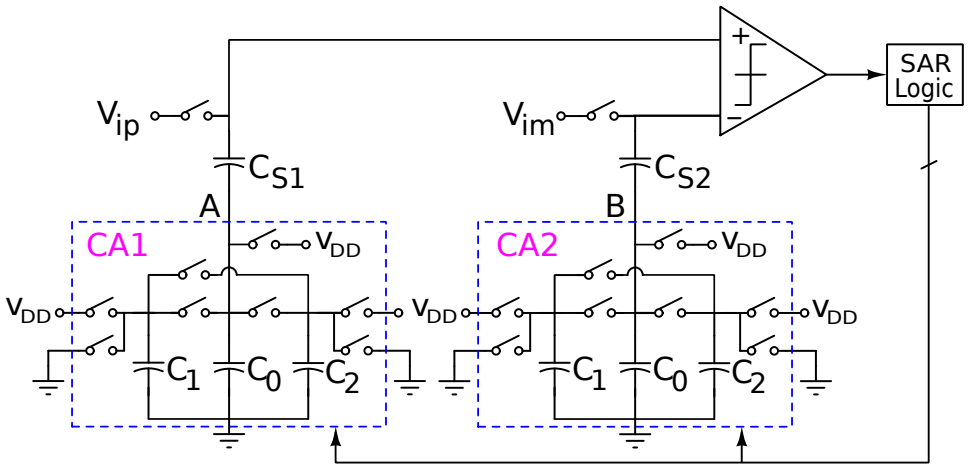



**Figure 3.4:** Example 3 bit SAR ADC architecture.

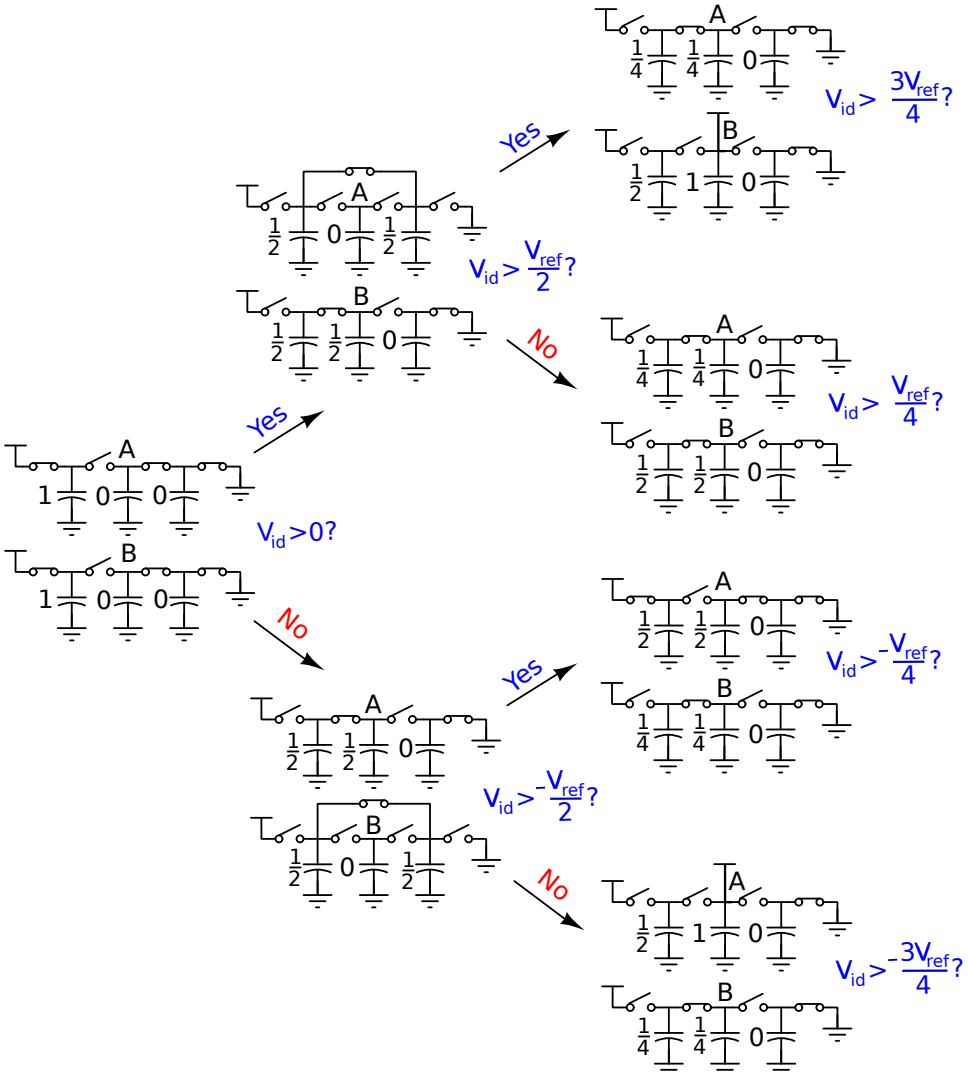



**Figure 3.5:** Illustration of 3 bit SAR ADC.

trial expression at each node of decision tree is also shown in Figure 3.5. Voltage $V_{id}$ is the difference between $V_{ip}$ and $V_{im}$. The comparison of top plate sampled differential inputs provides the MSB early on. If the MSB is logic high, CA2 generates a voltage at its output terminal to track the sampled input voltage. This voltage, however, need not necessarily attain the required DAC equivalent voltage. In the meantime, CA1 provides a level shift to the CA2 output voltage, so as to generate the required DAC equivalent voltage. Hence the two CAs working in coordination avoids unwanted charge sharing steps and clock cycles that would have been in place if the architecture had a single CA. The level shifting voltage generated by CA1 is

halved subsequently until a later phase of conversion is reached, wherein the output voltage of CA2 is just held until the end of conversion. The roles of the CAs are interchaged when MSB is logic low.

### 3.2.2 Conversion algorithm

For ADC resolution of 9 bits, each CA could have four unit capacitors; and in the presented work five is chosen. The additional capacitor will reduce the number of conversion clock cycles (refer subsection 3.3.5). Figure 3.6 and Figure 3.7 together represents binary tree structure of a 9 bit SAR ADC for MSB logic high. The CA output is shown enclosed within the box and the numbers outside the box represents the peripheral capacitor voltages.

In Figure 3.6, transitions shown upwards are for comparator output high and downwards are for comparator output low. In the tree shown, most of the required DAC voltages are generated in a single clock cycle. For few of the DAC voltages generation it requires two clock cycles, and thus clock cycle number 6 holds intermediate voltages. During this cycle comparator is turned $OFF$. Capacitors during clock cycles 9 and 10 continue to hold on to their charges. For the sake of avoiding congestion in the diagram the CA output voltage is alone shown for the last few cycles of conversion. In Figure 3.7, transitions are independent of comparator output until conversion reaches $9^{th}$ clock cycle. Transition to left is for comparator output high and vice versa. Again peripheral capacitor voltages are not shown for the last cycle.

When the MSB is logic low the same tree structure is reused with transition meanings reversed, which is equivalent to swapping the two CAs.

## 3.3 ARCHITECTURE ANALYSIS

### 3.3.1 Accuracy consideration

The CAs have switches connected on top plates of the unit capacitors. These switches add parasitic capacitances to the unit capacitors. The CMOS switches are minimum in size. Equal amount of switch parasitics reside over the unit capacitors. The parasitics within CA do not affect the accuracy in sharing of charge between two unit capacitors, but the comparator input terminal parasitics do. The analysis presented

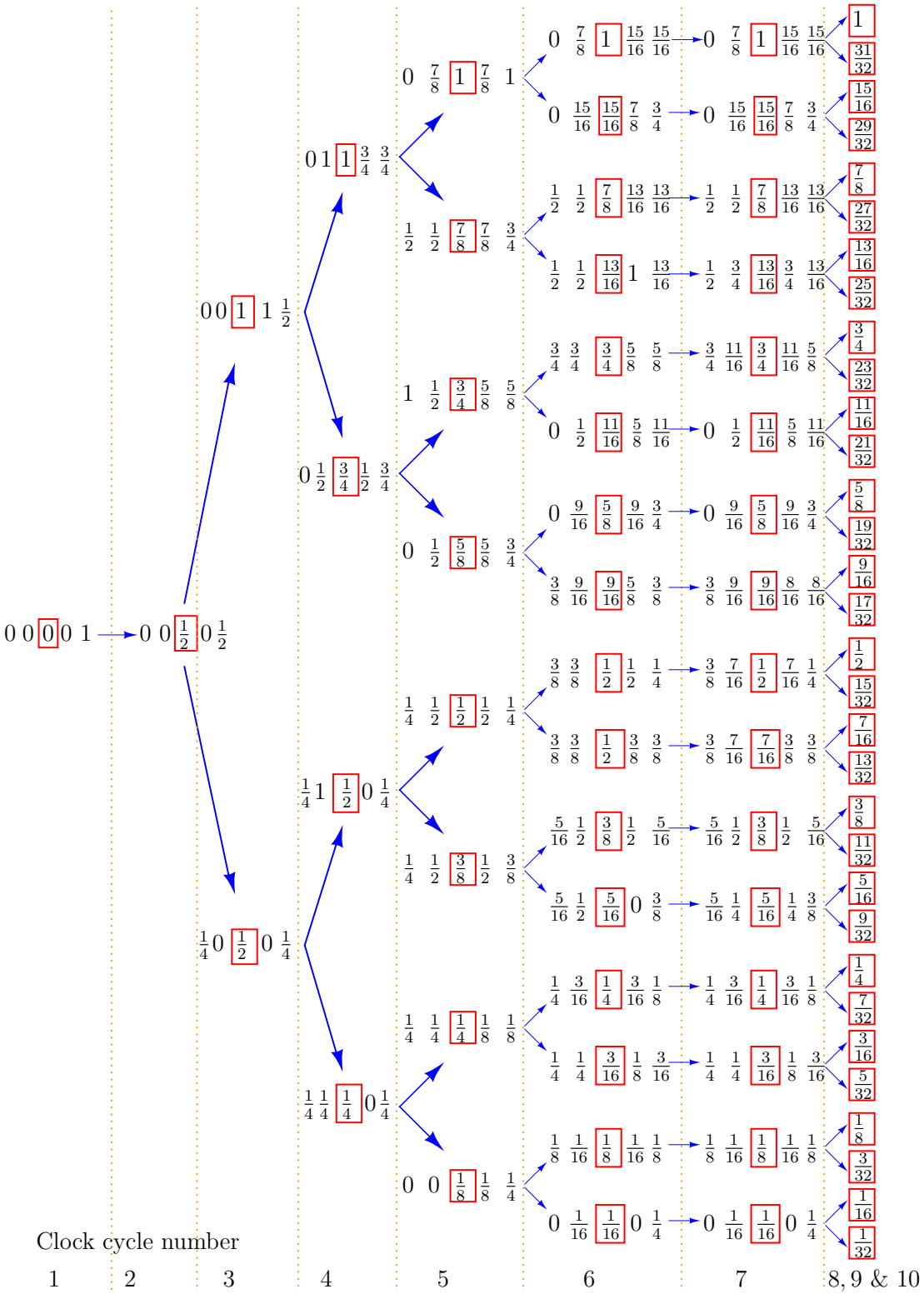



**Figure 3.6:** Binary tree structure describing voltages in CA2 when MSB is logic high. Node voltage at B is shown enclosed in box.

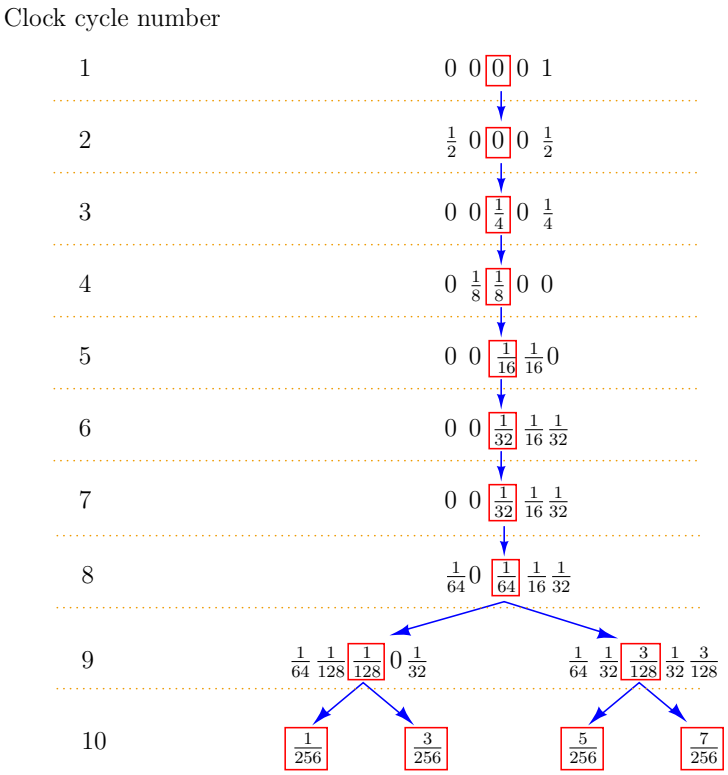
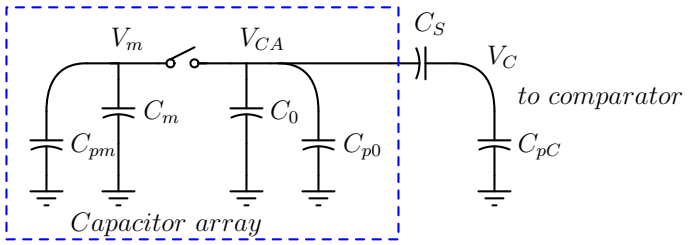



**Figure 3.7:** Binary tree structure describing voltages in CA1 when MSB is logic high. Node voltage at A is shown enclosed in box.

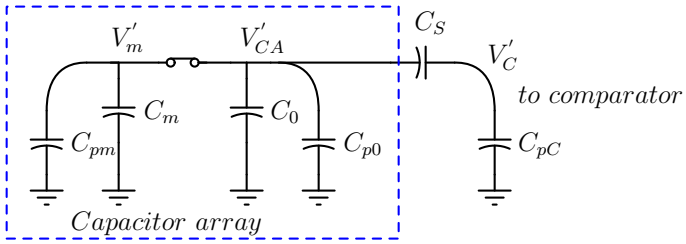
here is limited to static value of these parasitics alone and do not consider the voltage dependency of these parasitics. A simplified model to estimate the error in the generated DAC reference voltage is shown in Figure 3.8. $C_{pm}$ and $C_{p0}$ are the parasitics associated with unit capacitors $C_m$ and $C_0$ respectively. $C_m$ is any peripheral capacitor and $C_0$ is the central capacitor of the CA. The parasitics associated at the nodes are also shown. $C_{pC}$ is the parasitic at comparator input terminal. $V_m$, $V_{CA}$ and $V_C$ are the respective voltages before sharing of charge at top plate of capacitors $C_m$, $C_0$ and $C_{pC}$ (refer Figure 3.8a). The Voltages at the same after sharing of charge be represented as $V'_m$, $V'_{CA}$ and $V'_C$ (refer Figure 3.8b).

Let $q$ and $Q$ respectively represent the charge on a capacitor before and after sharing of charge. By the principle of charge conservation,

$$Q_{pC} + Q_S = q_{pC} + q_s$$




**(a)**




**(b)**

**Figure 3.8:** A model of CA to estimate error due to sharing of charge. (a) Before charing of charge (b) After sharing of charge.

where $Q_{pC}(q_{pC})$ and $Q_S(q_s)$ represent the parasitic and the dominant components of the charge on the capacitor $C_S$ respectively. Similarly,

$$Q_0 + Q_m + Q_{p0} + Q_{pm} - Q_S = q_0 + q_m + q_{p0} + q_{pm} - q_s$$

The voltage $V'_C$ across the capacitor $C_{pC}$ after sharing of charge is given by,

$$V'_C = \frac{Q_{pC}}{C_{pC}} = \frac{Q_S}{C_S} + (\frac{Q_0 + Q_p + Q_{pm} + Q_{p0}}{C_0 + C_m + C_{p0} + C_{pm}})$$

$$\frac{Q_{pC}}{C_{pC}} = \frac{q_{pC} + q_S - Q_{pC}}{C_S} + (\frac{q_0 + q_m + q_{p0} + q_{pm} + q_{pC} - Q_{pC}}{C_0 + C_m + C_{p0} + C_{pm}})$$

$$Q_{pC}(\frac{1}{C_{pC}} + \frac{1}{C_S} + \frac{1}{C_0 + C_m + C_{p0} + C_{pm}}) = \frac{q_{pC} + q_S}{C_S} + (\frac{q_0 + q_m + q_{p0} + q_{pm} + q_{pC}}{C_0 + C_m + C_{p0} + C_{pm}})$$

$$Q_{pC}(\frac{1}{C_{pC}} + \frac{1}{C_S} + \frac{1}{C_0 + C_m + C_{p0} + C_{pm}}) = \frac{C_{pC}V_C}{C_S} + (V_C - V_{CA}) + (\frac{q_0 + q_m + q_{p0} + q_{pm} + C_{pC}V_C}{C_0 + C_m + C_{p0} + C_{pm}})$$

$$\frac{Q_{pC}}{C_{pC}} = V'_C = V_C - (V'_{CA,ideal} - V_{CA})G \tag{3.2}$$

where $V'_{CA,ideal}$ is the intended CA output voltage due to charge sharing, expressed as

$$V'_{CA,ideal} = \frac{q_0 + q_m + q_{p0} + q_{pm}}{C_0 + C_m + C_{p0} + C_{pm}}$$

and

$$G = \frac{1}{C_{pC}(\frac{1}{C_{pC}} + \frac{1}{C_S} + \frac{1}{C_0+C_m+C_{p0}+C_{pm}})}$$

Voltage $(V'_{CA,ideal} - V_{CA})$ is the desired change in voltage after sharing of charge, which is never achieved due to presence of the comparator input terminal parasitic.

Also, the voltage $V'_{CA}$ across the capacitor $C_0$ after sharing of charge could be expressed as

$$V'_{CA} = \frac{Q_0 + Q_m + Q_{p0} + Q_{pm}}{C_0 + C_m + C_{p0} + C_{pm}}$$

$$V'_{CA} = \frac{q_0 + q_m + q_{p0} + q_{pm}}{C_0 + C_m + C_{p0} + C_{pm}} + \frac{q_{pC} - Q_{pC}}{C_0 + C_m + C_{p0} + C_{pm}}$$

Using the result from (3.2),

$$V'_{CA} = V'_{CA,ideal} + \frac{q_{pC} - [q_{pC} - (V'_{CA,ideal} - V_{CA})GC_{pC}]}{C_0 + C_m + C_{p0} + C_{pm}}$$

$$V'_{CA} = V'_{CA,ideal} + \frac{(V'_{CA,ideal} - V_{CA})GC_{pC}}{C_0 + C_m + C_{p0} + C_{pm}} \tag{3.3}$$

The error voltage $e_{CA}$ at the output terminal of the CA is therefore

$$e_{CA} = \frac{(V'_{CA,ideal} - V_{CA})GC_{pC}}{C_0 + C_m + C_{p0} + C_{pm}} \tag{3.4}$$

The deviation in voltage from the desired voltage at the comparator input terminal, $e_C$ could be written as

$$e_C = V_C - (V'_{CA,ideal} - V_{CA})G - (V_C - V_{CA} + V'_{CA,ideal})$$

$$e_C = (V'_{CA,ideal} - V_{CA})(G - 1) \tag{3.5}$$

The error voltages derived in (3.4) and (3.5) are dependent on the comparator input terminal parasitic and change in potential at the output node of CA. With $G < 1$, the error voltages computed in (3.5) and (3.4) have opposite signs, thus indicating the error correction to occur as the conversion progress. The output voltage across the capacitor $C_0$ may attain value ranging from $0 - V_{DD}$ (which is half the full scale voltage). The maximum value of $(V'_{CA,ideal} - V_{CA})$ is $\frac{V_{DD}}{2}$ and happens during the first incidence of charge sharing between central and peripheral capacitors in CA. For further sharing of charge, during remainder of clock cycles, the voltage $(V'_{CA,ideal} - V_{CA})$ reduces by factor of 2 with every cycle. Thus the worst case accumulated error (in terms of LSB) at any of the comparator input terminal, towards the end of conversion, is

$$k = -\frac{V_{DD}}{V_{FS}}(G-1)$$

$$k = -2^{N-1}(G-1) \tag{3.6}$$

By analyzing the expression for $G$, the size of capacitor $C_S$ is chosen much larger than $C_{pC}$. Oversizing of $C_S$, much above twice the size of $C_u$, is insignificant for improving the value of $G$. Considering capacitor $C_S$ to be twice the size of $C_u$, $G$ could be expressed as

$$G = \frac{1}{1 + \frac{C_{pC}}{C_u}}$$

Substituting for $G$ in (3.6), the size of unit capacitor to lend error voltage of $k$ times LSB is thus given as,

$$C_u \simeq (\frac{2^{N-1}}{k} - 1)C_{pC} \tag{3.7}$$

For a given resolution and foundry technology, (3.7) relates the size of unit capacitor to the comparator input terminal parasitic.

### 3.3.2 Noise in CA

Central capacitor $C_0$ and peripheral capacitor $C_m$ share the charge through a switch. The equivalent mean square thermal noise voltage before sharing of charge are respectively $v_{nC0}$

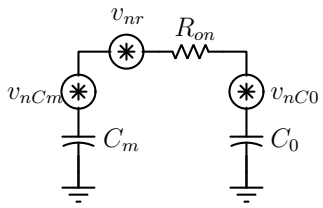



**Figure 3.9:** Noise model of the CA.

and $v_{nCm}$. Considering $R_{on}$ as the $ON$ state switch resistance, the added mean square thermal noise voltage during charge sharing to each of charge sharing capacitor is $kT/2C_u$, represented by a noise source $v_{nr}$. The aquired mean square noise on capacitor $C_0$ after $n$ times sharing of charge with peripheral capacitors is expressed as

$$\overline{v^2}_{nC0}[n] = \frac{\overline{v^2}_{nC0}[n-1] + \overline{v^2}_{nCm} + kT/C_u}{2} \tag{3.8}$$

Due to sampling of the supply voltage sources, the noise sources are initialized to $kT/C_u$. For value of $n$ is as large as resolution bits of the ADC. Following (3.8) the mean square noise voltage aquired by $C_0$ at the end of conversion reaches $2kT/C_u$. Generally, in the presented algorithm, the charge shared capacitors $C_0$ and $C_m$ are held together during comparison. As a result the equivalent noise at the CA output node is reduced to $kT/C_u$.

The sampling capacitors being twice the size of unit capacitors in CA, the total mean square noise voltage in the DAC is $3kT/C_u$.

Equating thermal noise power to quantization noise power, as done in (2.11), the minimum size of unit capacitors of the CA is

$$C_u = 36kT\frac{2^{2N}}{V_{ref}^2} \tag{3.9}$$

### 3.3.3 Capacitor mismatch

The presence of mismatch causes accumulation of error charges in CAs. For the sake of capacitor mismatch analysis, assume that the central capacitor of one of the CAs and peripheral capacitors of the other are larger compared to the rest of capacitors in CAs. The normalized capacitance value of larger being $1+\alpha$ and the smaller $1-\alpha$. The term $\alpha \ll 1$

and is equal to $\frac{\sigma_u}{C_u}$. The differential nature of the ADC architecture may reduce the net charge error, however, the assumption necessarily adds these error charges. The maximum of error is presented when output code is close to extreme.

As per the assumption, central capacitor of CA2 and peripheral capacitors of CA1 are considered larger than the rest of the capacitors in CAs. For an N bit ADC, the number of times the central capacitor sharing charge with peripheral capacitors is assumed to be N. It is further assumed that the central capacitor share charge with peripheral capacitor, which are always either precharged to $V_{DD}$ or discharged to *gnd*. Towards the end of conversion, the output voltage of one of the CAs will settle close to LSB, while the other will settle close to an absolute value of differential input $V_{id}$. For output codes closer to extreme, say 111..., CA2 experiences positive and CA1 experiences negative charge errors (refer to Figure 3.6 and Figure 3.7; charge error correction due to central capacitor of CA2 charging with supply rail is neglected). Here $q$ is the desired initial charge in the unit capacitors. The charge on central capacitor of CA2 during $i^{th}$ clock cycle is expressed as

$$q_i = \big(\frac{q_{i-1} + q(1-\alpha)}{2}\big)(1+\alpha) \tag{3.10}$$

Initial charge during first clock cycle $q_1 = 0$ in CA2. Similarly, the charge on central capacitor of CA1 during $i^{th}$ clock cycle will be

$$q_i = \big(\frac{0 + q(1+\alpha)}{2}\big)(1-\alpha) \tag{3.11}$$

In case of CA1, the initial charges $q_1 = q_2 = 0$. Table 3.1 shows the charge held by various capacitors of CAs for the mentioned code. Higher order terms of $\alpha$ are ignored since $\alpha \ll 1$. When $i = N$, the conversion completes. the maximum error voltage $\varepsilon_{max}$ due to mismatch could be expressed as difference between last terms of the two sequences. This could be simplified as,

$$|\varepsilon_{max}| = \frac{q\alpha}{2^{N-1}}\Big[(2^{N-1} - N) + (N-3)\Big] = \frac{q\alpha}{2^{N-1}}\Big[(2^{N-1} - 3)\Big] \tag{3.12}$$

For larger values of N, $|\varepsilon_{max}| \simeq q\alpha$. Upon substitution of $\alpha = \frac{\sigma_u}{C_u}$, (3.12) could be denoted

**Table 3.1:** Charge held by unit capacitors during charge sharing phase for output code 111...

| Clock | Charge held by | | | |
|---|---|---|---|---|
| | $C_0$ of CA2 | $C_m$ of CA2 (before sharing) | $C_0$ of CA1 | $C_m$ of CA1 (before sharing) |
| 1 | 0 | $q(1-\alpha)$ | 0 | $q(1+\alpha)$ |
| 2 | $\frac{q}{2}$ | $q(1-\alpha)$ | 0 | $q(1+\alpha)$ |
| 3 | $q(\frac{3+\alpha}{4})$ | $q(1-\alpha)$ | $(\frac{q}{4})$ | $q(1+\alpha)$ |
| 4 | $q(\frac{7+4\alpha}{8})$ | $q(1-\alpha)$ | $q(\frac{1-\alpha}{8})$ | $q(1+\alpha)$ |
| 5 | $q(\frac{15+11\alpha}{16})$ | $q(1-\alpha)$ | $q(\frac{1-2\alpha}{16})$ | $q(1+\alpha)$ |
| . | . | . | . | . |
| . | . | . | . | . |
| N | $\frac{q}{2^{N-1}}[2^{N-1}-1+(2^{N-1}-N)\alpha]$ | | $\frac{q}{2^{N-1}}[1-(N-3)\alpha]$ | |

as,

$$\frac{|\varepsilon_{max}|}{V_{ref}} \simeq 0.5\frac{\sigma_u}{C_u} \tag{3.13}$$

The above equation represents the relation between the conversion accuracy and the capacitance mismatch. The matching result is inline with results in Suarez et al. (1975). With modern technology foundries been able to provide well matched capacitors, the obtained result assures good conversion accuracy. Assuming $|\varepsilon_{max}|$ to be $k$ times LSB, (3.13) could be simplified to

$$\frac{\sigma_u}{C_u} \simeq \frac{k}{2^{N-1}} \tag{3.14}$$

### 3.3.4 Unit capacitor size

The relations to express the minimum size of unit capacitor are given by (3.7), (3.9) and (3.14). $V_{ref}$ of 1 V, $k$ equal to 0.5 LSB and $N$ equal to 9 yields are used for unit capacitance requirement evaluation. The minimum value of unit capacitor is 39 fF when noise limited. $\frac{\sigma_u}{C_u}$ is 0.2%, suggesting that the unit capacitance value is in few tens of fF for a 90 nm technology node. For the same technology, the gate parasitic of a minimum sized MOS device is around 0.25 fF. On substitution in (3.7), the unit capacitor size requirement is 128 fF. This value being largest amongst the three estimates, is the minimum value of

unit capacitor of the CA. The value when compared to a unit capacitor of BWCA based traditional SAR ADC is large. However, the matched binary capacitors in traditional SAR ADCs are highly complicated to route and occupy large space in order to provide sufficient isolation between capacitors, resulting in poor overall capacitance density. Whereas, the nonbinary capacitors in our ADC, which are few in number, offer lesser complexity in routing and maintain excellent overall capacitance density. This results in CA occupying a small area on a chip.

### 3.3.5 Trade off

For $m$ number of capacitors in CA1 and $n$ number in CA2, $m+n$ voltages could possibly appear simultaneously (including the supply voltage $V_{DD}$ available with each CA) within the CAs after charge sharing. These $m+n$ voltages assist in executing the binary search algorithm, leading to $m+n$ bit resolution (true for $m$ *and* $n > 2$). An additional bit in resolution (the MSB) is obtained due to top plate sampling of differential inputs. Therefore the resolution is given by

$$N = m + n + 1$$

For a resolution of $N$ bits the total capacitance required is given by

$$C_{total} = (m+n)C_u + 2C_S$$

$$C_{total} = (N+3)C_u \tag{3.15}$$

The above equation dictates the minimum number of required unit capacitors. However, few more unit capacitors could be added to the CAs in an effort to reduce the number of conversion clock cycles.

Figure 3.10 shows the relation between the number of clock cycles and resolution. The algorithm is adhoc (in the interest of low power dissipation and higher conversion speed), and as a proof, only selected resolutions are considered. $m$ and $n$ are selected equal; for resolution of 7, 9 and 11, the number of unit capacitors in each CA are 3, 4 and 5 respectively. The presence of 5 unit capacitors is capable of 11 bit resolution. However, when targeted

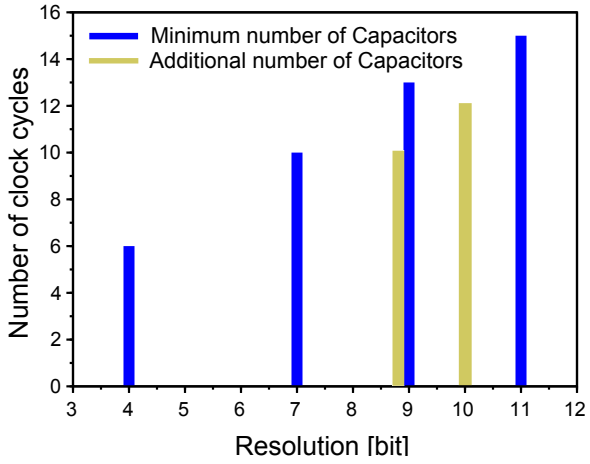



**Figure 3.10:** Requirement of conversion clocks against desired resolution.

resolution is relaxed to 10 bits, the required number of conversion clock cycles reduce from 15 to 12. In the plot shown, a 9 bit resolution is also achieved by using 5 unit capacitors in each CA and the required conversion clock cycles is 10. Thus emphasizing the speed, resolution, and area tradeoff.

The introduction of additional unit capacitors inside CA contributes to additional voltage levels. This enhances parallel operations in CAs to attain the required DAC equivalent voltage in fewer clock cycles. Hence, the required number of clock cycles for conversion are reduced and can be close to the number of cycles needed in a traditional SAR ADC. On the downside, the CA area slightly increases. Addition of a unit capacitor to CA would add few more switches, typically 2 to 4 in number. However, the control logic complexity need not necessarily increase.

### 3.3.6 Energy consumption estimate

#### 3.3.6.1 CAs

Plot of normalized energy consumption in CAs against output code for the presented 9 bit ADC is shown in Figure 3.11. The energy consumption is computed by taking into account the charging of unit capacitors while traversing through the binary tree shown in Figure 3.6 and Figure 3.7. The average energy consumption estimate is 3.42 $C_u V_{DD}^2$. By substituting

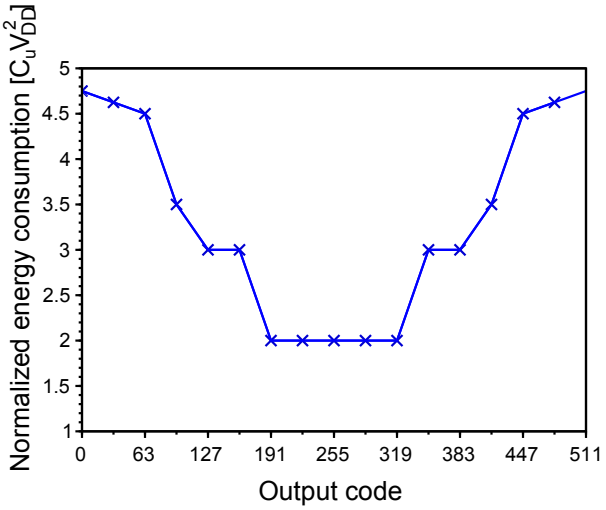



**Figure 3.11:** Energy consumption estimation of the CA.

the design values, this average energy amounts to 0.43 pJ. The value would reduce further if the residue charge left from the previous conversion cycle is also considered. As compared to the total energy consumption of the ADC, the energy consumption by the CAs is minimal.

#### 3.3.6.2 SAR control unit

The controller has two sections, namely, a sequential logic and a combinational logic block. The sequential block, as described in Figure 3.14, will have $N + 2$ D-type flip-flops (DFF) clocked at any given clock interval. Each DFF possess 4 inverter and 4 pass transistors amounting to an equivalent of $8C_{inv}$ capacitance load. Hence the energy consumed in sequential circuit is

$$E_{seq} = 8(N + 2)C_{inv}V_{DD}^2 \tag{3.16}$$

For a resolution of N bits, roughly it takes $\frac{N}{2}$ number of unit capacitors. The required number of switches in each CA will be $4(\frac{N}{2}) - 2$. The sum of number of binary input variables to the combinational logic circuit due to sequencer and data register is roughly $2N$. Given the number of binary inputs, Jukna (2012) provides an estimation of a minimum number of 2 input logic gates required in realization of Boolean function; for an N binary inputs, minimum number of gates required is $2N - 4$. While the combinational logic circuit for switching operations for one of the CAs require $2N$ binary input variables, the other

requires approximately $N$ (since this CA's output is independent of output code until last two clocks). The energy consumed in combinational logic circuit is

$$E_{combi} = (4\frac{N}{2} - 2)\big[(4N-4) + (2N-4)\big]2C_{inv}V_{DD}^2\alpha \tag{3.17}$$

where $\alpha$ is the average activity factor of the combinational circuit.

The total energy consumption of the ADC is energy consumption due to CAs, control logic and comparator, whose power consumption is provided by (2.33).

$$E_{tot} = 2C_{inv}V_{DD}^2\big[12N^2 - 28N + 16\big]\alpha + 8(N+2)C_{inv}V_{DD}^2 + 3.42\ C_uV_{DD}^2 + E_{comp} \tag{3.18}$$

Using (3.7) and k=0.5,

$$E_{tot} \approx 2C_{inv}V_{DD}^2\big[(12N^2 - 28N + 16)\alpha + 4(N+2) + 3.42\ 2^{N-1}\big] + E_{comp} \tag{3.19}$$

A normalized total energy plot for different values of $\alpha$ is shown in Figure 3.12.

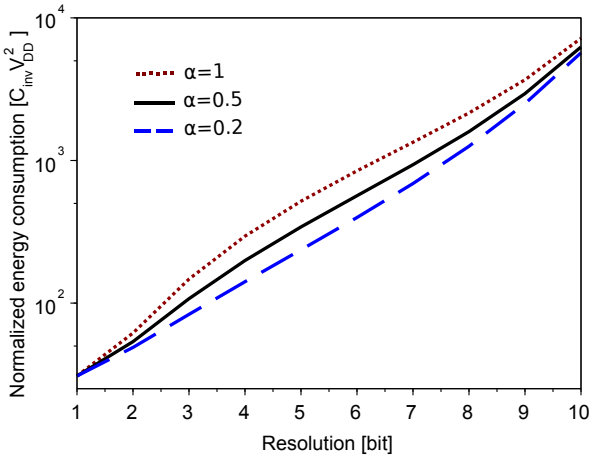



**Figure 3.12:** Normalized total energy consumption estimation of the ADC.

## 3.4 IMPLEMENTATION

A 9 bit SAR ADC is implemented. As discussed in the previous subsection, $m+n$ is chosen to be equal to 10. Each of the CAs has five unit capacitors. The CAs are designed to be identical so that switch control signals for the CA could be swapped between the two based on the MSB. Doing so, the CAs could exchange their roles, thereby reducing the combinational logic circuit complexity of the controller to nearly 50%.

Transmission gate with minimum size transistors is used as a switch between capacitors. As long as the channel charge injected to the capacitors are same, the capacitor voltages are accurate. However, the charge splitting in individual transistors is a complex mechanism and may not see equal charge exiting through source and drain nodes. By maintaining equal impedance at either end of the switch, a probability of having equal charge splitting can be expected. Switches connected to supply source may have different impedances at their ends and therefore sized accordingly to reduce the channel charge injection error. The input voltage sampling switches are bootstrapped, as in Abo and Gray (1999).

A dynamic two stage latched comparator (van Elzakker et al., 2010) is preferred for comparison of voltages. Since the parasitics at the input terminals of the comparator influence the CA size, a minimum size is chosen for transistors connecting to these terminals. The smaller transistor size minimizes the comparator kickback. But as a demerit would show a large mismatch between transistor devices. The comparator could be carefully laid out to reduce the mismatch. The presence of the mismatch, however, leads to an offset voltage that reduces dynamic range alone without sacrificing ADC linearity. Comparator kickback is further reduced by oversizing the discharge capacitors of the comparator. The common mode input voltage of the comparator remain greater than $\frac{V_{DD}}{2}$, due to which the input transistors of the comparator operate more linearly. The gain of pre-amplifier is close to 5 for the bandwidth assigned.

The plot of parasitics at the CA output node and comparator input terminal for various process corners is shown in Figure 3.13. The usage of transmission gate based switches reduces the parasitic variation at CA output node. The maximum variation in the total parasitic capacitance at charge sharing nodes of CA is found to be close to 0.1 fF (refer

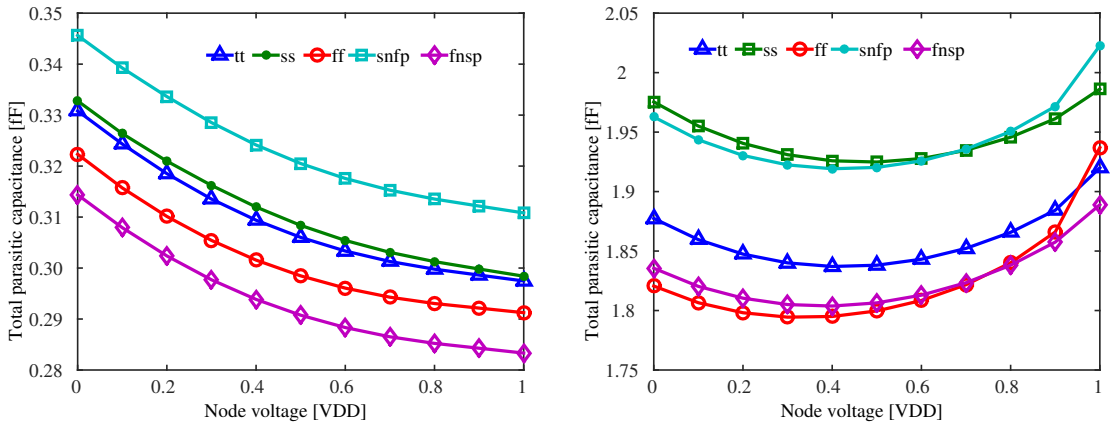



**Figure 3.13:** Voltage dependent parasitics for various process corners at (a) comparator input terminal (b) CA output terminal.

Figure 3.13b). This variation in parasitic capacitance is small and therefore the sharing of charge between unit capacitors is minimally affected. The parasitics at comparator input terminal $C_{pC}$ is voltage dependent. The voltage dependency reduces for higher values in voltage. The common mode input voltage of the comparator, remaining greater than $\frac{V_{DD}}{2}$, reduces the parasitic capacitance variation to value less than 0.01 fF (refer Figure 3.13a). This voltage dependent variation in capacitance of parasitic is 3% to its nominal value, but will not pose any threat to linearity of the ADC. This is due to the fact that both the terminals of the comparator have similar parasitics and any voltage error arising will treated as common mode error and will get cancelled by the differential nature of the comparator.

Going by the discussion in subsection 3.3.4, the size of the unit capacitor is chosen to be 128 $f$F.

The binary tree structure presented in Figure 3.6 and Figure 3.7 is nothing but a finite state machine. While the binary output bits and clock forms the state and state input variables, the switch control signals are state output variables. The state output variables are expressed as Boolean functions, preferably in sum-of-products form.

The control logic circuit constitutes a simpler sequencer and data register, combinational logic gates and control signal swapping circuits. Figure 3.14 shows the sequencer and data register. The circuit is similar to the one presented in Anderson (1972). The sequencer

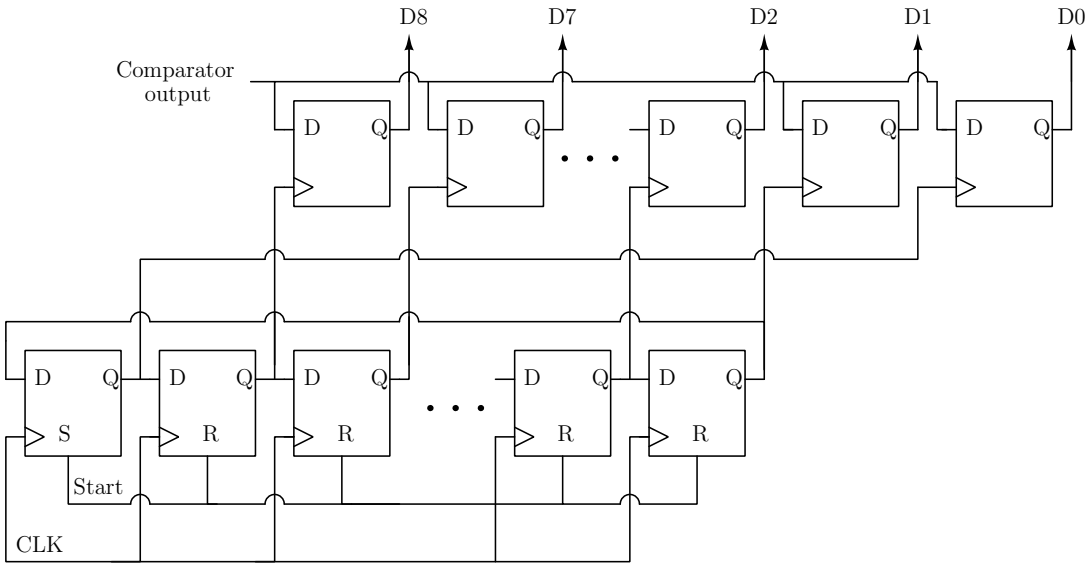



**Figure 3.14:** Circuit diagram of the sequencer and data register.

is a circular shift register, the purpose of which is to right shift logic high for every rising clock edge. The 9 bit ADC takes 10 clock cycles for conversion and hence the sequencer constitutes 10 static DFF. Towards the end of every clock cycle, except for the $6^{th}$, the output of the sequencer enables a D flip-flop of the data register to acquire the comparator output bit. The comparator has no valid output bit towards the end of $6^{th}$ clock cycle (refer Figure 3.6 and Figure 3.7). Total of 93 logic gates make up the combinational circuit, wherein 58% of logic gates are 2 input AND gates. To minimize power consumption, these AND gates are implemented using pass transistors as shown in Figure 3.15a. The other gates are implemented using static CMOS inverter, NAND, NOR, AOL logic gates. In all cases the fan-in and fan-out for the logic gates do not exceed four. The switch control signals are allowed to be swapped between the CAs with the help of multiplexers. The multiplexer circuit is shown in Figure 3.15b. A static CMOS logic style is preferred over a pass transistor logic. This allows the switch control signals to be buffered and also level shifted if desired. $a$ and $b$ are the switch control signals passed on to the swapping circuit, while $\overline{X}$ and $\overline{Y}$ are the complementary outputs. When the $MSB$ is logic low, swapping of signals takes place. The outputs of the swapping circuit are gated with the help of $CLK$. The ADC is implemented using UMC 90nm technology library. The laid out design occupies

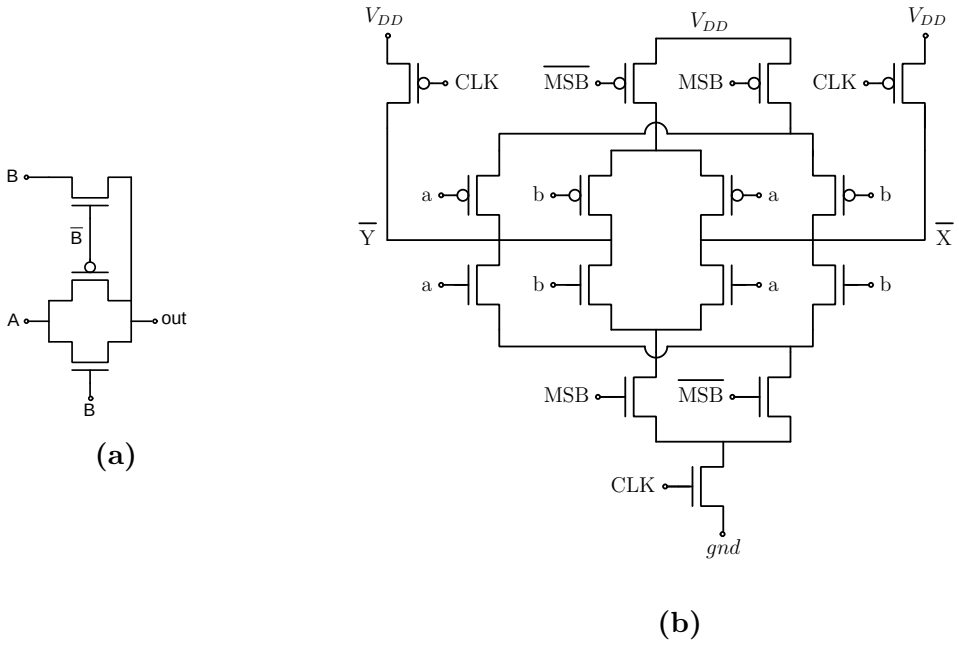



**Figure 3.15:** Circuit diagram of (a) Pass transistor based AND gate circuit (b) Control signal swapping circuit.

an area of 0.00371 $mm^2$ and is shown in Figure 3.16.

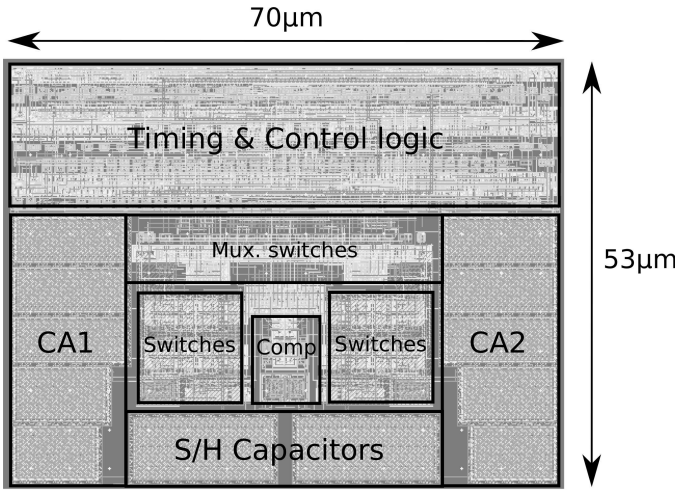



**Figure 3.16:** Layout of ADC core.

## 3.5 SIMULATION RESULTS

The 9 bit ADC operates at 1 V supply voltage. A netlist is generated by post layout extraction for simulation requirements. The complete ADC power consumption is 473 $n$W at sampling frequency of 100 KHz. Noise bandwidth for simulations is 50 times the sampling frequency.

### 3.5.1 Linearity test of the ADC

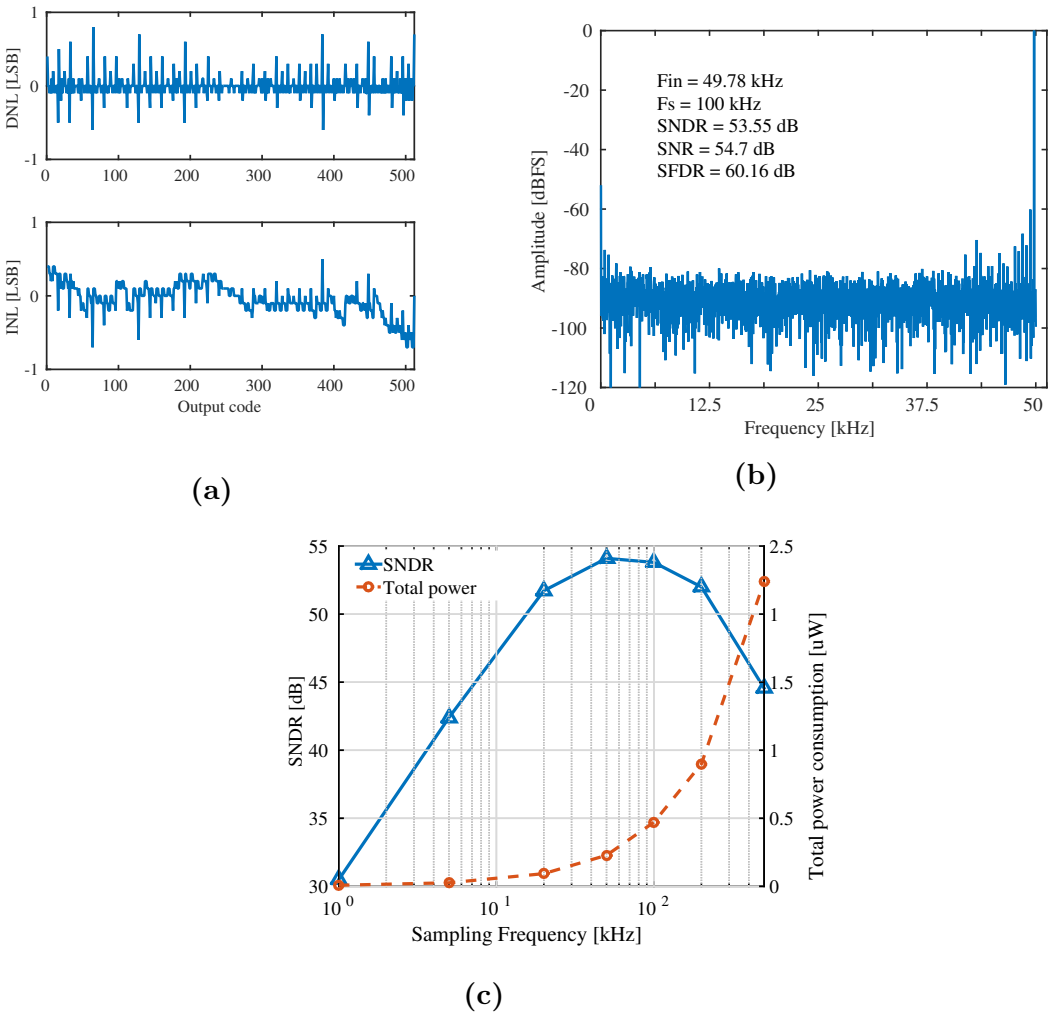



**Figure 3.17:** Plot of (a) Differential and integral nonlinearity (b) FFT spectrum (c) SNDR and total power consumption vs Sampling frequency.

**Table 3.2:** ADC performance summary

| ADC Performance | | |
|---|---|---|
| Technology | | 90 nm CMOS |
| Core area ($mm^2$) | | 0.00371 |
| Supply voltage (V) | | 1 |
| Differential input range (V) | | 2 |
| Resolution (bit) | | 9 |
| Sampling rate (kS/s) | | 100 |
| DNL (LSB) | | +0.8/-0.6 |
| INL (LSB) | | +0.5/-0.7 |
| SNDR [at Nyquist](dB) | | 53.55 |
| SFDR [at Nyquist](dB) | | 60.16 |
| ADC Power Breakdown | | |
| Supply voltage (V) | | |
| DAC, Comparator | 1.0 | 1.0 |
| SAR | 1.0 | 0.7 |
| Comparator (nW) | 83 | 83 |
| SAR logic (nW) | 287 | 113 |
| Swapping (nW) | 103 | 321 |
| Total power (nW) | 473 | 517 |

The static performance of the ADC is shown in Figure 3.17a. Absolute values of both the static nonlinearities are limited below 1 LSB. The dynamic performance of the ADC is verified at its Nyquist input frequency. The spectral simulation is shown in Figure 3.17b. The SNDR of the ADC is found to be 53.55 dB for the typical Process corner. Owing to good linearity characteristics of the ADC, the distortion power component is close to 1 dB.

Table 3.2 summarizes the performance of the ADC at typical process corner. The power consumption of the SAR block does not scale down when the supply voltage is reduced. This is due to poor performance of the control signal swapping circuits. The circuits have vertically stacked transistors and hence suffer from poor rise time and fall time at reduced supply voltage. The supply voltage is varied by ±20%. The power consumption breakdown

**Table 3.3:** ADC performance under varied supply voltage

| $V_{DD}$ | 0.8 | 1.0 | 1.2 |
|---|---|---|---|
| Sampling frequency (kHz) | 20 | 100 | 100 |
| Total power (nW) | 59 | 473 | 665 |
| ENoB @ Nyquist (bit) | 7.9 | 8.6 | 8.8 |
| FoM (fJ/c-s) | 12.6 | 12.2 | 14.8 |

and the performance are recorded in Table 3.3.

Figure 3.17c shows the plot of SNDR and total power consumption of the ADC against the sampling frequency. The input frequencies are chosen close to satisfy Nyquist sampling rate. The power consumption is linearly related to $f_s$. The SNDR reduces at higher sampling frequencies due to capacitor coupling effect. As the sampling frequency is reduced, the leakage current dominates the conversion accuracy (refer (2.8)). This leakage current occurs simultaneously for all the unit capacitors and throughout the conversion cycles. The leakage current depends on capacitor voltages and hence code dependent. Increased charge leakage from the unit capacitors causes SNDR to drop at lower frequencies.

To verify the ADC performance against capacitor mismatch and process variations Monte Carlo simulations of 200 runs are carried on the extracted netlist. The static non-linearity curves are plotted as shown in Figure 3.18a. The nonlinearity is more towards the

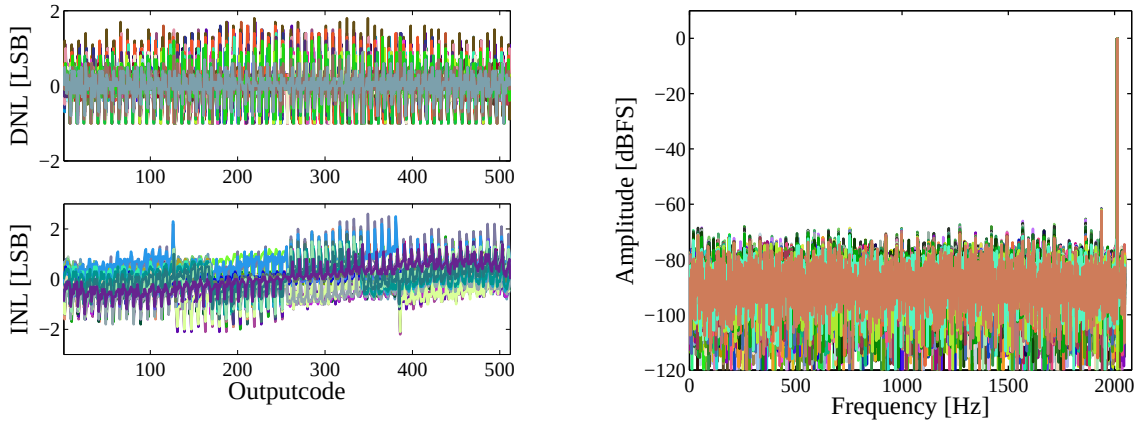



**Figure 3.18:** Statistical distribution of (a) DNL and INL errors (b) FFT spectrum.

extreme codes because of increased impact of voltage dependent parasitics for those. The mean and $3\sigma$ DNL errors are 1.01 LSB and 0.77 LSB respectively. 1.4 LSB and 1.08 LSB respectively are those of INL errors. Similar number of runs are carried out to test dynamic nonlinearity. Figure 3.18b shows the plots of FFT spectrum. The mean and $3\sigma$ SNR are 52.04 dB and 3.63 dB respectively. The deviation from the mean could be attributed to nonidealities originating from process variation. The third harmonic component is distinctly visible in the spectrum, largely due to the signal dependent switch nonidealities.

For the present size of the unit capacitor, the achievable mismatch factor is below 0.1% (An information provided by foundry). The impact of capacitor mismatch on conversion accuracy is verified by simulation of the ADC model. The mean SNR and $3\sigma$ SNR deviations against capacitor mismatch are plotted in Figure 3.19. The plot shows that the proposed ADC architecture is capacitor mismatch tolerant by a large extent.

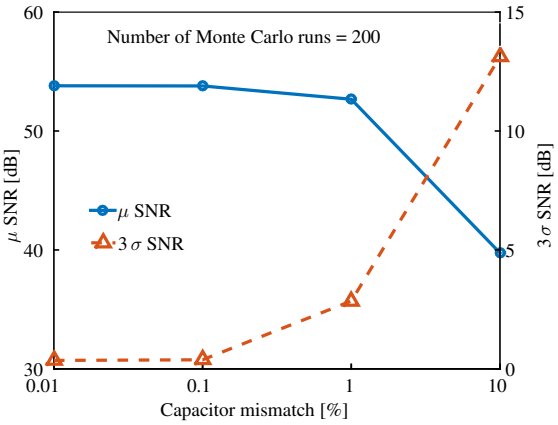



**Figure 3.19:** SNR against capacitor mismatch.

## 3.6 COMPARISON AND DISCUSSION

The ADC is compared with other state-of-art SAR ADC designs in Table 3.4. The proposed ADC has good area performance and at the same time performing considerably well with energy efficiency. Chung et al. (2015) uses capacitor-swapping technique to overcome capacitor mismatch issues. Unit capacitors, forming MSBs, are swapped for consecutive conversion cycles. With this effort, the INL is quenched. Multi-level swapping is needed

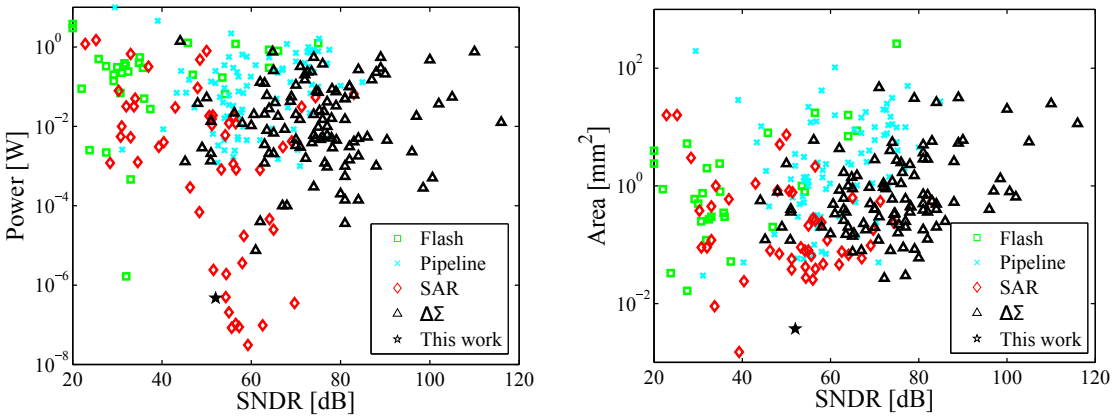
to achieve a low INL error, and hence slight overhead in area and controller complexity. Programmable comparator, along with digital redundancy technique, fetches several MSB bits with small power consumption and remaining LSBs when switched to low noise condition. Tai et al. (2014) implements subranging SAR ADC with energy efficient algorithm at lower technology node. First 5 MSBs are obtained with a coarse ADC using a low power comparator and remainder 5 bits with a fine ADC that uses low noise comparator. The coarse and fine DAC maintain constant common mode voltage at the comparator inputs, which helps in achieving good linearity. A recent work, Harpe et al. (2014) uses dithering of DAC, chopping and data driven noise reduction techniques with oversampling scheme. Custom designed unit capacitors deliver low power consumption in capacitor arrays and dithering overcomes the capacitor mismatch. The offset and even order harmonics are reduced using chopper circuits, while quantization noise is averaged out with the help of data driven noise reduction technique. While this is made possible with the help of oversampling for obtaining high resolution and hence low bandwidth, the same may impose a significant overhead for lower resolutions. Charge injection DAC structure and interrupted settling of voltage at DAC is introduced in Choo et al. (2016) to overcome capacitor and bandwidth limitations to provide high speed ADC with high area efficiency.

In the proposed ADC, nonbinary unit capacitor are used. The capacitor sizes are in a range where matching is easily achieved. Unlike other ADCs, the DAC does not require reference buffers for fast settling of voltages and hence power consumption is low. The proposed architecture trades DAC array power consumption with complexity in controller. This shall be an advantage to have the ADC design to easily co-exist with digital technology process and also one can incorporate low power techniques in digital circuits for reduction of power consumption. Sacrificing comparator bandwidth, pre-amplifier gain is maintained high enough to reduce latch offset and power consumption. Chopper circuit at the input of comparator is avoided to keep the parasitics low. However, efforts are made to achieve good matched layout. The power consumption of the ADC is least dependent on the capacitor array but on complexity of digital controller circuit. Unlike other SAR ADC designs, CAs occupy a smaller portion of the ADC layout (refer Figure 3.16). This indicates that the area of the ADC would only slightly increase if higher resolution is desirable. It is

interesting to note that the designed SAR ADC is quite competent with many other state-of-art designs even though proposed ADC is simple and do not incorporate any linearity improvement techniques that are mentioned in this section. The ADC is compared with the other published ADCs at ISSCC (during 1997-2016) in Figure 3.20.

**Table 3.4:** ADC performance comparison

| | Tai *et al.* (2014) | Chung *et al.* (2015) | Harpe *et al.* (2014) | Choo *et al.* (2016) | This work |
|---|---|---|---|---|---|
| Supply voltage (V) | 0.45 | 0.9 | 0.8 | - | 1 |
| Process (nm) | 40 | 110 | 65 | 40 | 90 |
| Sampling rate (MS/s) | 0.2 | 1.0 | 0.128 | 1K | 0.1 |
| Power (W) | 84n | 16.5$\mu$ | 1.367$\mu$ | 1.26m | 473n |
| ENoB (bit) | 8.95 | 10.92 | 12.35 | 5.46 | 8.35 |
| Core area ($mm^2$) | 0.0065 | 0.092 | 0.18 | 0.00058 | 0.00371 |
| FoM (fJ/c-s) | 0.85 | 8.47 | 8.2 | 28.7 | 14.5 |
| AE ($\mu m^2$/code) | 13.14 | 47.48 | 34.48 | 13.18 | 11.37 |




**(a)** **(b)**

**Figure 3.20:** Performance of the implemented ADC against published ADCs at ISSCC (during 1997-2016).

# Chapter 4

# SWITHED CAPACITOR INTEGRATOR BASED SAR ADC

In this chapter, another novel SAR ADC architecture using nonbinary capacitors is proposed. Charge is passively shared between two unit capacitors to yield binary fractions of full scale charge. The shared charge is then integrated on to an input sample-and-hold capacitor with the help of an SC integrator circuit. The proposed architecture is less parasitic sensitive and has low noise characteristics. A low power subthreshold differential amplifier with high enough gain is designed to minimize total power consumption. The control logic complexity and number of conversion clock cycle requirements are just as that of a traditional SAR ADC. As desired in the previous chapter, low power and area-efficient ADC is the design objective. A 931 nW 8 bit 780 kS/s 0.7 V SAR ADC based on nonbinary weighted dual CA is designed and implemented in a 90 nm CMOS process. The ADC has a small area footprint of 0.00145 $mm^2$. An ENoB of 6.71 and an FoM of 11.39 fJ/c-s is achieved. The performance is verified through simulation.

# 4.1 PROPOSED SAR ADC

## 4.1.1 Concept

Consider two unit capacitors, $C_1$ and $C_2$, of which $C_1$ is initially precharged to full scale reference voltage $V_{ref}$ and $C_2$ discharged to *gnd*. An illustration is shown in Figure 4.1a. The switches are assumed to be closed when clock is high. At the rising edge of $\phi 2$, charge stored in $C_1$ is passively shared with $C_2$. The charge retained in each of these capacitors after sharing is equal to half the initial charge on $C_1$. $C_2$ discharges to *gnd* during phase $\phi 1$. The cycle could be repeated to yield binary fractions of the initial charge. The consecutive voltages across the capacitors during phase $\phi 2$ will be $\frac{V_{ref}}{2}$, $\frac{V_{ref}}{4}$, $\frac{V_{ref}}{8}$ and so on. As an equivalent we could also discharge $C_2$ to *gnd* by using switched capacitor technique, illustrated in Figure 4.1b. During phase $\phi 1$ charge in $C_2$ is transferred to an integrator

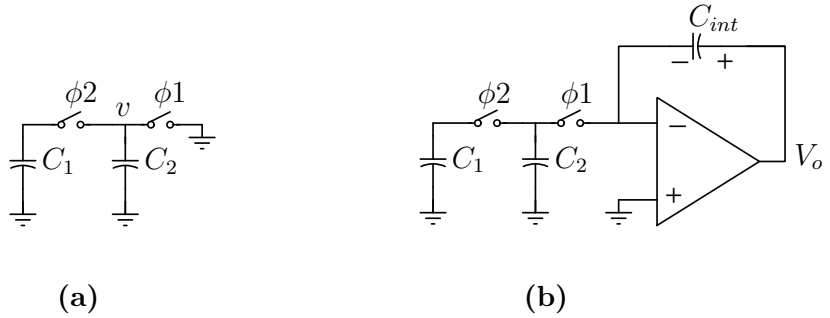



**Figure 4.1:** Illustration of (a) passive charge sharing between unit capacitors and (b) SC integration.

capacitor $C_{int}$. Assuming $C_{int}$ is also an unit sized capacitor and is initially precharged to input voltage $V_{in}$, the output voltage $V_o$ of integrator after N clock cycles is given by

$$V_o = V_{in} - \sum_{i=2}^{N} D_i \frac{V_{ref}}{i}$$

where $D_i$ is a binary decision used in the integration process to discharge $C_2$ at $i^{th}$ clock cycle.

The above method realizes an ADC using switched capacitor integration technique. However in a realistic circuit, we see few serious issues concerning the conversion accuracy.

Firstly, switch parasitics and their variation with respect to voltage introduces error voltage during sharing of charge. Secondly, thermal noise at the integrator output due to the switch and the amplifier increases linearly with clock cycle. The sharing of charge between two unit sized capacitors is made parasitic insensitive by allowing equal amount of parasitics on both. However, voltage dependent junction parasitics at the charge sharing nodes can still be present. The resultant voltage, say $v$, due to sharing of charge between two unit capacitors, $C_1$ and $C_2$, is represented by (4.1).

$$v = \frac{Q_1 + Q_2 + q_{p1} + q_{p2}}{C_1 + C_2 + c_{p1}(v) + c_{p2}(v)} \tag{4.1}$$

where $Q_1$, $q_{p1}$ and $c_{p1}(v)$ are respectively charge, parasitic charge and parasitic capacitance associated with capacitor $C_1$. Similarly $Q_2$, $q_{p2}$ and $c_{p2}(v)$ are associated with capacitor $C_2$. Capacitors $c_{p1}(v)$ and $c_{p2}(v)$ are voltage dependent parasitics, contributing to the error in sharing of charge. The swing in voltage $v$ and switch implementation are two critical factors influencing this error. With $C_1$ being initially charged to $V_{ref}$ and $C_2$ discharged to $gnd$, the maximum value of $v$ will be equal to $V_{ref}/2$.

To mitigate the error in charge sharing, first, we suggest to make use of two separate passive charge sharing circuits. One such circuit operates with positive rail supply voltage $V_{DD}$ and the other with negative rail supply voltage $V_{SS}$. Supply voltages shall be $V_{DD} = -V_{SS} = V_{ref}/2$. The charge aquired by unit capacitors of both charge sharing circuits, during phase $\phi 2$, will be the same, but opposite in polarity. In a given clock cycle, charge from a unit capacitor of either of the two charge sharing circuits will be allowed to integrate on to $C_{int}$. The choice is based on previous comparison result of the integrator output voltage against common mode voltage $gnd$. Second, we double the size of the integration capacitor $C_{int}$, due to which the thermal noise power at the output of the integrator is reduced by a factor of 4 (discussed in subsection 4.2.1). This gain reduction of the integrator halves the intended DAC equivalent voltage. To compensate this voltage attenuation by the integrator, double the charge needs to be transferred. In support of this, all unit capacitors in both charge sharing circuits sample their respective supply voltage during initialization.

By having two separate passive charge sharing circuits, the worst case voltage swing is limited to $V_{ref}/4$ instead of $V_{ref}/2$. This would enhance the charge sharing accuracy by twofold (assuming rate of change in voltage dependent parasitic with respect to node voltage is a constant).

The polarity of charge to integrate with $C_{int}$ is decided based on previous comparison result. Thus the integration phase operates conditionally. But the charge sharing phase does not. The sharing of charge between capacitors and comparison of the integrator output is performed simultaneously. The width of charge sharing phase is large enough to relax performance requirements of the comparator. The number of phases per clock remains at two.

### 4.1.2 Circuit Description

Figure 4.2 shows the proposed switched capacitor integrator based SAR ADC. Unit capacitors $C_1$ and $C_2$ form a passive charge sharing capacitor pair, meant for obtaining charge equivalent to positive binary fractions of reference voltage. Unit sized capacitors $C_3$ and $C_4$ form the other passive charge sharing capacitor pair. The purpose of them is to acquire equal amount of charge as that of capacitor combination $C_1$ and $C_2$, but opposite in polarity. Capacitor $C_{int}$ is both serving as sample-and-hold and integrator capacitor. The bottom plates of all the charge sharing capacitors, noninverting terminal of operational transconductance amplifier (OTA) and inverting terminal of comparator are all connected to common mode potential *gnd*. The comparator output $B_i$ is the ADC output at successive clocks. $B_i$ is fed to control logic circuit, which executes successive approximation algorithm by operating switches in reference to the clock signal. A dual power supply voltage source is used, with common terminal voltage at *gnd*. It may happen that the voltage magnitudes of $V_{DD}$ and $V_{SS}$ differ. Under such circumstances, changes could be brought into the architecture, wherein capacitors $C_3$ and $C_4$ sample voltage $V_{DD}$ at their bottom plates,

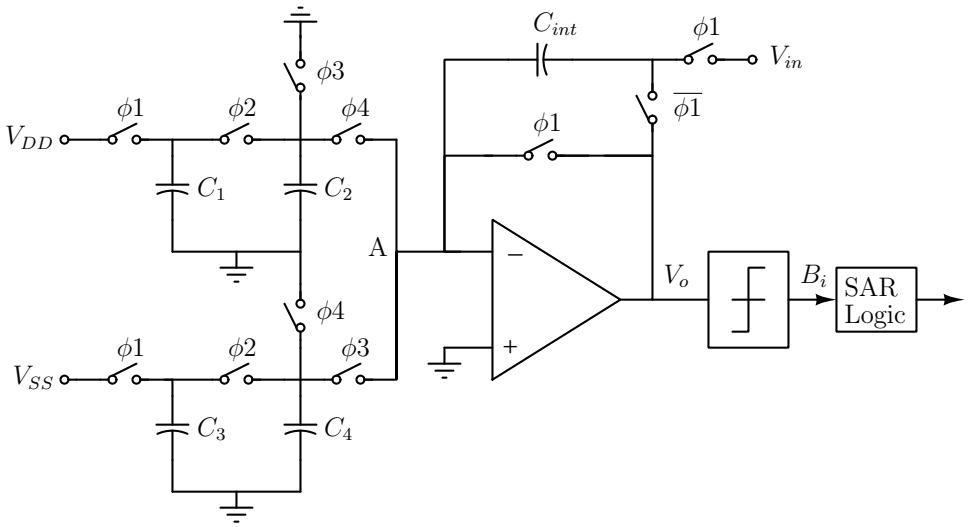



**Figure 4.2:** Proposed SAR ADC.

### 4.1.3 Operation

For an N bit ADC, the conversion happens in N clock cycles. The clock phases are nonoverlapping. Each clock cycle constitutes a charge sharing and a charge integration phase. Nominally, capacitors $C_1 = C_2 = C_3 = C_4 = C$ and $C_{int} = 2C$. Supply voltage $V_{DD} = -V_{SS} = V_{ref}/2$. Terminal $A$ in Figure 4.2 corresponds to virtual ground. Following describes the the different stages of operation. Step 1 is performed once at the beginning of every conversion cycle, while steps 2 and 3 are executed N times for an N bit conversion.

1. *Sampling:* Phases $\phi1$ and $\phi2$ raise, so as to sample the analog input voltage $V_{in}$ on to $C_{int}$, and charge capacitors $C_1$ and $C_2$ to voltage $V_{DD}$, and capacitors $C_3$ and $C_4$ to voltage $V_{SS}$ (refer Figure 4.3a). The integrator output voltage $V_o = V_{in}$.

2. *Passive charge sharing and comparison:* With $\phi2$ remaining high, capacitors $C_1$ and $C_2$ share charge, so do $C_3$ and $C_4$ (refer Figure 4.3b). Integrator output voltage $V_o$ is compared against common mode voltage *gnd* to decide upon the MSB.

3. *Charge integration:* Based on the comparison output, either $\phi3$ or $\phi4$ will raise, leading to transfer of charge from either capacitor $C_2$ or $C_4$ to capacitor $C_{int}$ (refer Figure 4.3(c-d)). Capacitor not involved in charge transfer will discharge to *gnd*. If the MSB was logic low,

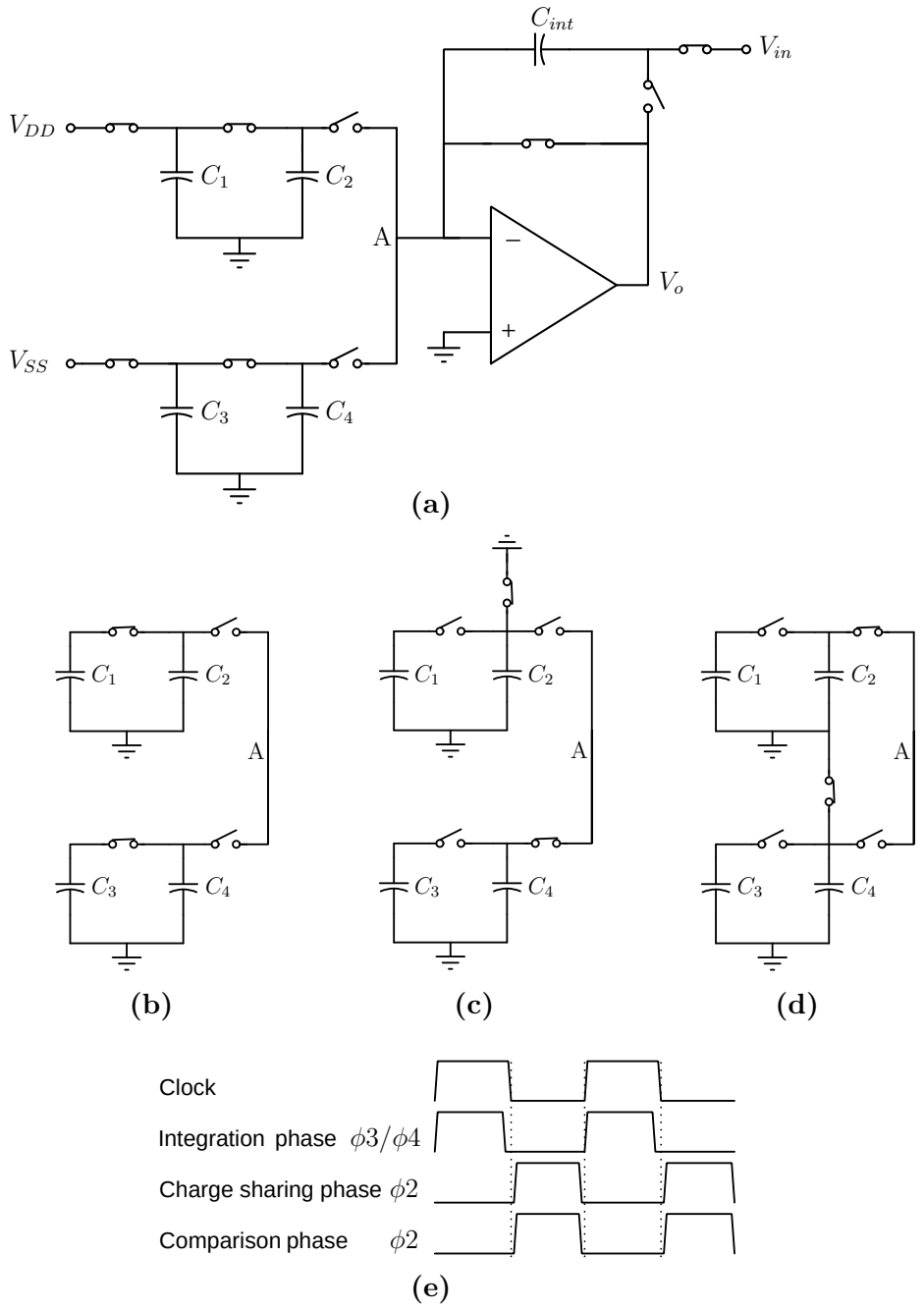



**Figure 4.3:** Illustration of the proposed architecture. Circuit configuration during (a) initialization / sampling phase (b) passive charge sharing and comparison phase (c) charge integration phase, say, for MSB result of '0' and (d) charge integration phase otherwise. (e) Desired clock phases for conversion during steps $2-3$.

phase $\phi 3$ raises. Else, phase $\phi 4$ will raise. Capacitors $C_1$ and $C_3$ hold on to their charge. The new output voltage will be

$$V_o = V_{in} + (-1)^{MSB} V_{ref}/4$$

4. The remaining bits are similarly determined by following steps $2-3$. Desired clock phases for conversion, during steps $2-3$, are shown in Figure 4.3e.

# 4.2 ARCHITECTURE ANALYSIS

## 4.2.1 Noise estimation

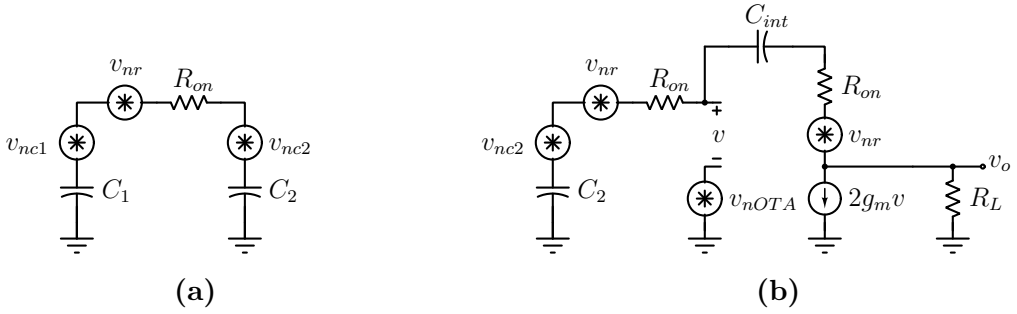



**Figure 4.4:** Noise analysis model of the ADC during (a) charge sharing and (b) charge integration.

For simplicity, a portion of network (in Figure 4.2) having $C_1$, $C_2$ and $C_{int}$ is considered. The switches are the source of thermal noise due to finite $ON$ state resistance. The switch is modelled as a resistor $R_{on}$ in series with a noise source $v_{nr}$. Noise model during charge sharing process is shown in Figure 4.4a. Sharing of charge adds thermal noise onto the capacitors. $v_{nc1}$ and $v_{nc2}$ respectively represent such noise with $C_1$ and $C_2$. The mean square (MS) noise voltage across all the capacitors initially is equal to $kT/C$, suggesting $\overline{v^2}_{nc1}[1] = kT/C$. Since $C_2$ always discharges to either $gnd$ or virtual ground before commencement of charge sharing, $v_{nc2}$ for any clock cycle will be $kT/C$. The noise acquired after sharing

during $n^{th}$ cycle is given by

$$\overline{v^2}_{nc1}[n+1] = \overline{v^2}_{nc2}[n+1] = \frac{1}{2}\left(\overline{v^2}_{nc1}[n] + \frac{2kT}{C}\right) \tag{4.2}$$

The noise acquired by $C_2$ towards the end of charge sharing phase is introduced in integration phase and vice versa. Noise model during integration phase is shown in Figure 4.4b. The acquired noise by $C_2$, along with integrating switch noise and transconductance amplifier (OTA) noise, is added onto $C_{int}$. Input referred thermal noise of the OTA is represented by source $v_{nOTA}$. Output resistance $R_L$ of the OTA is assumed to be infinite. The noise source $v_{nr}$, placed at integrator output node, is due to switching during input sample-and-hold process. The integrating switch noise and OTA noise are given by (4.3) and (4.4) Schreier et al. (2005)

$$\overline{v^2}_{nSW} = \frac{kT/C}{1+1/x} \tag{4.3}$$

$$\overline{v^2}_{nOTA} = \frac{kT\Gamma/C}{1+x} \tag{4.4}$$

The parameter $x = 2g_mR_{on}$. $\Gamma$ is commonly known as Ogawa's / excess noise factor (device noise alone). $g_m$ represents the OTA transconductance. Since integrator gain is halved, the noise added at integrator output during every cycle is

$$\overline{v^2}_{n,o}[n] = \frac{1}{4}\left(\overline{v^2}_{nc2}[n] + \overline{v^2}_{nSW} + \overline{v^2}_{nOTA}\right) \tag{4.5}$$

The total MS noise at output, including input sampling noise, towards the end of $N^{th}$ clock cycle is

$$\overline{v^2}_{n} = \sum_{n=2}^{N} \overline{v^2}_{n,o}[n] + \frac{kT}{C} \tag{4.6}$$

With $x \gg 1$, the OTA noise could be neglected and Table 4.1 shows computed MS noise values. Equating obtained thermal noise to quantization noise, the minimum size of total capacitance required for different ADC resolutions is plotted in Figure 4.5. Plot is shown, wherein the BWCA based SAR ADC is limited by mismatch. (4.7) from Zhang et al. (2012) estimates the total capacitance requirement.

**Table 4.1:** Noise computation for the proposed ADC

| Clock | $\overline{v^2}_{nc2}$ (kT/C) | $\overline{v^2}_{n}$ (kT/C) |
|---|---|---|
| 1 | 1 | 1 |
| 2 | 1.5 | 1.625 |
| 3 | 1.75 | 2.3125 |
| 4 | 1.875 | 3.03125 |
| 5 | 1.9375 | 3.765625 |
| 6 | 1.96875 | 4.5078125 |
| 7 | 1.984375 | 5.25390625 |
| 8 | 1.9921875 | 6.001953125 |

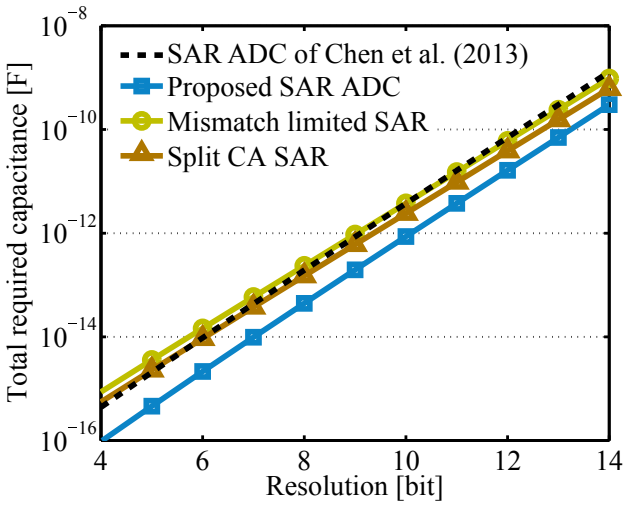



**Figure 4.5:** Total capacitance requirement in various SAR ADC architectures.

$$C_{BWCA} = 2^N 18(2^N - 1)K_\sigma^2 K_C \tag{4.7}$$

where $K_\sigma$ is the mismatch coefficient and $K_C$ is the capacitor density, whose respective values considered are 1% $\mu$m and 2 fF/$\mu m^2$. Plot also shows total capacitance estimate for a split BWCA with two identical arrays. (4.7) is modified and presented in (4.8). The estimate shows slight reduction in total capacitance as $K_\sigma$ reduces with large size capacitors. $K_\sigma$ taken as 0.8% $\mu$m.

$$C_{splitBWCA} = 2^{(\frac{N}{2}+1)} 18(2^{(\frac{N}{2}-1)})2^N K_\sigma^2 K_C \tag{4.8}$$

A similar noise estimation is done for proposed architecture in Chen et al. (2013) and its plot of total capacitance requirement is also shown in the figure. Since integrator gain is unity and possibly two integrations per bit, the accumulated thermal noise is large in their case and in worst case is given as

$$\overline{v^2}_n \approx 4\sum_{n=2}^{N} \overline{v^2}_{n,o}[2n] + \frac{kT}{C} \tag{4.9}$$

All the plots are normalized to voltage range of 1 V. It is evident that the proposed architecture of SAR ADC has least total capacitance requirement. As a comparison, for resolution of 10 bits, the total capacitance value of proposed ADC is 0.785 pF against 2.4 pF of split BWCA SAR and 3.7 pF of the rest.

### 4.2.2 Capacitor mismatch

For mismatch analysis, assume capacitors $C_2$ and $C_4$ are larger than capacitors $C_1$ and $C_3$, their normalized capacitance value being $1+\alpha$ and $1-\alpha$ respectively with $\alpha \ll 1$. The normalized capacitance value of capacitor $C_{int}$ shall be $2(1 \pm \frac{\alpha}{\sqrt{2}})$ and we shall pick the smaller term (negative symbol) in this analysis. These assumptions will lead to explore the worst possible error due to unit capacitor mismatch. Let $q$ be the desired initial charge in the unit capacitors. Table 4.2 shows the charge held by unit capacitors of charge sharing circuits at different clock cycles during analog to digital conversion. The higher order terms of $\alpha$ are ignored.

For an N-bit ADC, the sequence of stored charge in capacitors $C_2$ and $C_4$ will be $q(1+\alpha)$, $\frac{q}{2}$, $\frac{q}{4}(1-\alpha)$, $\frac{q}{8}(1-2\alpha)$ and so on till $\frac{q}{2^{N-1}}(1-(N-2)\alpha)$.

The integrator output voltage is dependent on output bits and can be written as,

$$V_o = V_{in} - q\Bigg[\Big(B_{N-1}(1+\alpha) + \frac{B_{N-2}}{2} + \frac{B_{N-3}}{4}(1-\alpha) + ... + \frac{B_1}{2^{N-2}}(1-(N-3)\alpha)\Big) - \Big(\overline{B}_{N-1}(1+\alpha) + \frac{\overline{B}_{N-2}}{2} + \frac{\overline{B}_{N-3}}{4}(1-\alpha) + ... + \frac{\overline{B}_1}{2^{N-2}}(1-(N-3)\alpha)\Big)\Bigg]\frac{1}{2(1-\frac{\alpha}{\sqrt{2}})}$$

**Table 4.2:** Charge held by unit capacitors during charge sharing phase

| Clock | Charge held by | |
|---|---|---|
| | $C_1$ ($C_3$) | $C_2$ ($C_4$) |
| 1 | $q(1-\alpha)$ | $q(1+\alpha)$ |
| 2 | $q(\frac{1-2\alpha}{2})$ | $q(\frac{1}{2})$ |
| 3 | $q(\frac{1-3\alpha}{4})$ | $q(\frac{1-\alpha}{4})$ |
| 4 | $q(\frac{1-4\alpha}{8})$ | $q(\frac{1-2\alpha}{8})$ |
| . | . | . |
| . | . | . |
| N | $q(\frac{1-N\alpha}{2^{N-1}})$ | $q(\frac{1-(N-2)\alpha}{2^{N-1}})$ |

The above equation could be rewritten as

$$V_o \approx V_{in} - q\sum_{k=1}^{N-1}\frac{1}{2^k}\Big(B_{N-k}\big(1-(k-2)\alpha\big) - \overline{B}_{N-k}\big(1-(k-2)\alpha\big)\Big)\Big(1+\frac{\alpha}{\sqrt{2}}\Big) \tag{4.10}$$

Note that, towards the end of conversion, the integrator output voltage should ideally converge to zero. However, the nonzero value arises due to the capacitor mismatch. Denoting the error as $\varepsilon$, we get,

$$\varepsilon \approx V_{in} - q\sum_{k=1}^{N-1}\frac{1}{2^k}\Big(B_{N-k}-\overline{B}_{N-k}\Big) + q\alpha\sum_{k=1}^{N-1}\frac{1}{2^k}\left[\Big(B_{N-k}-\overline{B}_{N-k}\Big)(k-2) - \Big(\frac{B_{N-k}-\overline{B}_{N-k}}{\sqrt{2}}\Big)\right]$$

The magnitude of the output error voltage is then

$$|\varepsilon| \approx q\alpha\sum_{k=1}^{N-1}\frac{1}{2^k}\left[\Big(B_{N-k}-\overline{B}_{N-k}\Big)(k-2) - \Big(\frac{B_{N-k}-\overline{B}_{N-k}}{\sqrt{2}}\Big)\right] \tag{4.11}$$

In (4.11), the term $(B_{N-k}-\overline{B}_{N-k})$ bear difference in sign for $k \geq 2$. Thus the voltage $\varepsilon$ is maximum at places of one and three quarters of output codes. Let us choose the code to be 0011..1. Note, this selection of code is conditionally true and depends on the assumption of capacitor sizes made earlier in this analysis. The expression of $\varepsilon$ for the preferred output

code is

$$|\varepsilon_{max}| \approx q\alpha\left[\frac{\left(1+\frac{1}{\sqrt{2}}\right)}{2^1}+\frac{\left(0+\frac{1}{\sqrt{2}}\right)}{2^2}+\frac{\left(1-\frac{1}{\sqrt{2}}\right)}{2^3}+...+\frac{\left(N-3-\frac{1}{\sqrt{2}}\right)}{2^{N-2}}\right]$$

Summing the arithmetico-geometric series within,

$$|\varepsilon_{max}| \approx q\alpha\left[1+\frac{1}{2\sqrt{2}}-\left(\frac{1}{2}\right)^{N-1}\left(N-1-\frac{1}{\sqrt{2}}\right)\right] \tag{4.12}$$

For larger values of N, the term $\left(\frac{1}{2}\right)^{N-1}\left(N-1-\frac{1}{\sqrt{2}}\right)$ converges to zero. On substitution of normalized charge $q$ as $\frac{V_{ref}}{2}$ and $\alpha$ as $\frac{\sigma_u}{C_u}$, (4.12) could be reduced to,

$$\frac{|\varepsilon_{max}|}{V_{ref}} \approx 0.676\frac{\sigma_u}{C_u} \tag{4.13}$$

Above equation represents the relation between the conversion accuracy and the capacitance mismatch. This mismatch result is similar to the one obtained in Suarez et al. (1975). With modern chip fabrication technologies being able to provide well matched capacitors, the obtained result assures good conversion accuracy. For an obtained unit capacitor size (30 fF) in the design, the standard deviation of unit capacitance is around 0.1%. Considering that the ADC delivers 8 bit accuracy, the conversion error introduced due to worst capacitor matching is within the range of 0.2 LSB.

## 4.3 IMPLEMENTATION

### 4.3.1 Amplifier

The amplifier circuit is the vital component, influencing the power and speed performance of the ADC. An OTA is designed in subthreshold region to reduce power consumption. A dual supply voltage source with common terminal voltage at *gnd* energizes the OTA. The circuit diagram is illustrated in Figure 4.6. The OTA offers required DC gain and bandwidth at low voltage and consumes less power and surface area. The body of all the transistors (both NMOS and PMOS) in the circuit is tied to *gnd* in order to reduce their threshold voltage.

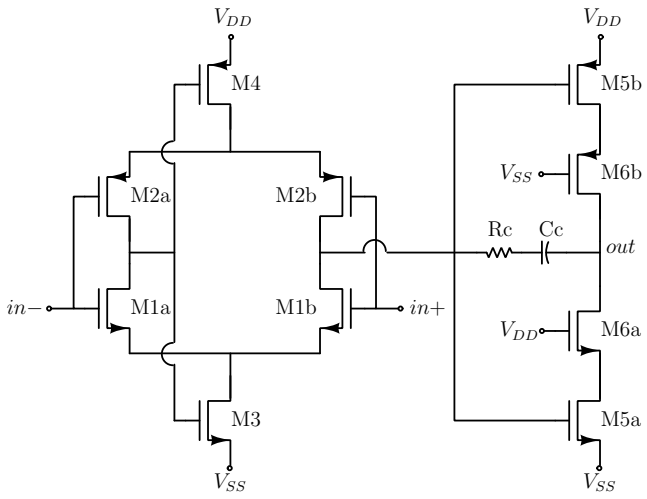



**Figure 4.6:** Amplifier circuit diagram.

The transistors' bulk-to-source junctions are hence slightly forward biased, but since the forward bias voltage is around 350 mV the bulk-to-source junctions are well below danger zone of conduction. The differential input inverter based amplifier (Bazes, 1991) is used as the first stage of the amplifier followed by the class C inverter. In the first stage, transistors $M1_a$ and $M1_b$ form the NMOS differential pair, while transistors $M2_a$ and $M2_b$ are the PMOS differential pair. The current sources formed by $M3$ and $M4$ are self biased by the output of $M1_a$ and $M2_a$ inverter pair. The source terminal of transistors $M1_a$ and $M2_a$ are degenerated by negative feedback. This ensures proper biasing of the input differential pair against all variations in the PVT. The transconductance pairs $M1_{a,b}$ and $M2_{a,b}$ have input common mode at *gnd*, thus avoiding gate bias circuit that usually draw considerable amount of power. Output stage ($M5_{a,b}$ and $M6_{a,b}$) is in cascode configuration to boost the gain and provide necessary slew rate performance. Simple Miller RC compensation is used to stabilize the circuit.

#### 4.3.1.1 Small signal analysis

A simplified small signal model of the OTA is shown in Figure 4.7. The gain of the first stage is given by

$$A_1 = (g_{m1} + g_{m2})r_{d1-2} \tag{4.14}$$

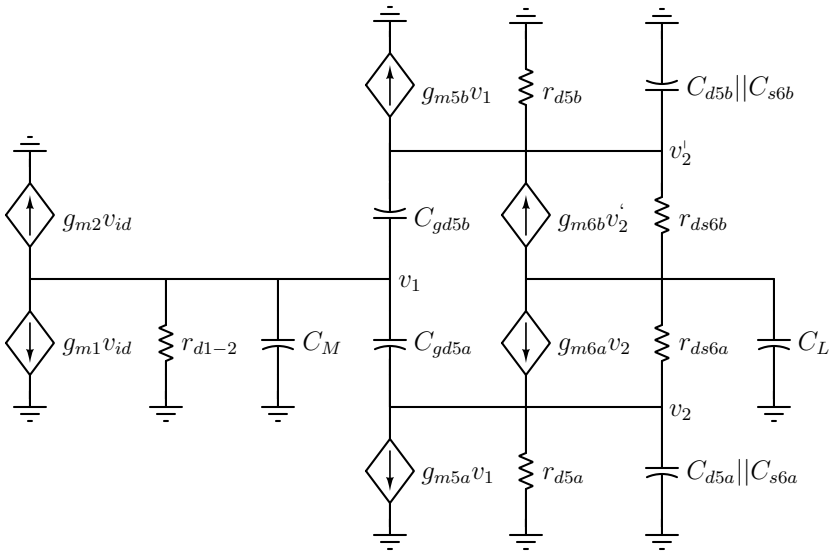



**Figure 4.7:** OTA small signal model.

where $g_{m1}$ and $g_{m2}$ are the transconductances of transistors $M1_{a-b}$ and $M2_{a-b}$ respectively and $r_{d1-2}$ is the equivalent output resistance at the first stage.

The output of the first stage is fed to the class C inverter constituting $M5_{a-b}$ and $M6_{a-b}$ in complementary cascode structures. The gain of the second stage could be written as

$$A_2 \approx g_{m5}g_{m6}r_{d5}r_{ds6} \tag{4.15}$$

where $g_{m5}$ and $g_{m6}$ are the transconductances of transistors $M5_{a-b}$ and $M6_{a-b}$ respectively. $r_{ds5}$ and $r_{ds6}$ are their respective output resistances. The total DC gain is given by

$$A_V = A_1A_2 \tag{4.16}$$

The second stage offers a high voltage gain as evident from (4.15). Owing to this large gain, a small compensation capacitance $C_c$ is sufficient to provide stability to the amplifier. This capacitor, along with resistor $R_c$ in series, is connected across the second stage.

$v_1$, $v_2$ and $v_2'$ are the intermediary node voltages in the amplifier (along the pole locations). $C_M$ is the capacitor equivalent to the sum of drain capacitances at node having voltage $v_1$ and the Miller capacitance $(1+A_2C_c)$. Due to the Miller effect, a dominant pole

**Table 4.3:** Design values of OTA components

| Component | Type | Length ($n$m) | Width ($n$m) |
|---|---|---|---|
| $M1_a$, $M1_b$ | N_12_LL | 1000 | 120 |
| $M2_a$, $M2_b$ | P_12_LL | 200 | 120 |
| $M3$, $M5_a$ | N_12_LL | 280 | 120 |
| $M4$, $M5_b$ | P_12_LL | 120 | 560 |
| $M6_a$ | N_12_LL | 90 | 120 |
| $M6_b$ | P_12_LL | 90 | 200 |
| $R_c$ | resistor 140 K$\Omega$ | 5 x 12000 | 440 |
| $C_c$ | capacitor 30 $fF$ | 7000 | 3300 |

$f_{p1}$ exist close to the origin and other poles are pushed to high frequency region, providing good phase margin and thus enabling good stability.

$$f_{p1} = \frac{1}{2\pi r_{d1-2} C_M} \tag{4.17}$$

The component sizes of the designed OTA are mentioned in Table 4.3. The presented differential amplifier is used in realization of the SC integrator. The gain error of the integrator could be expressed as

$$|gain\ error| \approx \frac{(C_{in}/2C_{int} + 1)}{A_V} \tag{4.18}$$

where $C_{in}$ is a intended capacitance between virtual node and $gnd$.

The limited sizes of the transistors show considerable mismatch leading to offset voltage. This offset voltage will severely degrade the accuracy requirements of both the charge sharing and charge integration process of the ADC. An autozeroing technique (Enz and Temes, 1996), illustrated in Figure 4.8, is efficient in removing the input referred offset voltage and $1/f$ noise of the amplifier. Auto-zeroing technique essentially stores offset voltage to a capacitor during sampling phase and feeding back the stored offset so as to cancel the offset voltage from the signal path. This is equivalent to shifting the virtual ground point of the differential amplifier to the junction node of capacitors $C_{int}$ and $C_{off}$. The switches

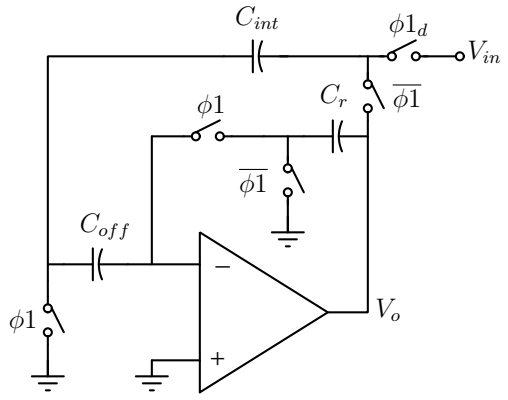



**Figure 4.8:** Input referred offset cancellation of the amplifier (Enz and Temes, 1996).

are operated in phases $\phi_1$ and $\phi_2$. To assist autozeoring, Capacitor $C_r$, nearly charged to 0.5 LSB equivalent voltage during previous analog to digital conversion, shorts the integrator output. By doing so large variation in phase margin is avoided, which otherwise would have resulted due to variation in feedback factor. The feedback factor remain unchanged if capacitor $C_r$ is equal to the size of the unit capacitor. To satisfy accuracy requirement in the stored offset voltage, capacitance of $C_{off}$ is chosen to be equal to unit capacitance.

#### 4.3.1.2 Power analysis

As discussed in earlier sections, the proposed ADC architecture is robust against parasitics and offer low noise at the integrator output. This results in reduced load capacitance at the amplifier output. For a required bandwidth, the transconductance $g_m$ is as given by (4.19). The resulting low $g_m$ allows to trade noise for power consumption.

$$g_m = C_{L,eff} UGB \tag{4.19}$$

The power consumption of the OTA, under the present data conversion environment, is expressed as (4.20). Detailed derivation is presented in Peluso et al. (2013).

$$P = 4N_N N_C kTV_{ov} ln\left(\frac{2}{3}DR^2\right)\frac{DR^2}{V_{ref}} f_{clk} \tag{4.20}$$

where $V_{ov}$ is the transistor gate overdrive voltage, $N_N$ and $N_C$ respectively are excess noise factor (takes into account other noise sources, such as the noise related to switches of charge sharing capacitors and the OTA) and excess capacitance factor at the integrator output. In this architecture $N_N$ is expressed as Peluso et al. (2013)

$$N_N = \left(\frac{\overline{v^2}_q}{\frac{kT}{C_{int}}}\right)\left(\frac{2g_mR_{on}+\Gamma}{1+2g_mR_{on}}\right) \tag{4.21}$$

wherein $\overline{v^2}_q$ is the quantization noise power. $\Gamma$ is a product of channel noise factor $\gamma$ and ratio of drain-source conductance to transconductance at zero drain-source voltage $g_{d0}/g_m$.

In the present work, the total thermal noise power at the integrator output, as in (4.6), is equated to half of the quantization noise power (dynamic range of 48.16 dB). This requires the integrating capacitor to be 60 $f$F for an 8 bit conversion. Assuming $2g_mR_{on} \gg 1$, (4.21) results is $N_N = 9$. The excess capacitance factor $N_C$ is chosen to be 2, since $C_{L,eff}$ is twice the integrating capacitor. For $V_{ref}$ of 0.7 V, $V_{ov}$ of 0.1 V and clock frequency of 6.24 MHz, the OTA estimated power consumption is 186.7 nW. This estimated power consumption is less than the actual value (369 nW) for the OTA. The reasons being (1) the OTA is assumed to be single stage (2) the nonlinear slewing of the OTA is unaccounted and (3) the product $2g_mR_{on}$ could be comparable to unity, leading to increased OTA noise (by factor $\Gamma$) at the integrator output. Typical value of $\gamma$ is in the range 2/3 to 3. For short channel transistors, $\gamma$ increases and $g_m$ reduces in comparison to $g_{d0}$ (Sackinger, 2011). $\Gamma$ and hence the input referred noise of the OTA increases. With the product $2g_mR_{on}$ being lower than unity in the designed ADC, $N_N$ is increased roughly by a factor of four compared to earlier assumption (due to $\Gamma$ nearing 4). This results in total noise power to be twice the quantization noise power, degrading the dynamic range by another 3 dB. Recomputing (4.20), the power consumption of the OTA is now twice the former value and agrees with the values obtained from simulation.

#### 4.3.1.3 Performance

The DC gain and the phase margin of the OTA are 82.12 dB and $70.61^o$ respectively at typical PVT. The simulated Bode plot is shown in Figure 4.9. The unity gain bandwidth

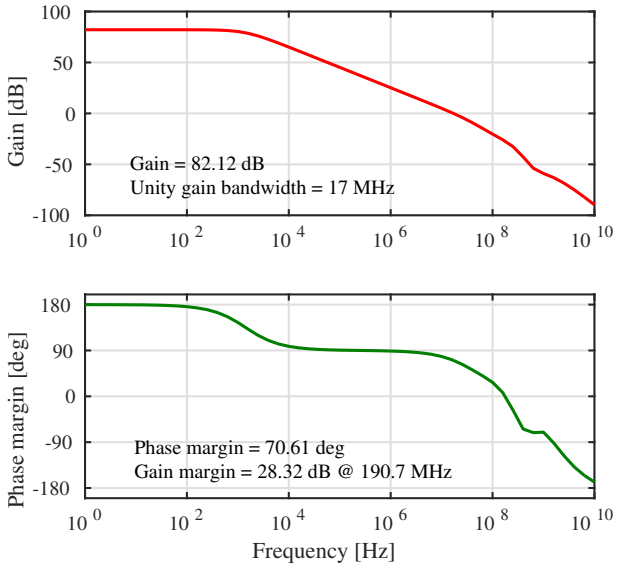



**Figure 4.9:** Bode plot of the OTA.

is close to 17 MHz. Similarly the OTA's common mode rejection ratio (CMRR) and power supply rejection ratio are also simulated. The plots are shown in Figure 4.10. Since the OTA is differential in operation, the CMRR value is close to the OTA DC gain at low frequencies and drops at higher frequencies as the OTA gain reduces. Likewise, the PSRR is also considerably high and mainly attributed due to the performance at first stage of the OTA.

It is essential that the OTA performs satisfactorily at all PVT variations. To ascertain

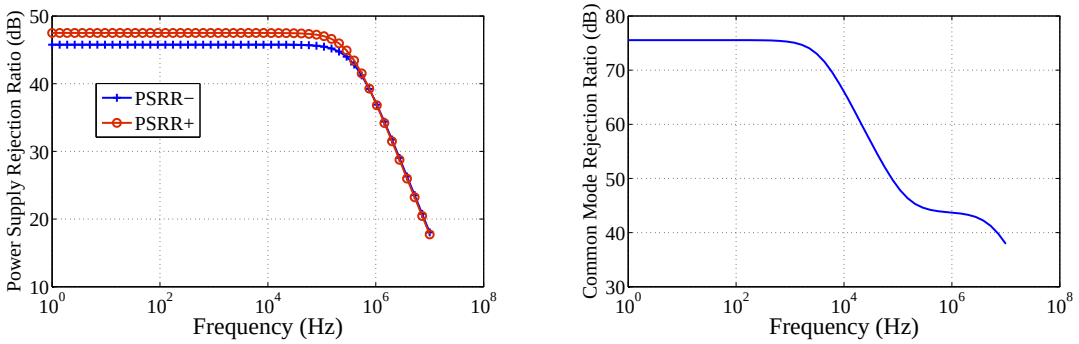
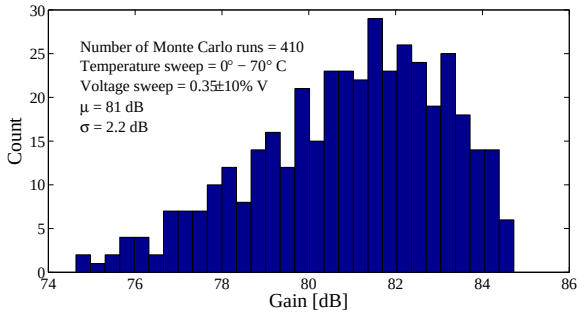
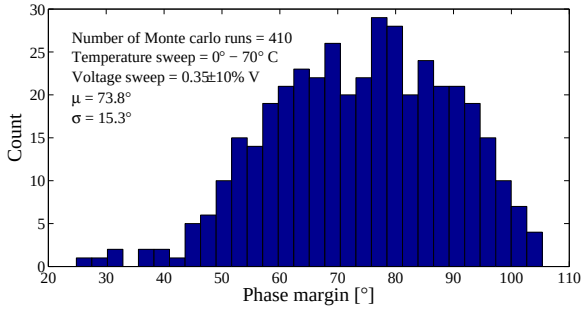



**Figure 4.10:** (a) PSRR and (b) CMRR performance of the OTA.

this, simulations are performed for a range of PVT variations. The gain and phase margin of the OTA are plotted against PVT variations in Figure 4.11. For 410 Monte Carlo runs, the DC gain has a mean value of 81 dB and $\sigma$ of 2.2 dB, and the mean and $\sigma$ of phase margin are $73.8^o$ and $15.3^o$ respectively. The results obtained are indicative of conversion assurance of the ADC for all PVT variations. Owing to the higher gain offered by the class C inverter, the power supply rejection ratio achieved at lower frequencies are close to 47 dB and 45 dB, respectively, for VDD and VSS supply sources. The true differential nature of operation of the amplifier supports a good common mode rejection ratio. The tail current sources in the first stage of OTA are self-biased and hence able to deliver good CMRR despite mismatch. Figure 4.12 shows distribution of PSRR and CMRR against mismatch for 200 Monte carlo runs. The mean PSRR is 46.7 dB and its standard deviation $\sigma$ is 8.37 dB. Similarly, the mean CMRR is 65.6 dB and its $\sigma$ is 6.25 dB.




**(a)**




**(b)**

**Figure 4.11:** Distributions of (a) DC gain and (b) phase margin of the OTA against PVT variations.

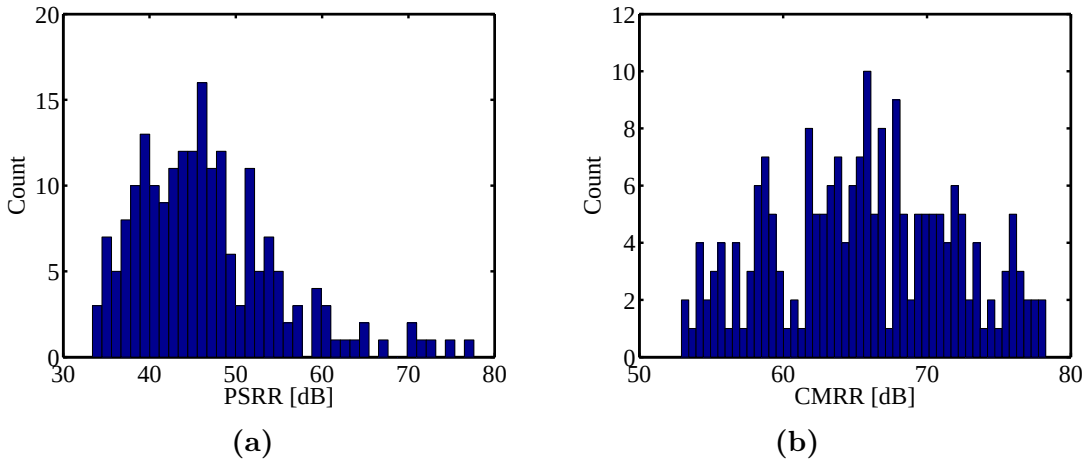



**Figure 4.12:** Distribution of (a) PSRR and (b) CMRR performance of the OTA.

### 4.3.2 Switches and capacitors

Owing to bottom plate sampling technique, the integrator capacitor $C_{int}$ does not acquire signal dependent charge error during input voltage sampling. The charge sharing switch experiences varied amount of channel charge in every clock cycle due, but conversion accuracy is unaffected if the charge is equally split. Impedance seen at either end of the charge sharing switch is same. The circumstances governing the splitting of the channel charge is described in subsection 2.2.1. In the case of charge integration switch, the impedances are different, but remain constant throughout the operation of the ADC. This allows the complementary transistors of the switch to be sized accordingly to minimize error due to channel charge injection for a given temperature and process corner. In addition, complementary transistors lower the variation of voltage dependent parasitic capacitances at charge sharing nodes. This is an added benefit, as it reduces the error due to passive charge sharing between capacitors. Compensating charge injection using PMOS and NMOS together is not always effective because they spread independently and more process dependent. A more accurate charge injection error cancellation is possible by using differential form of the proposed architecture. It takes just an additional integrator capacitor to realize the same.

Switches with small geometry (size) are preferred in order to keep switch parasitics to a minimum. Dummy transistors are placed, wherever necessary, to have equal amount

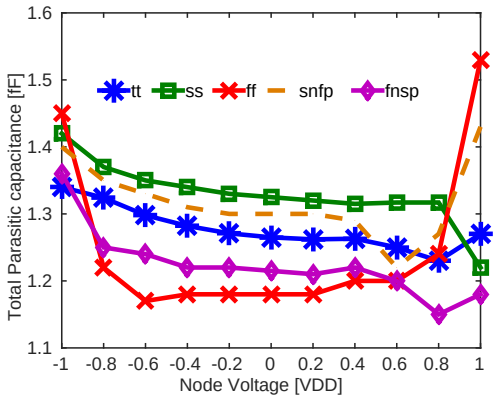



**Figure 4.13:** Node parasitic capacitance at various corners.

of parasitic at all the charge sharing nodes in the architecture. The voltage dependent parasitic at charge sharing node for typical as well as for all process corners is plotted in Figure 4.13. The change in doping concentration of transistor's diffusion regions at various process corners cause parasitic capacitance to vary. This variation is more for a low threshold voltage transistors. The data obtained are used to model parameter variation in statistical simulation of the ADC. In the given technology, MOM capacitors offer mismatch characteristics similar to metal-insulator-metal capacitors. MOM capacitors show better capacitance density and need no extra masks for fabrication. Hence MOM capacitors are chosen in the design, that largely meets the $KT/C$ noise requirement of the ADC for the given resolution.

### 4.3.3 Comparator

The comparator specifications are relaxed due to charge sharing process being independent of the comparison result. A double-tail dynamic latched comparator (van Elzakker et al., 2010) serves the purpose. Figure 4.14 shows the first stage of the used comparator. Transistors $M_4$ and $M_5$ precharge capacitors $C_{D+}$ and $C_{D-}$ to $V_{DD}$ when $clk$ is low. As soon as the $clk$ goes high, capacitors start to discharge while transistors $M_1$, $M_2$ and $M_3$ pass through saturation and linear regions. Assuming $g_m$ as the transconductance of input transistors and $t$ as the time period during which transistors are in saturation, an expression for gain

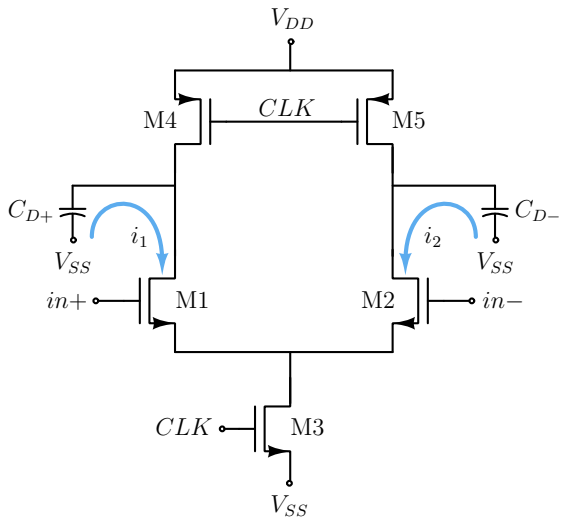



**Figure 4.14:** First stage of double-tail dynamic latched comparator.

of the first stage of the comparator could be written as,

$$A_V = -\frac{g_m t}{C_D}$$

The capacitor size is chosen to be 15 fF. This large size of capacitors improves matching and reduces comparator kickback. The gain $A_V$ is maintained high by increasing the time period $t$. The voltage at the inputs of the comparator settles down to $gnd$ towards the end of conversion. The devices in the comparator circuit are matched to reduce the offset voltage. The comparator consumes very less power due to relaxed gain and bandwidth requirement.

### 4.3.4 Control logic

The SAR control logic consists of a set of DFFs, logic gates and a delay circuit. For an N bit ADC, $N + 2$ number of DFFs are used to form a shift register, as shown in Figure 4.15. When the ADC is turned $ON$, a logic high is inserted at the left most DFF. The same is right shifted in synchronization with the clock and later regained through delay circuit at the start of conversion of new analog input. The same register also receives the data bit from the output of the comparator and right shifts the data bits forming serial to parallel conversion

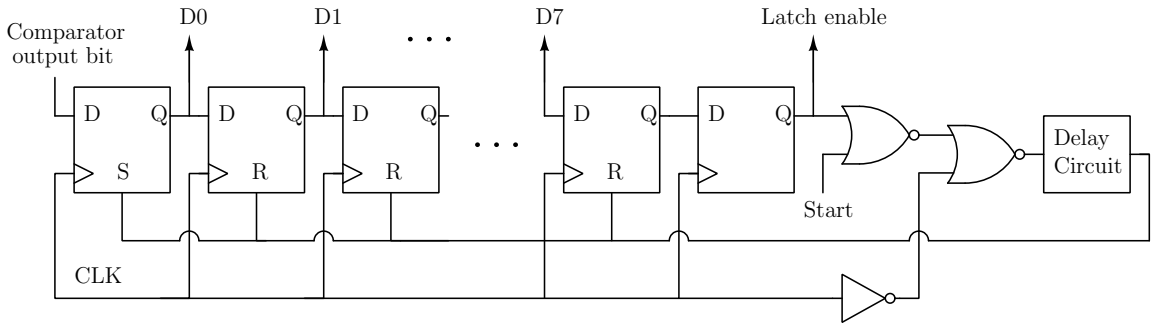



**Figure 4.15:** Circuit diagram of the sequence and data register.

of the data. Upon reaching the end of conversion, the digital equivalent of input analog data is fetched to external circuitry and the flip flop contents are reset as desired. The control logic is used to turn-ON / turn-OFF the switches of the SAR ADC (Figure 4.2). Although the switches appear to be more in number, fewer combinational logic circuit elements are required. The Boolean expressions governing the switch operations, (Figure 4.2), are as follows:

$$\phi 1 = \phi_{reset} \quad ; \quad \phi 2 = \overline{\phi} + \phi_{reset}$$

$$\phi 3 = \overline{B}_{N-1}.\phi.\overline{\phi 1} \quad ; \quad \phi 4 = B_{N-1}.\phi.\overline{\phi 1}$$

where $B_{N-1}$ represent the previous bit output. $\phi$ and $\overline{\phi}$ are the nonoverlapping clock phases. All the required clock phases are derived from a single external input clock signal (Figure 4.3e).

## 4.4 SIMULATION RESULTS

The 8-bit ADC has been designed using 90-nm CMOS process of UMC at ±350 mV supply, the common terminal voltage being the common mode voltage. The ADC operates for analog input voltage spanning full scale rail-to-rail supply voltage. An auxiliary supply voltage of 600 mV is used for increasing gate overdrive of switches. The layout of the ADC is shown in Figure 4.16 and the area occupied is 0.00145 mm$^2$ (57 $\mu$m x 25.5 $\mu$m). Netlist is generated by postlayout extraction for simulation requirements. Noise bandwidth for

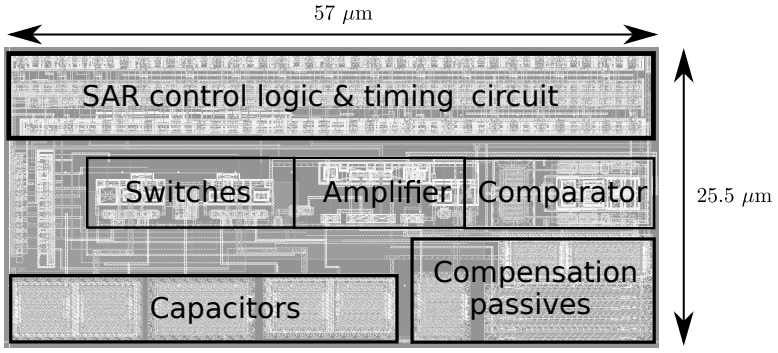



**Figure 4.16:** Layout of the ADC.

simulations is 50 times the sampling frequency.

The complete ADC power consumption is 931 $n$W at sampling frequency of 780 KHz. The power consumption distribution chart is shown in Figure 4.17.

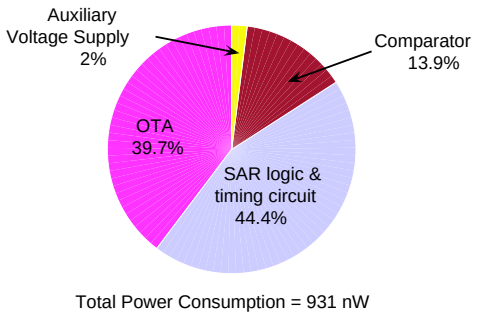



**Figure 4.17:** Power consumption distribution of the ADC.

### 4.4.1 Linearity test of the ADC

Static performance of the ADC is shown in Figure 4.18a. The ADC is tested with a ramp signal to avail 10-points per LSB. The output has no missing codes. The code density plot indicates that the absolute values of both the static nonlinearities are limited below 1 LSB. Dynamic performance of the ADC is verified at its Nyquist input frequency. SNR of the 8-bit ADC is found to be 45.63 dB for the typical Process corner. Close to a value of 1.8 dB loss from an ideal SQNR is due to design decision of having total thermal noise equal to half the quantization error. For the sake of low power consumption, the OTA transconductance

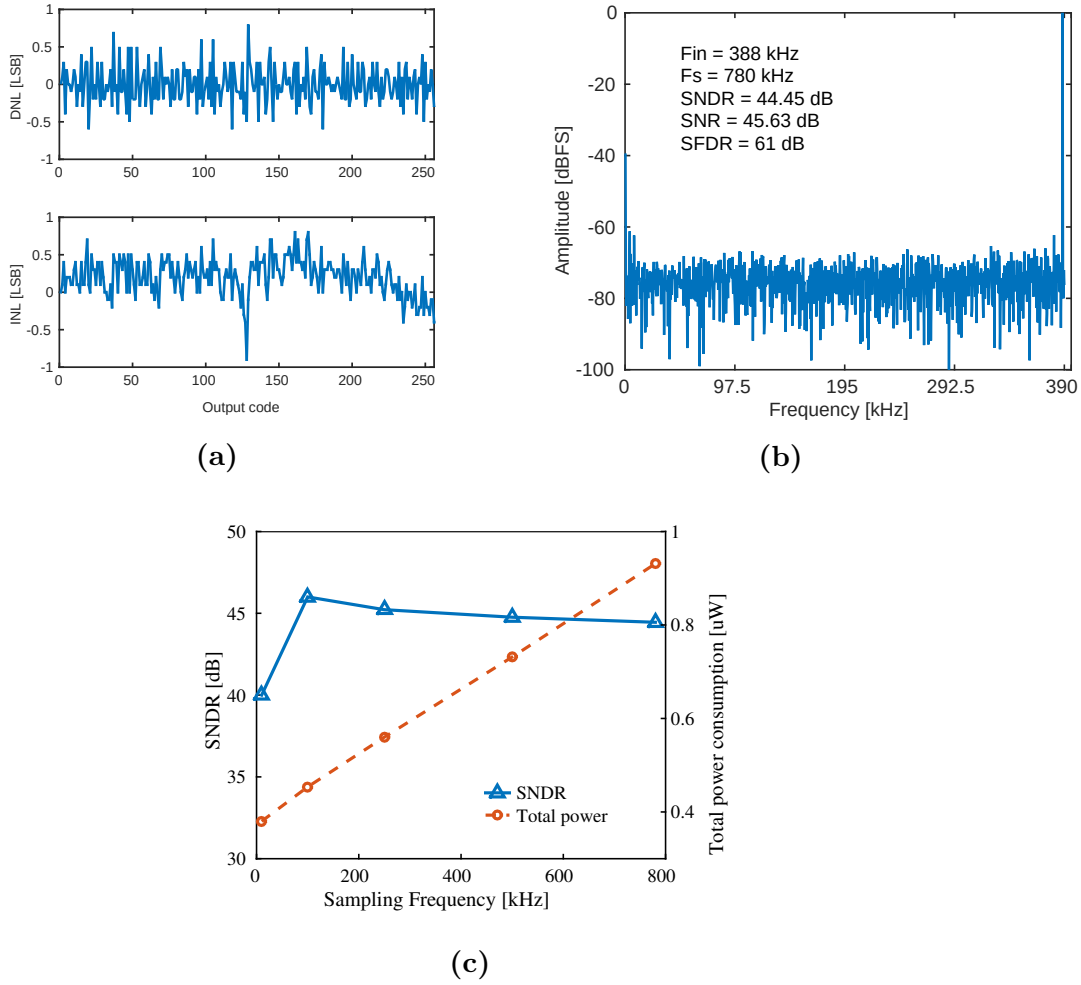



**Figure 4.18:** Plot of (a) Differential and integral nonlinearity (b) FFT spectrum (c) SNDR and total power consumption vs sampling frequency.

is chosen low. The result is large input referred thermal noise of the OTA. Thus the SNR degradation of around 3.5 dB is largely due to the OTA noise. Spectral simulation is shown in Figure 4.18b. The distortion component is close to 1 dB, largely attributed to switch nonidealities. The achieved signal-to-noise-and-distortion ratio (SNDR) of the ADC is 44.45 dB and the spurious-free dynamic range (SFDR) is 61 dB. Table 4.4 summarizes the performance of the ADC. The power consumption by the three blocks of the ADC and the ADC performance is recorded in Table 4.5 for supply voltage variation by ±10%.

Figure 4.18c shows the plot of SNDR and total power consumption of the ADC against the sampling frequency. The SNDR reduces at lower sampling frequencies due to increased

**Table 4.4:** ADC performance summary

| ADC Performance | |
|---|---|
| Technology | 90 nm CMOS |
| Core area ($mm^2$) | 0.00145 |
| Supply voltage (V) | ±0.35 |
| Input range (V) | -0.35 to +0.35 |
| Resolution (bit) | 8 |
| Sampling rate (kS/s) | 780 |
| DNL (LSB) | +0.8/-0.6 |
| INL (LSB) | +0.8/-0.9 |
| SNDR [at Nyquist](dB) | 44.45 |
| SFDR [at Nyquist](dB) | 61 |

**Table 4.5:** ADC performance under supply voltage variation of ±10%

| $V_{DD}$ (mV) | 315 | 350 | 385 |
|---|---|---|---|
| Sampling frequency (kHz) | 390 | 780 | 780 |
| OTA power (nW) | 138 | 369 | 854 |
| Comparator power (nW) | 54 | 129 | 172 |
| SAR power (nW) | 110 | 413 | 340 |
| Total power (nW) | 357 | 931 | 1502 |

charge leakage by the unit capacitors. The change in power consumption is linearly related to change in frequency. For higher frequencies, switching power dominates the total power consumption.

To verify the ADC performance against process variations and capacitor mismatch Monte Carlo simulations of 200 runs are carried on the extracted netlist. Static nonlinearity curves are plotted in Figure 4.19a. The mean and $3\sigma$ DNL errors are 0.87 LSB and 0.54 LSB respectively. In the case of INL the respective error values are 1.37 LSB and 1.59 LSB. Same number of runs are carried out to test dynamic nonlinearity. Figure 4.19b shows the plots of FFT spectrum. The mean and $3\sigma$ values of SNR are 42.16 dB and 1.7 dB respectively. The values agree with the theoretical data. An additional 2.33 dB loss when

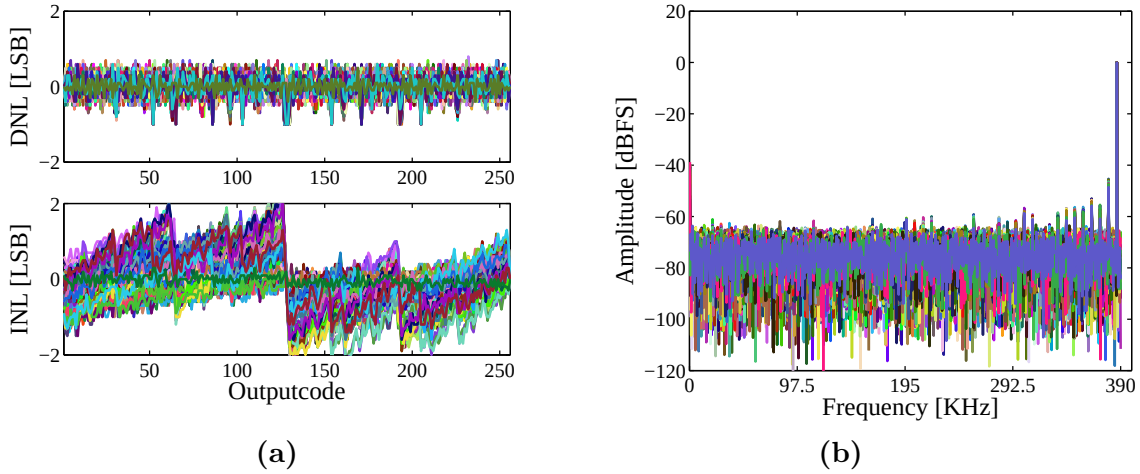



**Figure 4.19:** Statistical distribution of (a) DNL and INL errors (b) FFT spectrum.

compared to typical process corner simulation is largely due to channel charge injection variation experienced at different processes.

For the present size of unit capacitor (30 fF), the achievable mismatch factor is 0.1 %. The impact of capacitor mismatch on conversion accuracy is verified by simulation of the ADC model. The mean SNR and $3\sigma$ SNR deviation against capacitor mismatch (noise and parasitics neglected) are plotted in Figure 4.20. The plot shows that the proposed ADC architecture is capacitor mismatch tolerant to a large extent.

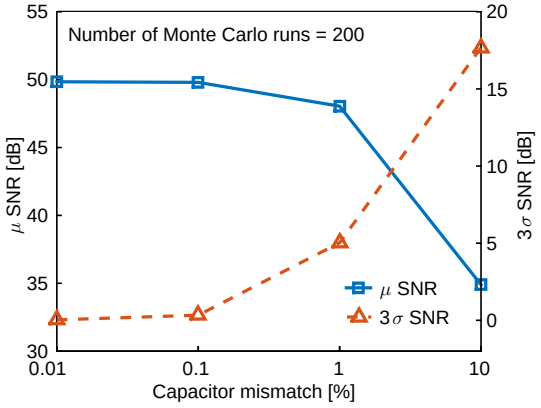



**Figure 4.20:** Mean and $3\sigma$ SNR against capacitor mismatch.

## 4.5 COMPARISON AND DISCUSSION

The ADC is compared with other state-of-art SAR ADC designs in Table 4.6. The proposed

**Table 4.6:** ADC performance comparison

| | Harpe *et al.* (2014) | Yoshioka *et al.* (2014) | Chen *et al.* (2015) | Lin (2017) | This work |
|---|---|---|---|---|---|
| Supply voltage (V) | 0.8 | 0.4 | 0.7 | 0.3 | ±0.35 |
| Process (nm) | 65 | 40 | 65 | 90 | 90 |
| Sampling rate (MS/s) | 0.128 | 1.02 | 0.1 | 0.15 | 0.78 |
| Power (W) | 1.367$\mu$ | 710n | 645n | 67.3n | 931n |
| ENoB (bit) | 12.35 | 7.18 | 10.5 | 8.85 | 6.71 |
| Core area ($mm^2$) | 0.18 | 0.0153 | 0.03 | 0.031 | 0.00145 |
| FoM (fJ/c-s) | 8.2 | 4.8 | 4.5 | 0.97 | 11.39 |
| AE ($\mu m^2$/code) | 34.48 | 105.5 | 20.72 | 67.18 | 13.85 |

ADC shows good area performance and at the same time competitive with energy efficiency. The AE is 13.85 $\mu m^2/code$ and the FoM of the ADC at 780 kS/s is 11.39 $fJ$/conv-step. A 2 bit/step design in Yoshioka et al. (2015) shows improvement in energy efficiency. Multiple threshold configuring comparators are used. The thresholds of comparators are dynamically varied by employing voltage control sources. Successive activation of comparators halve the DAC settling time. But the added complexity costs in terms of area occupied. Chen et al. (2015) employs statistical estimation method by performing several repeated measurements to evaluate LSB. This will help in reduction of both comparator and quantization noise of the ADC. However, to do so, large number of clock cycles are required. As already cited in previous chapter, Harpe et al. (2014) uses dithering of DAC, chopping and data driven noise reduction techniques with oversampling scheme. Unit capacitors are custom designed to deliver low power consumption in capacitor arrays and dithering overcomes the capacitor mismatch. The offset and even order harmonics are reduced using chopper circuits, while quantization noise is averaged out with the help of data driven noise reduction technique. The ADC is oversampling for obtaining high resolution and hence low bandwidth, the same may impose a significant overhead for lower resolutions. The first 2-bit guess scheme is

proposed in Lin and Hsieh (2017) to reduce the DAC switching power. The scheme also relaxes the unit capacitor matching requirement by reducing the standard deviations of static nonlinearities.

In the proposed, again a low power and area-efficient ADC is designed. The DAC is non-binary and consumes insignificant power. Area efficiency in this case is obtained by relying on analog blocks. Thermal noise is reduced by reduced gain of the switched capacitor integrator. The ON-state switch resistance is lowered by using an auxillary supply voltage. Operation of the ADC at low voltage is supported by threshold voltage reduction of MOS transistors, wherein body terminals are slightly forward biased. As with the previous ADC design, the unit capacitor array occupies smaller portion of the ADC layout (refer Figure 4.16).Noise is traded for power and the achieved linearity is typical as any other SAR ADC designs. ENoB is close to 1 bit less than the theoretical 8 bits. The ADC is compared with the other published ADCs at ISSCC (during 1997-2016) in Figure 4.21. The performance of the implemented ADCs is well captured in Figure 4.21c, wherein the graph takes power, speed, resolution and area into account. The performance (area against FoM) of the two ADCs presented in this thesis is clearly superior to the recently published data.

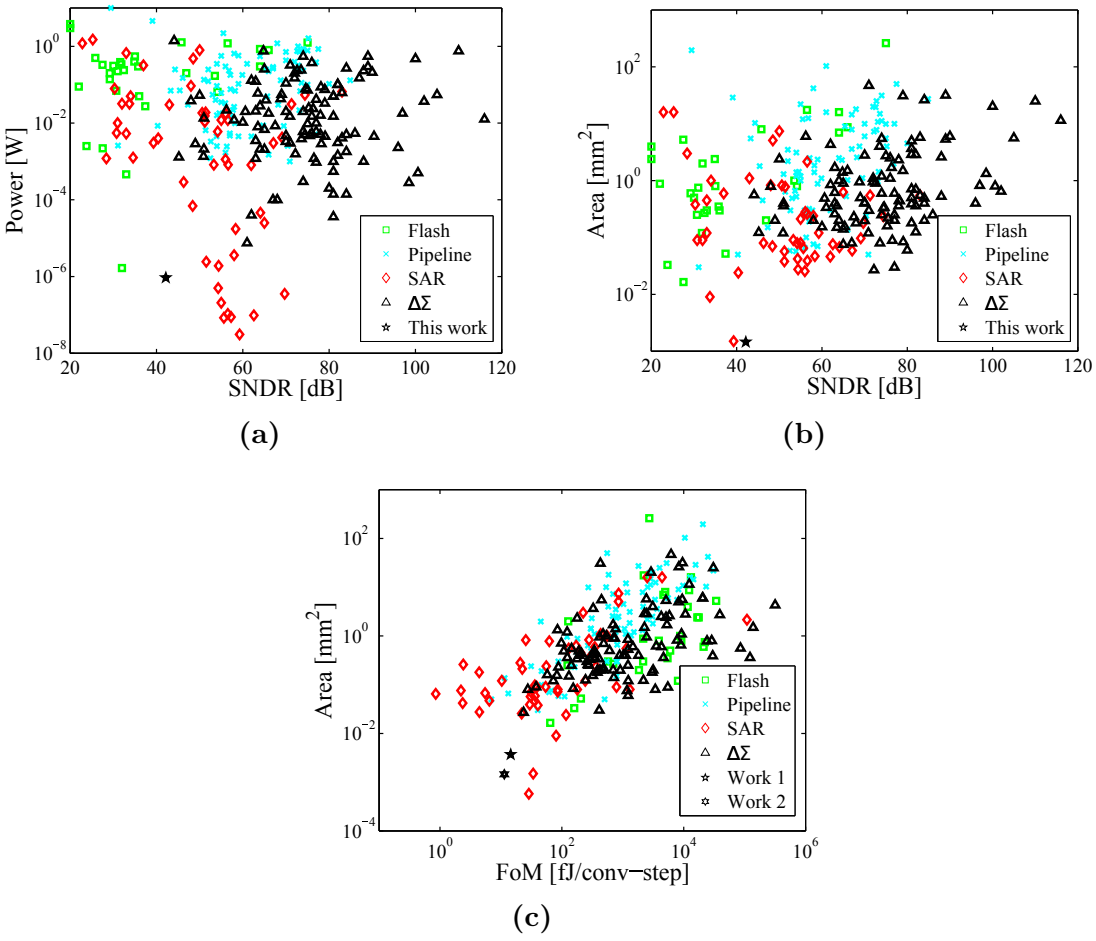



**Figure 4.21:** Performance of the implemented ADC against published ADCs at ISSCC (during 1997-2016).

# Chapter 5

# NOISE-SHAPING SAR ADC

An oversampling ADC trades speed for resolution. However, it will be a significant advantage if the inband noise is shaped away during oversampling. A $\Delta\Sigma$ ADC achieves this. The $\Delta\Sigma$ modulator will essentially have a quantizer, a feedback DAC and a loop filter. For a higher resolution, the modulator may use either a multi-bit quantizer or a higher-order loop filter or both. A higher-order loop filter demands multiple integrators (other than integrator within a quantizer). The number of such integrators required will be equal to the order of the loop filter. In this chapter, noise-shaping schemes using an SC integrator based SAR ADC are proposed. The proposed second-order SAR ADC is realized using no additional integrator circuit, but for few capacitors. First, a low noise and less parasitic sensitive SAR quantizer architecture is proposed. The quantization error residue is sampled into residue capacitors and later fed back to realize noise-shaping function. The residue feedback scheme is simple and can suitably modified to realize a bandpass or a highpass ADC (Nguyen et al., 2006). The proposed noise-shaping technique could as well be adopted in any multi-bit $\Delta\Sigma$ ADC that uses SC SAR ADC as its quantizer. The quantizer is differential in operation and similar to the proposed ADC architecture in section 4.1. Due to high resolution requirement, the unit capacitor size is large, thus leading to variation in amplifier and timing circuit specifications. In this chapter, the emphasis is not to redesign the architecture components, but to provide a proof of concept of noise shaping attribute of the proposed ADC. The modulator is modelled and non-idealities, such as, capacitor

mismatch, switch parasitics and noise are included. Since the architecture is similar to the one presented in the chapter 4, the voltage dependent parasitics estimated for architecture presented there are also incorporated with this model. All results presented in this chapter pertains to simulation of the model alone.

## 5.1 SAR ADC

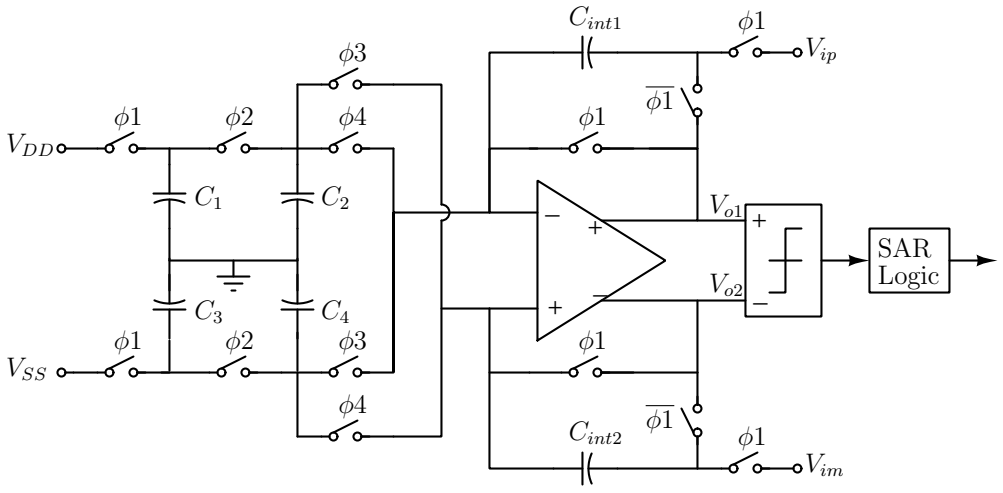



**Figure 5.1:** Differential architecture of the SAR ADC.

Since the $\Delta\Sigma$ ADC performance is highly dependent on linearity characteristics of the multi-bit DAC, improvements to the ADC architecture are highly desirable. A straightforward approach for linearity improvement would be to use a differential architecture as shown in Figure 5.1. Notably the ADC has two integrating capacitors $C_{int1}$ and $C_{int2}$. The ADC now samples differential inputs $V_{ip}$ and $V_{im}$. Capacitors $C_2$ and $C_4$ will discharge to *gnd* by transferring acquired charges to integrating capacitors. Although channel charge injection error could be reduced to zero due to differential architecture, the noise power gets doubled. Presence of even small offset error would drift the integrator output common mode voltage, away from *gnd*, eventually leading to nonlinear characteristics. The processing of the SC integrator residue charge by an external circuit is very limited. Due to this, when the ADC is used as quantizer in a $\Delta\Sigma$ modulator, the quantization noise shaping will be

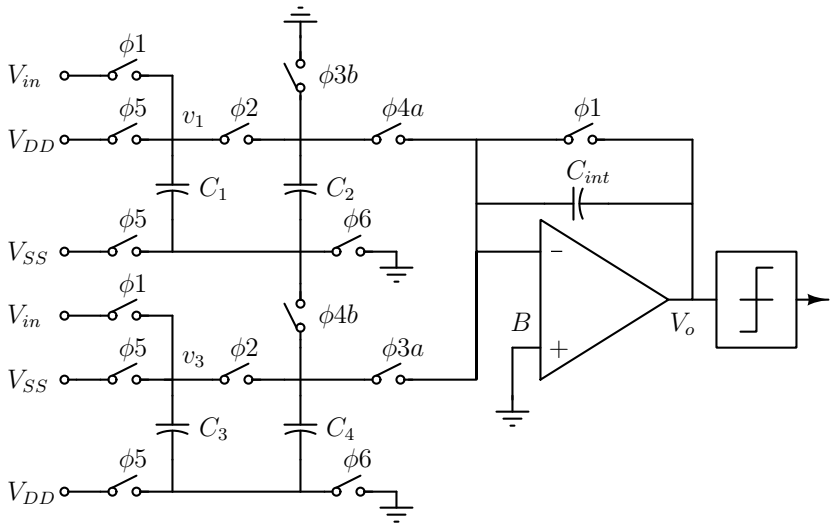



**Figure 5.2:** Proposed architecture of SAR ADC

restricted only to a first order. Hence another variant of the ADC architecture presented in section 4.1 is shown in Figure 5.2.

Distinctly, the input voltage is sampled on to unit capacitors $C_1$ to $C_4$ and the input equivalent charge is thereafter transferred to integrating capacitor $C_{int}$. As a result capacitor matching is confined to unit capacitors alone. The integrating capacitor size is quadrupled to reduce integration gain to $\frac{1}{4}$ and therefore the noise power at the integrator output is attenuated by a factor of 16. This reduction in noise power significantly reduces the oversampling ratio (OSR) requirement for a given resolution and speed. The proposed SAR quantizer is similar to the presented ADC in section 4.1. The ADC has an SC integrator, two passive charge sharing circuits, a comparator and a SAR logic block.

### 5.1.1 Operation

For an N bit ADC, the conversion happens in N clock cycles. The clock phases are nonoverlapping. Each clock cycle constitutes a charge sharing and a charge integration phase. Nominally, $C_1 = C_2 = C_3 = C_4 = C$ and $C_{int} = 4C$. Supply voltage $V_{DD} = -V_{SS} = V_{ref}/2$ with common mode voltage at *gnd*. Following describes the step-by-step operation. Step 1 is performed once at the beginning of every conversion cycle, while steps 2 and 3 are exe-

cuted N times for an N bit conversion. All the phases remain low unless explicitly specified.
1. *Sampling:* During first clock cycle, phases $\phi1$, $\phi2$ and $\phi6$ raise, so as to sample input $V_{in}$ to $C_1$, $C_2$, $C_3$ and $C_4$ (Figure 5.3a). Later in the cycle, the sampled charges are transferred to $C_{int}$ by raising phases $\phi2$, $\phi6$, $\phi3a$ and $\phi4a$ (Figure 5.3b). Output voltage $V_o = -V_{in}$. At the begining of second clock cycle, phases $\phi2$ and $\phi5$ raise, so as to sample $V_{ref}$ to $C_1$, $C_2$, $C_3$ and $C_4$ (Figure 5.3c).
2. *Passive charge sharing and comparison:* Phases $\phi2$ and $\phi6$ raise. $C_1$ and $C_2$ share charge, so do $C_3$ and $C_4$ (Figure 5.4a). Meantime $V_o$ is compared against *gnd*, the half-way mark in $V_{ref}$ range. If $V_o$ is positive, MSB=0. Otherwise MSB=1.
3. *Charge integration:* Based on the obtained MSB either $C_2$ or $C_4$ will transfer charge to $C_{int}$. For MSB=0, $\phi6$ and $\phi4_{a,b}$ raise, leading to transfer of charge from $C_2$ to $C_{int}$ (Figure 5.4b). Otherwise, $\phi6$ and $\phi3_{a,b}$ raise, to transfer charge from $C_4$ to $C_{int}$ (Figure 5.4c). The other capacitor, not involved in charge transfer ($C_4$ if MSB=0, else $C_2$), will discharge to *gnd*. The new output voltage $V_o = -V_{in} - (-1)^{MSB}V_{ref}/4$.
4. The remaining bits are similarly determined by following steps $2-3$.

## 5.2 NOISE-SHAPING TECHNIQUE

In the case of low frequency input signals, the residue charge left over after the conversion will remain on $C_{int}$ if the capacitor is not reset. The residue charge, if fed back, can be used to achieve noise attenuation. The residue charge on $C_{int}$ is equivalent to a NTF of $(1-Z^{-1})$. An activity as simple as non-resetting of $C_{int}$ will attenuate the noise by first-order. To achieve a higher noise attenuation, the residue voltage is to be extracted, saved and fed back. A second order noise-shaping technique is illustrated here. The residue voltages (residue charges) of two successive conversions are fed back to have the NTF equal to $(1 - Z^{-1})^2$. The topology is based on error feedback scheme (Schreier and Temes, 2005) and is shown in Figure 5.5.

The proposed residue feedback circuit for a second-order noise shaping SAR is shown in Figure 5.6a. The circuit has two residue sampling capacitors, $C_{R1}$ and $C_{R2}$, in feedback. The resetting of $C_{int}$ is done once, only when ADC is powered up. All switches shown in

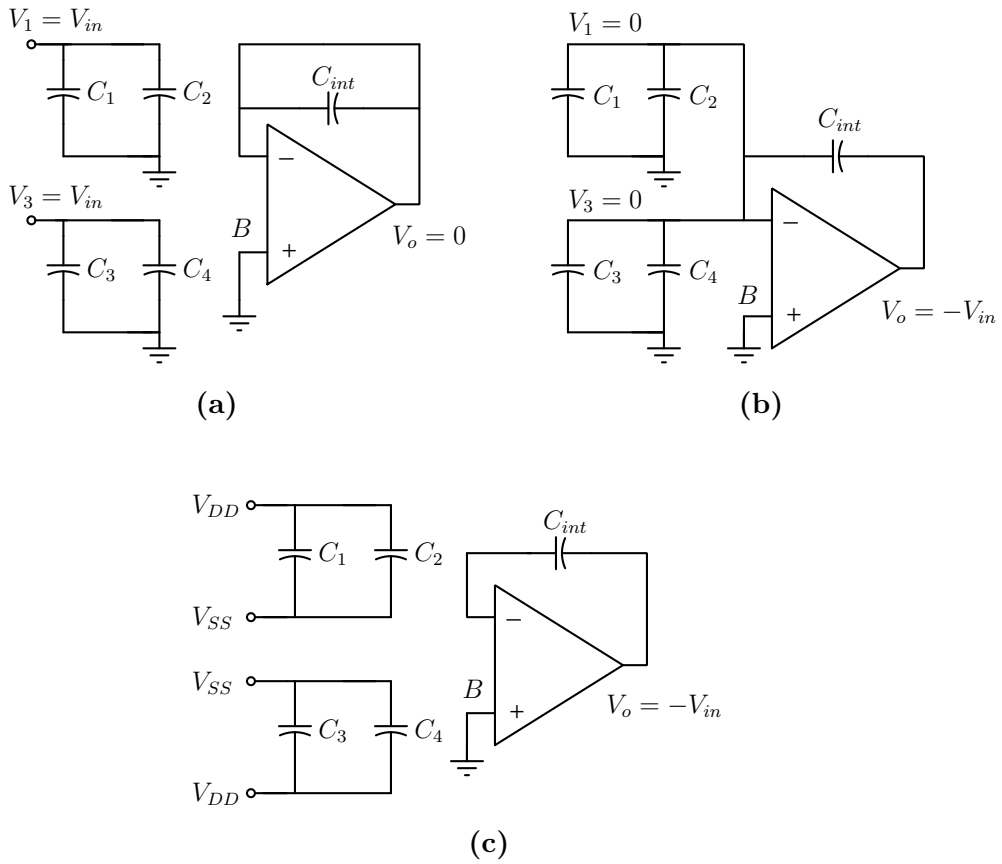



**Figure 5.3:** Step 1: proposed SAR ADC during sampling phase

Figure 5.6a operate only during input sampling clock phase. Following is the step-by-step operation, in addition to those mentioned earlier in subsection 5.1.1:

1. *Residue extraction:* while ADC samples the input $V_{in}[n]$, phases $\phi 7$ and $\phi 9$ raise to sample quantization error voltage $V_{in}[n-1] - V_{DAC}[n-1]$ to $C_{R1}$(Figure 5.7a). ($C_{R2}$ would have similarly sampled $V_{in}[n-2] - V_{DAC}[n-2]$ during sampling of input $V_{in}[n-1]$, by raising phases $\phi 8$ and $\phi 9$).

2. *Residue feedback:* while sampled input equivalent charge is being integrated to $C_{int}$, phase $\phi 11$ raises (Figure 5.7b). Voltage at node B, say $V_b = e[n-1] - e[n-2]$. Soon after, $\phi 9$ raise and $V_o = -V_{in}[n] + 2e[n-1] - e[n-2]$. For rest of the conversion clock cycles, $\phi 9$ remain raised.

At the next conversion cycle, same steps are repeated, but the roles of the two residue

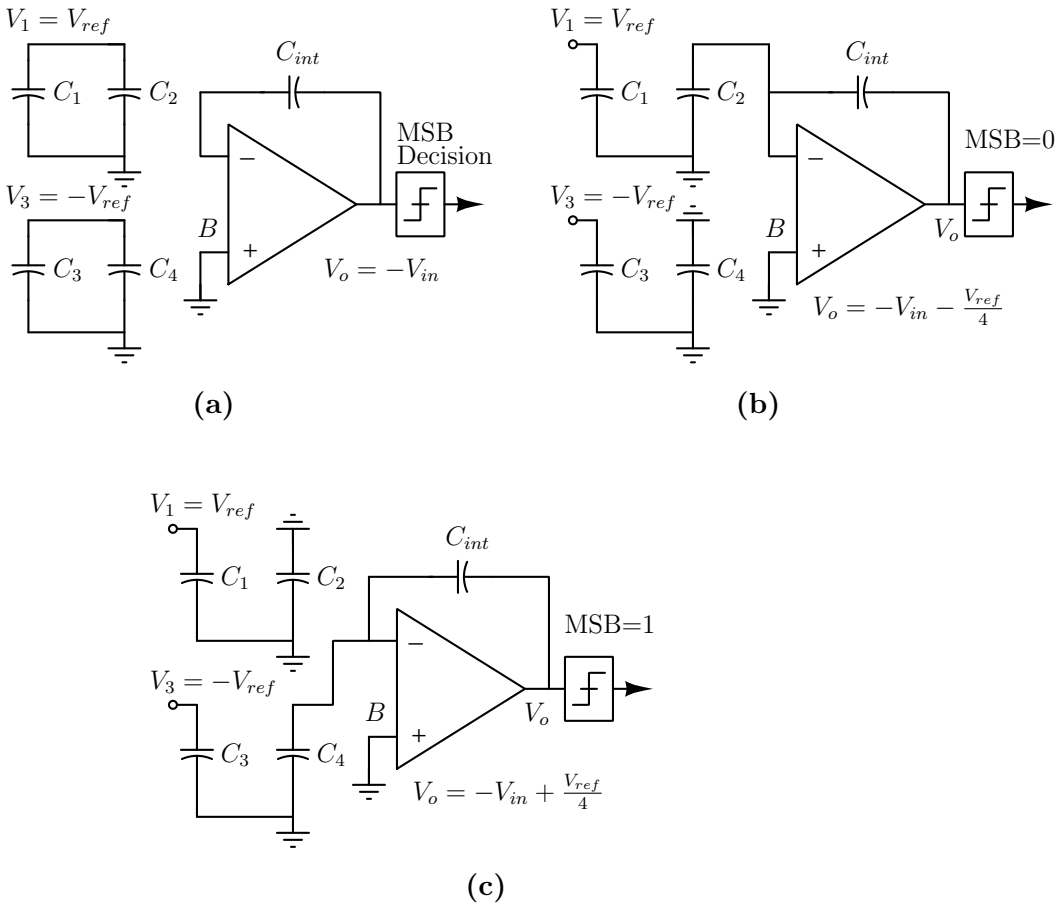



**Figure 5.4:** Steps 2 and 3: proposed SAR ADC during charge sharing and integration phases

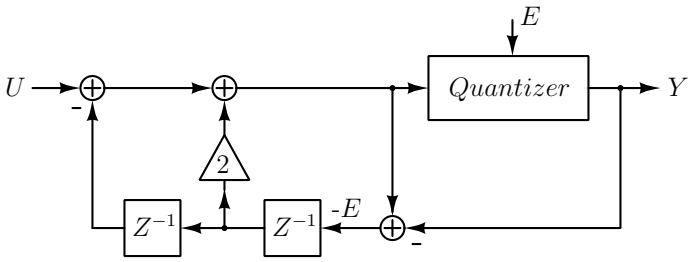
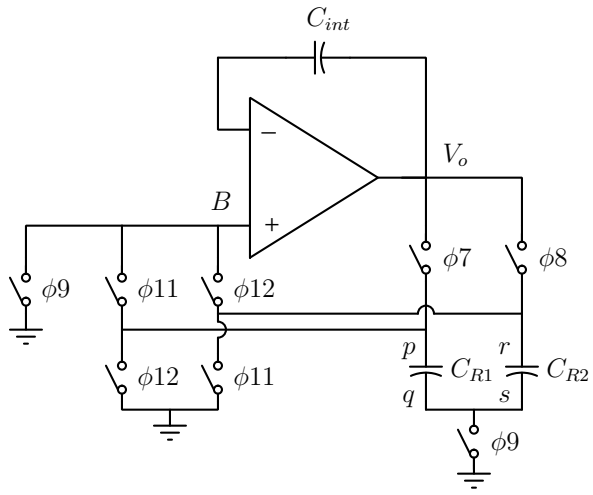


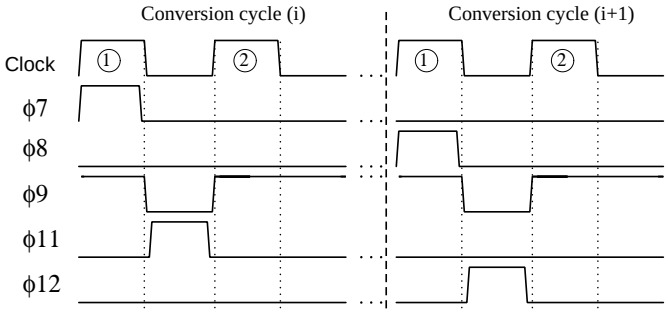

**Figure 5.5:** The error feedback topology

capacitors are now reversed. The required timing diagram for residue feedback is shown in Figure 5.6b.

The technique does not demand feedback capacitors to be matched in size, but the switch




**(a)**




**(b)**

**Figure 5.6:** (a) Residue feedback circuit for $2^{nd}$ order noise-shaping (b) Timing diagram

nonidealities have to be addressed. Quantization noise voltage will be in smaller magnitude in comparison to a voltage change across feedback capacitor due to channel charge injection. Therefore switch design should thoroughly implement channel charge error cancellation techniques, such as usage of complementary transmission gates and dummy transistors. The switch parasitics have minimum impact on feedback as the voltage variation across them is very small. Performance evaluation of the ADC under feedback variation is carried in subsection 5.6.1.

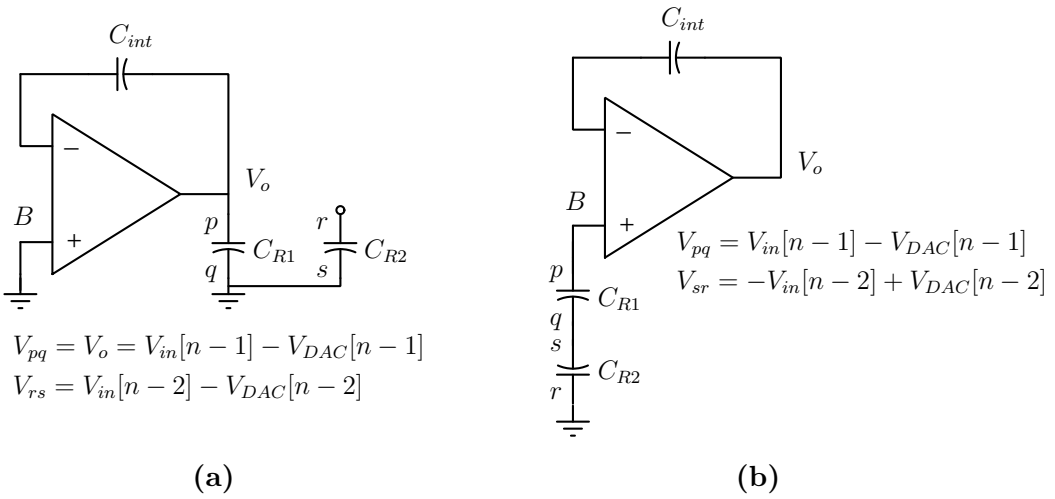



**Figure 5.7:** Steps 1 and 2: error feedback operation in noise-shaping SAR ADC

## 5.3 HIGHPASS AND BANDPASS ADC

A highpass and a bandpass ADC could also be realized by noise-shaping technique, presented earlier. Respective NTFs are $(1+Z^{-2})$ and $(1-Z^{-2})$. To realize such functions, the quantization error $(V_{in}[n-1] - V_{DAC}[n-1])$, stored in $C_{int}$, needs to be eliminated and error $(V_{in}[n-2] - V_{DAC}[n-2])$ needs to be fed back. Step$-2$ of noise-shaping technique is modified as follows. For highpass, terminal $r$ in Figure 5.8a is connected to op-amp, while $p$ is grounded. $V_o = -V_{in}[n] + e[n-2]$. In case of bandpass, reversal of terminals of $C_{R1}$ (by suitable switching) is required (Figure 5.8b). $V_o = -V_{in}[n] - e[n-2]$.

The presented noise-shaping technique could also be extended to further the noise-shaping order. The number of residue capacitors required depends on order and coefficients of NTF. The coefficients could be modified by passive multiplication (capacitors sample error and later placed in series) and division (capacitors sample error and later placed in parallel to share charge). However, the performance will be limited by parasitics.

## 5.4 CAPACITOR MATCHING

With an 8 bit quantizer, second order $\Delta\Sigma$ modulator and OSR of 32, the maximum SQNR is 112.3 dB (refer (2.43)). A thermal noise analysis of the quantizer is similarly done as in

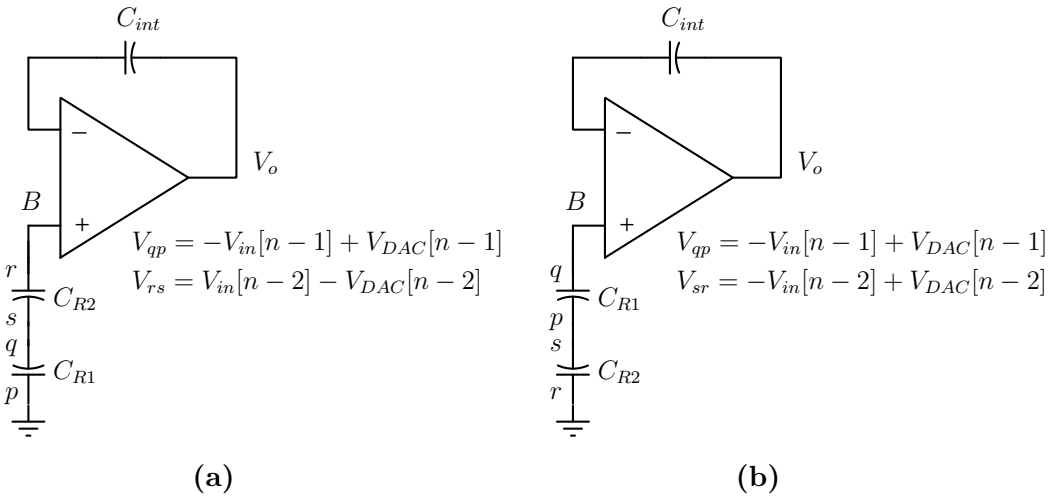



**Figure 5.8:** Step 2: feedback circuit operation in highpass and bandpass SAR ADC

subsection 4.2.1. The in-band quantization noise power is as given in (2.41).

A similar assumption on capacitor size variations is made as in subsection 4.2.2. The error voltage $\varepsilon$ due to mismatch is expressed here as (refer to the derivation of (4.11); but two changes are to be considered. $C_{int}$ is free from matching requirement and integrator gain is $\frac{1}{4}$.)

$$|\varepsilon| \approx q\alpha \sum_{k=1}^{N-1} \frac{1}{2^{k+1}} \left[ \Big( B_{N-k} - \overline{B}_{N-k} \Big)(k-2) \right] \tag{5.1}$$

In (5.1), the term $(B_{N-k} - \overline{B}_{N-k})$ is zero for $k = 2$ and bear difference in sign for $k \geq 2$. Thus the value of $\varepsilon$ will be maximum for mid-point and quarter-points of the output code. For such a code, say 0111...1, the error voltage is obtained as

$$|\varepsilon_{max}| \approx q\alpha \left[ \frac{1}{2^2} + \frac{0}{2^3} + \frac{1}{2^4} + \frac{2}{2^5} + ... + \frac{N-3}{2^N} \right]$$

Summing the arithmetico-geometric series within,

$$|\varepsilon_{max}| \approx q\alpha \left[ 0.5 - \left( \frac{1}{2} \right)^N (N-1) \right] \tag{5.2}$$

Again, with substitutions and as N is large, (5.2) could be simplified as

$$\frac{|\varepsilon_{max}|}{V_{ref}} \approx 0.5\frac{\sigma_u}{C_u} \tag{5.3}$$

With $B$ bits in quantizer and $\epsilon_{max}$ equal $k$ LSB,

$$\frac{k}{2^B} \approx 0.5\frac{\sigma_u}{C_u} \tag{5.4}$$

Capacitor matching requirement obtained in (5.4) is for quantizer alone. For the $\Delta\Sigma$ modulator with oversampling, the same is

$$\frac{k}{2^N}\sqrt{OSR} \approx 0.5\frac{\sigma_u}{C_u} \tag{5.5}$$

where N is the total resolution bits of $\Delta\Sigma$ ADC. Further, the equation could be written to compare with matching requirement of quantizer as

$$\frac{k\sqrt{OSR}}{2^B.2^{(\frac{2L+1}{2}\log_2 OSR)}} \approx 0.5\frac{\sigma_u}{C_u} \tag{5.6}$$

The requirement demands a large value of unit capacitors when high resolution is desirable. The DEM technique, when employed, averages out the random mismatch and provides a better performance. However, the averaging of random mismatch do not lead to an optimum performance. An alternative solution would be to sort the unit capacitors, say in an ascending order, and later assign roles to these capacitors. Once a sort is done, the first and the third capacitor form a pair of unit capacitors for sharing of charge; the second and the fourth capacitor forms the other pair. The second and third capacitors are

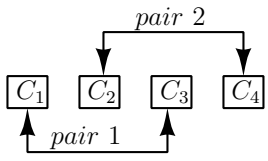



**Figure 5.9:** Pairing of sorted unit capacitors.

meant for active charge transfer. A represention is shown in Figure 5.9. For the second order noise-shaping topology, the method is able to achieve a 6 dB improvement in SNR when compared to the DEM technique.

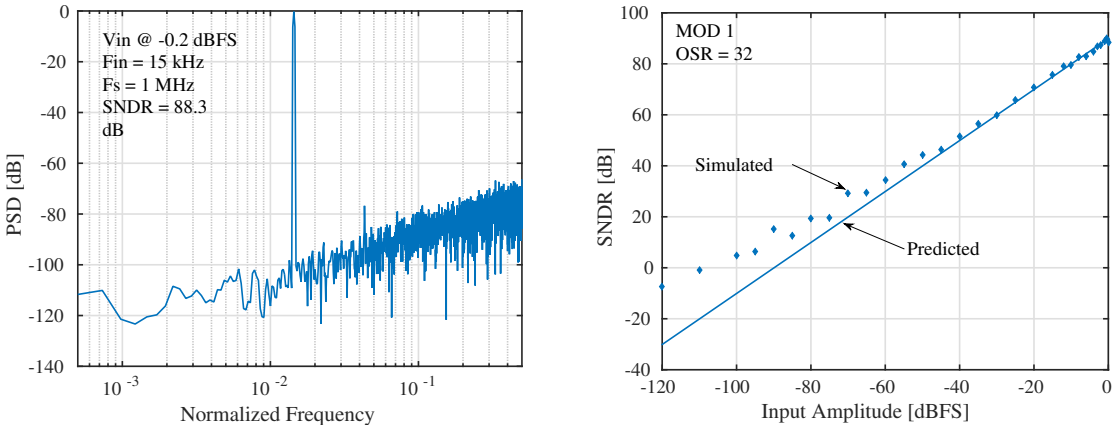
## 5.5 COMPARISON

A similar SC technique based SAR ADC is proposed by Chen et al. (2013). Their technique is limited to first order $\Delta\Sigma$ ADC and takes two integrations per bit, leading to slow conversion speed and noise accumulation at integrator output (Schreier et al., 2005). However, our proposed ADC attenuates noise by 15 dB more in comparison to Chen et al. (2013) (due to single integration per bit and gain of $\frac{1}{4}$). Owing to the second order NTF of the proposed ADC, the SNR achieved is far higher compared to Chen et al. (2013). Additionally, the proposed technique also realizes highpass and bandpass ADCs.

Noise-shaping techniques are also presented for SAR ADC involving traditional binary weighted capacitor arrays (Kim et al., 2010, Fredenburg and Flynn, 2012). These ADCs require additional integrator circuit to realize noise-shaping feature.

## 5.6 SIMULATION RESULTS

An 8 bit SAR quantizer with a unit capacitor size of 1 pF is modelled. The ADC is energized by a $\pm$0.35 V dual power supply voltage source. The OSR is set to be 32. The model included switch parasitics and nonidealities. Capacitor mismatch is assumed to be well below 0.1%, which is very common in sub-micron technologies. The quantizer takes 9 internal clocks for conversion and is able to provide an SNDR of 49 dB, largely attributed to good capacitor matching and low noise. A -0.2 dBFS input signal at 15 kHz is sampled at 1 MHz. The presented results are the average of the 500 Monte Carlo runs. First, the simulation results of first order $\Delta\Sigma$ are presented in Figure 5.10. The predicted values of maximum SQNR could be obtained from (2.43). The simulated mean SNDR is 88.3 dB. For the obtained SNDR, the unit capacitor are of large enough size to meet the noise and matching requirements. SNDR vs input amplitude plot shows good matching between




**(a)** **(b)**

**Figure 5.10:** Simulated (a) power spectral density and (b) SNDR vs input amplitude of first order $\Delta\Sigma$ ADC.

simulated and predicted values for higher amplitudes. The SNDR of first order modulator is an erratic function of the input amplitude and frequency (Schreier and Temes, 2005).

Simulation results of second order lowpass $\Delta\Sigma$ are presented in Figure 5.11. The mean SNDR is 101.2 dB. SNDR vs input amplitude plot shows the simulated SNDR values placed below the predicted maximum values by nearly 10 dB. The chosen unit capacitors of 1 pF, fall below in their value to meet noise and matching requirements needed for higher SNDR. For the desirable resolution, the feedback DAC is nonlinear. But the distortions are out of band and hence unaccounted in plots shown in Figure 5.11a and Figure 5.11b. To account distorion effects, the input frequency is lowered and the obtained SNDR values are plotted in Figure 5.11c. The third harmonic component falls into the band when the input frequency to sampling frequency ratio falls below $\frac{1}{6}$. The SNDR continues to deteriorate further when higher order harmonics fall within the in-band range.

The bandpass ADC is simulated with an input signal of frequency close to $\frac{f_s}{4}$. The obtained mean SNDR is 81.7dB and its output spectrum is as shown in Figure 5.12a. The second order bandpass and highpass ADC have a single NTF zero at intended frequency and hence lends performance similar to that of first order $\Delta\Sigma$ ADC. The simulated power spectral density plot of the highpass ADC is shown in Figure 5.12b. The obtained mean SNDR at an input frequency close to $\frac{f_s}{2}$ is 78.4 dB.

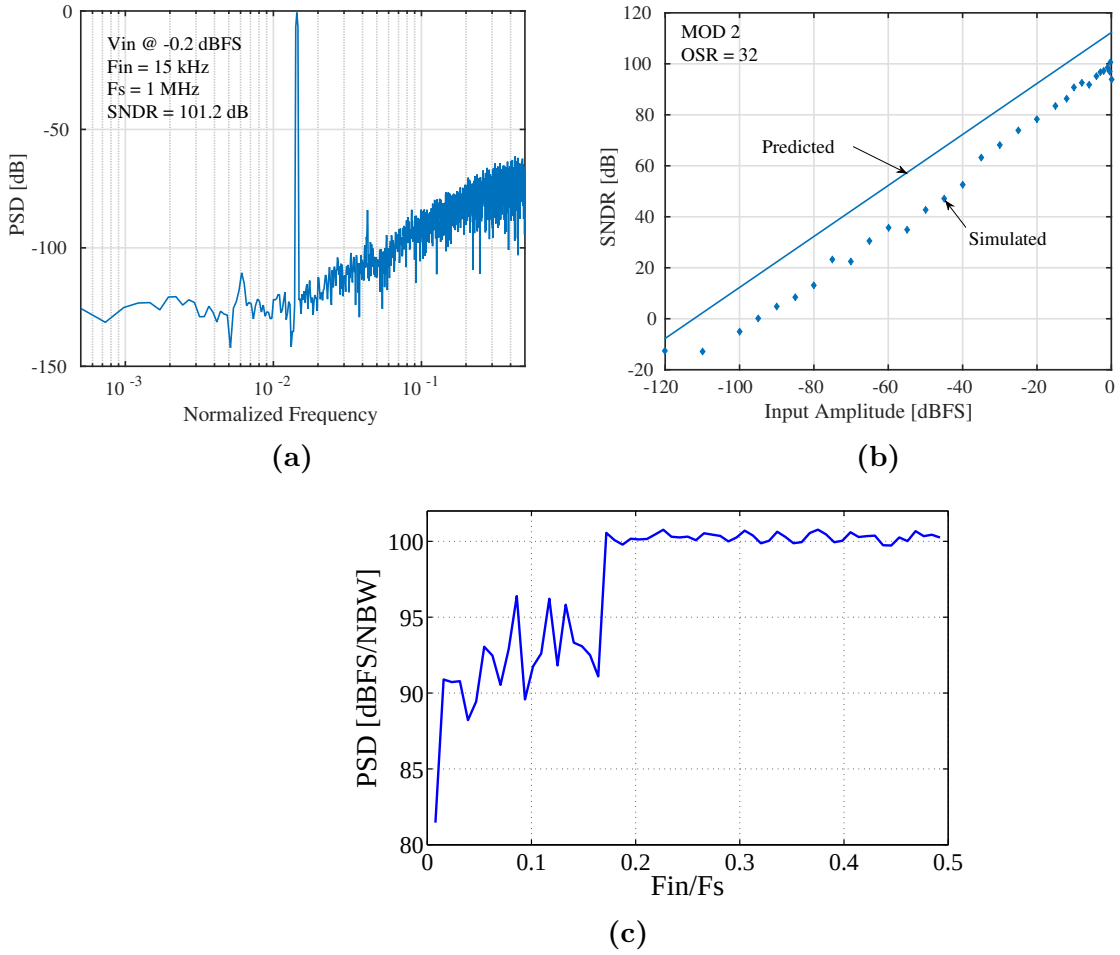



**Figure 5.11:** Simulated (a) power spectral density (b) SNDR vs input amplitude and (c) SNDR vs input frequency of second order $\Delta\Sigma$ ADC.

### 5.6.1 Sensitivity to feedback variation

A practical second order NTF could be written as

$$NTF = 1 - 2\alpha_1 Z^{-1} + \alpha_2 Z^{-2}$$

$\alpha_1$ and $\alpha_2$ are feedback coefficients representing variation from the ideal. Such variation is basically caused due to switch nonidealities (discussed in section 5.2). The zeroes of the NTF are at $Z_1 = \frac{\alpha_1+\sqrt{\alpha_1^2-4\alpha_2}}{2}$ and $Z_2 = \frac{\alpha_1-\sqrt{\alpha_1^2-4\alpha_2}}{2}$. Typical value of $\alpha_1$ and $\alpha_2$ is 1. However, any variation in these values result in zeroes placed either away from Z-plane unit

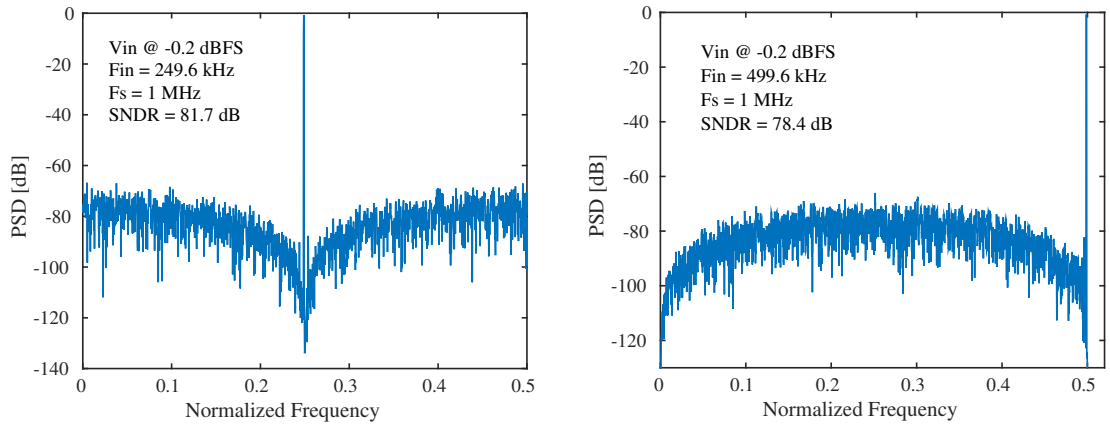



**Figure 5.12:** Simulated power spectral densities of proposed noise-shaping ADC

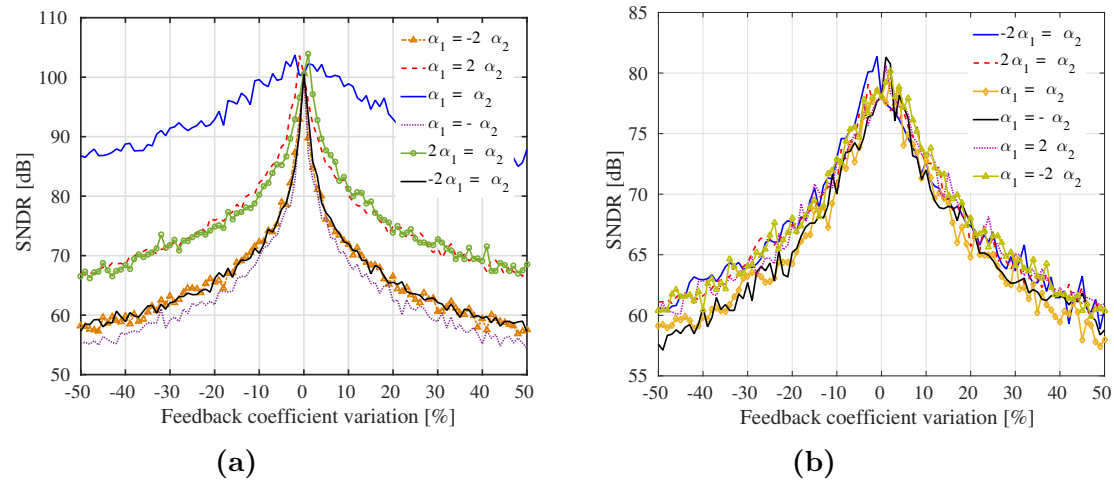



**Figure 5.13:** SNDR vs feedback coefficient variation for (a) lowpass and (b) bandpass ADC.

circle or away from intended frequency or both. A simulation study is carried, wherein the coefficients are varied and the respective SNDR values are computed. Figure 5.13 shows the plot of SNDR against feedback coefficient variation for the second order $\Delta\Sigma$ ADC. The desirable coefficients variation would be that $\alpha_1$ and $\alpha_2$ have same magnitude and sign. The SNDR degradation is severe when the two differ in their sign. However not much difference is noticed in case of BP ADC.

# Chapter 6

# CONCLUDING REMARKS AND FUTURE WORK

## 6.1 CONCLUSIONS

In this thesis, two novel ultra-low-power and area efficient SAR ADC architectures employing nonbinary capacitor arrays are introduced. The ADCs are designed and implemented in 90 nm CMOS process of UMC library. Nonbinary capacitors in the architectures show good matching. Adoption of passive sharing of charge between the capacitors, to generate required DAC equivalent voltage, greatly reduces the power consumption in the capacitor array. The parasitic on charge sharing nodes is designed to be small and equal. The parasitic variation is reduced by means of good switch design and smaller voltage swing. Despite the presence of the parasitics, higher amount of accuracy in sharing of charge between capacitors is achieved.

In the first work, two CAs operate in tandem with simultaneous switchings and therefore adds complexity and power dissipation at the controller circuit end. This shift in complexity is welcomed as more sophisticated low power design techniques are available in the digital domain. The performance limitation comes from the comparator input terminal parasitics, which however more than meets the thermal noise and capacitor mismatch requirements. The designed ADC occupies an area of 0.00371 $mm^2$. When excited with 1 V power supply,

the ADC consumes 473 nW of power and delivered 8.35 ENoB at 100 kS/s with a FoM of 14.5 fJ/c-s. Since the power consumption is mainly due to digital circuits, the power consumption scaled linearly with the sampling frequency.

In the second work, a switched capacitor integrator is used to generate the DAC equivalent voltage. A dual power supply source and two separate passive charge sharing blocks enhanced the conversion speed and assisted in the reduction of integrator gain at ease. The architecture, itself being low noise, achieved low power dissipation and low area by allowing a noisy OTA. Further, the integrator is designed in a subthreshold region to reduce power dissipation. The designed ADC occupies an area of 0.00145 $mm^2$. The ADC consumed 931 nW when operated with $\pm$0.35 V supply and delivered 6.71 ENoB at 780 kS/s with a FoM of 11.39 fJ/c-s. The OTA draws a fixed DC bias current. The power consumption of the OTA does not scale down as the sampling frequency is lowered and hence not suggestive to operate at lower sampling frequencies. Both the ADCs are robust against mismatch and PVT variations. The same is verified by Monte Carlo simulations of the modelled ADCs.

The residue charge left within the integrator of proposed ADC in second work is taken advantage to realize quantization noise shaping. The proposed residue feedback techniques realize a first and several second order lowpass, bandpass and highpass ADCs. The technique is passive by nature and demands no additional active circuit. However, the size of the unit capacitor is now increased to reduce DAC nonlinearity. The modelled ADC linearity is validated with the help of Monte Carlo simulations.

## 6.2 FUTURE WORK

Advances in IC design and VLSI are giving opportunities to a plethora of new applications in the fields of biomedical electronics, wireless sensors and communications, consumer electronics and much more. The processing capabilities, the number of IOs and offerable functionalities of the IC is reaching greater heights with time. This essentially demands larger throughput support from the signal interfacing circuits. A large number of analog inputs appearing simultaneously are frequently witnessed in applications, such as multi-channel neural recording systems and CMOS image sensors (Gao et al., 2012, Shin et al.,

2012). Yet again, the constraints are low power dissipation and low area.

To achieve the goal, either a high bandwidth ADC is shared among multiple recording channels by employing a time-domain multiplexer (Zou et al., 2013) or multiple channel-dedicated ADCs (Gao et al., 2012) could be employed. In the first case, though the architecture is area efficient, a buffer preceding the ADC can draw a significant amount of power due to the shortened sampling time of the ADC. In the second case, resource sharing with the ADC is limited leading to area inefficiency. It will be wise to have a parallel operation of multiple sub ADCs and simultaneous sharing of resources between them.

The ADC architecture of chapter 3 could be extended for a parallel conversion of multiple analog inputs. The proposed concurrent SAR ADC architecture is shown in Figure 6.1. Each sub ADC constitutes a CA, a comparator, a code register and code dependent combinational circuit. All sub ADCs are identical and share a common CA, a sequencer and code independent combinational circuit. Algorithm could be devised to have a larger percentage of controller complexity shifted to code independent combinational circuitry. The sharing of hardware resources results in reduced power consumption and area for a given throughput. For $m$ number of sub ADCs, the architecture demands $m + 1$ CAs. Owing to multiple sub ADCs accessing the shared CA, the total parasitics and the cross-talk effects on the shared CA become more significant. Thus, to retain a good conversion accuracy, the capacitor size of the shared CA is increased to $m$ times the unit capacitance. However, overall capacitance density and matching will be good for larger capacitors. The binary search algorithm and the swapping of switch control signals will be similar to the one witnessed in chapter 3.

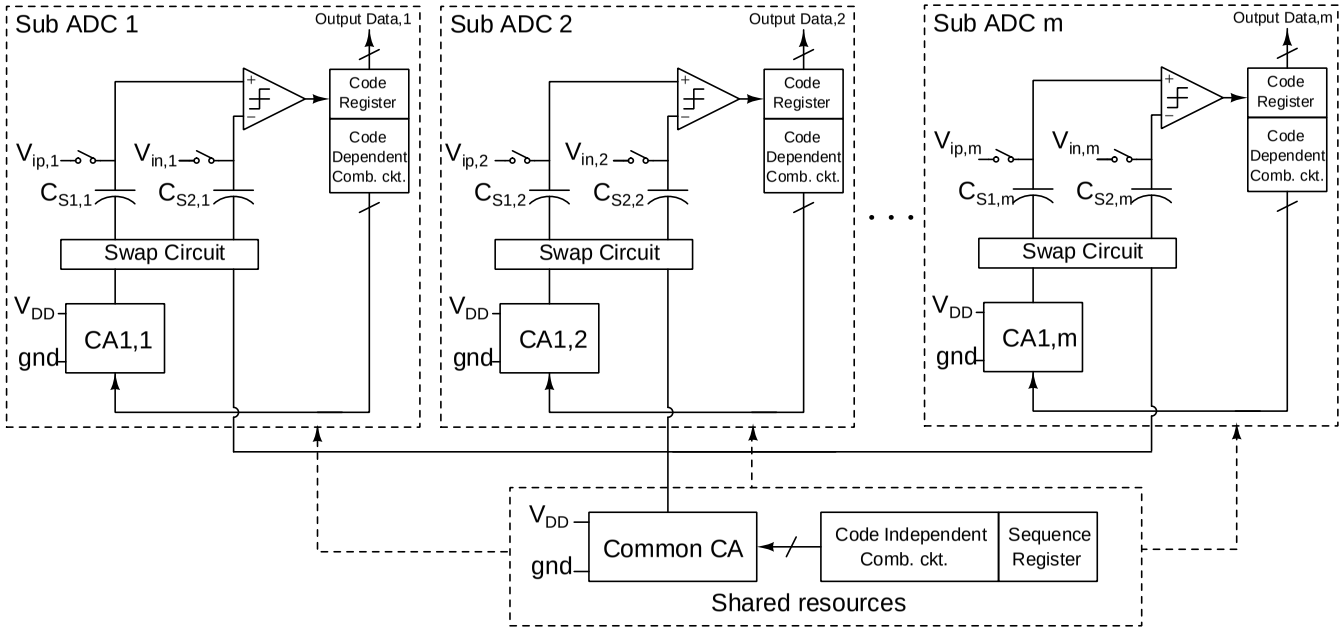



**Figure 6.1:** Concurrent SAR ADC architecture.

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# Publications based on the thesis

The thesis outlines the study and designs of ultra low power and low area SAR ADCs and is a result of the research carried at the Department of Electronics and Communication Engineering, National Institute of Technology Karnataka between July 2011 and January 2016. The research during this period has resulted in the following publications:

***A. International Conference Proceedings:***

1. Jagadish, D. N. and Bhat, M. S. (2014). "Low energy and area efficient nonbinary capacitor array based SAR ADC." *Proc., 5th Int. Sym. Electron. Syst. Des.*, IEEE, Surathkal, India, 54-57.

2. Jagadish, D. N. and Bhat, M. S. (2014). "A low voltage inverter based differential amplifier for low power switched capacitor applications." *Proc., 5th Int. Sym. Electron. Syst. Des.*, IEEE, Surathkal, India, 58-62.

3. Sridhar, R. N., Jagadish, D. N., and Bhat, M. S. (2016). "A low-energy area-efficient dual channel SAR ADC using common capacitor array technique." *Proc., Int. Conf. Distrib. Comput. VLSI Ele. Circuits Robot.*, IEEE, Surathkal, India, 148-152.

***B. Refereed International Journals***

1. Jagadish, D. N. and Bhat, M. S. (2015). "Low energy and area efficient nonbinary capacitor array based successive approximation register analog-to-digital converter." *J. Low Power Electron.*, 11(3), 436-443.

2. Jagadish, D. N., Laxminidhi T., and Bhat, M. S. (2017). "An 11.39 fJ/conversion-step 780 kS/s 8 bit Switched Capacitor based Area and Energy Efficient SAR ADC in 90 nm CMOS." *IET Circuits Devices Syst.*, (Provisionally accepted).

### *C. Patents filed*

1. Jagadish, D. N. and Bhat, M. S. (2013). "Successive approximation register analog to digital converter circuit and conversion method thereof." *Indian patent application*, 4777/CHE/2013.

2. Laxminidhi, T., Jagadish, D. N., and Bhat, M. S. (2014). "Switched capacitor integrator based successive approximation register analog to digital converter circuit and conversion method thereof." *Indian patent application*, 3549/CHE/2014.

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