POWER-SHIELD:
A POWER-QUALITY ENHANCER FOR CURRENT-SOURCE TYPE OF NONLINEAR LOADS

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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QUOTATIONS

My desires are many and my cry is pitiful, but ever didst thou save me by hard refusals; and this strong mercy has been wrought into my life through and through.

Day by day thou art making me worthy of the simple, great gifts that thou gavest to me unasked – this sky and the light, this body and the life and the mind – saving me from perils of overmuch desire.

There are times when I languidly linger and times when I awaken and hurry in search of my goal; but cruelly thou hidest thyself from before me.

Day by day thou art making me worthy of thy full acceptance by refusing me ever and anon, saving me from perils of weak, uncertain desire.

XIV: Gitanjali, *Rabindranath Tagore*

DEDICATION

To:

Abbe, Appa, and Akka

and

Shri. M. B. Naik and Shri. A. M. Prabhu

DECLARATION

I hereby ***declare*** that the Research Thesis entitled **POWER-SHIELD: A POWER-QUALITY ENHANCER FOR CURRENT-SOURCE TYPE OF NONLINEAR LOADS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirements for the award of the Degree of ***Doctor of Philosophy*** in Electronics and Communication Engineering is a ***bona fide report of the research work carried out by me***. The material contained in this thesis has not been submitted to any University or Institution for the award of any degree.

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Date: 15^{th} May 2017

CERTIFICATE

This is to *certify* that the Research Thesis entitled **POWER-SHIELD: A POWER-QUALITY ENHANCER FOR CURRENT-SOURCE TYPE OF NONLINEAR LOADS**, submitted by **Jora M. Gonda** (Register Number: 03221020A) as the record of the research work carried out by him, is *accepted* as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of ***Doctor of Philosophy***.

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ABSTRACT

KEYWORDS: Power Quality; Current-Source Nonlinear load; Active Power Filtering; Passive Filter; Series Active Filter, Parallel Active Filter, Parallel Passive Filter, Series Passive Filter, International Standards.

Electrical power is the most convenient form of energy-source in terms of generation, transmission, utilization, and efficiency. It can be converted to any form which is necessary and useful to mankind. The process of conversion has undergone tremendous changes due to the advancements in the technology and the demand by the consumer. The efficiency, size, cost, and reliability in the conversion process are important. Power Electronics has been playing an important role in this process. However due to the switching action in the power-electronics-converters lot of harmonics are generated. These harmonics are injected into the power system and they spread across it, some times even getting amplified. This can affect the operation of other devices connected to the system, because such currents manifest as harmonic voltages across the power system network. The voltage disturbances – sag, swell, and switching transients at the load-point are also of serious concern to the load. The performance and the life of the electrical equipment suffer in general, while there are some equipment which are sensitive to the disturbances from the utility side. There are reports of heavy loss of revenue due to the failure of sensitive equipment. Thus the quality of Electrical Power provided by the utility and the permissible extent of pollution of the utility grid by the consumer became important. This has led to the development of the International Standards with the active participation of all the stakeholders – the utility, the consumer, the equipment manufacturer, the measuring instrument manufacturer, and the researchers – who play the role of defining the quantities which shall be/ can be compensated. The violation of these norms is likely to invite heavy penalties.

One class of load drawing nonsinusoidal current from the source is the current-source type of nonlinear loads or current-stiff nonlinear loads. These loads are found in applications like – the Current-Source Inverter fed Induction Motor and Synchronous Motors, the DC Motor loads, the Permanent Magnet Synchronous Motors, the battery charging circuits in the constant-current charging mode, electro plating, high energy

magnet applications, the superconducting magnetic energy storage systems, and plug-in Electric vehicle battery chargers. While they draw the harmonic currents from the loads, they are also sensitive to disturbances from the source side.

Considerable amount of work is done towards mitigating the problems due to such loads and to insulate them from the disturbances from the source. A thorough study is carried out regarding the sources of distortion, effects of distortion, power theory, applicable standards, and means for compensation – topology, compensating-signal extraction techniques, modeling, control, and switching techniques. The performance of different options available are evaluated.

This led to the conceptualization of a multifunction device – Power-Shield that can shield the source and the load from each other as far as the unwanted disturbances and pollution are concerned. In this work the philosophy adopted is that of the mission in IEEE Std. 519:1992, revised in 2014, which prescribes that *the utility is responsible for maintaining a good quality voltage and frequency, and that the consumer shall draw a near sinusoidal, unity power factor, and balanced current from the source.* It is intended to make the load insensitive to the disturbances from the source side and offer itself as a balanced and linear load on the utility system. The custom power device Power-Shield is achieved by a judicious choice and combination of the topology and the control principle. The choice of the topology is validated through the extensive simulation study. *The* Power-Shield *thus arrived at consists of a low power Parallel Active Filter, a Series Active Filter, a Parallel Passive Filter (a combination of tuned (to significant harmonics) filter and a Reactive Power Compensator), and a Commutation Reactance, in that sequence from the utility end to the load end.*

Also comprising this thesis are two novel, input-locked (in phase and amplitude) and synchronized algorithms for the extraction of the compensating quantities and a modified hysteresis switching technique based on the sensing of the voltage at the far-end (in relation to the injecting converter) of the injection inductor. *The algorithms exhibit a very good transient response of around 60 ms, zero steady-state error, and excellent noise rejection capability. The novel switching principle proposed here for the sampled hysteresis control has the attraction of a lesser number of unipolar switchings per cycle*

and a better control over the error band.

A single-phase thyristor controlled rectifier feeding a separately excited DC motor as an example of a current-stiff load is assembled. Parallel Passive Filters comprising of capacitor for reactive power compensation and tuned harmonic filters for harmonic compensation are designed, implemented, and tested. A three-phase IGBT based inverter is fabricated to serve as a single-phase Parallel Active Filter and a half bridge Series Active Filter. It is tested up to 400 V, 15 A, and at a switching frequency of 32 kHz. The test results and analysis thereof are presented. *It is found that the topology arrived at demonstrated the superior quality of filtering by rendering the Parallel Passive Filter more effective. The clean switching waveforms across the IGBTs at that voltage and frequency is a testimony to the quality of fabrication of the converter circuit.*

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ABBREVIATIONS

ALL	Amplitude Locked Loop
ANC	Adaptive Noise Cancellation
ANN	Artificial Neural Network
AP	Active Filter
APF	Active Power Filter
CCITT	Consultative Committee for International Telephony and Telegraphy
CENELEC	European Committee for Electro-technical Standardization
CIGRE	International Council for Large Electric Systems, Geneva
CSI	Current Source Inverter
CSNL	Current Stiff Nonlinear Loads
DC	Direct Current – to mean a Constant/ not time varying
DFS	Discrete Fourier Series
DVR	Dynamic Voltage Restorer
DSC	Digital Signal Controller
EMI	Electro Magnetic Interference
ESR	Equivalent Series Resistance
FACTS	Flexible AC Transmission Systems
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
IEC	International Electro-technical Commission, Geneva (Commission Electro-technique Internationale)
IEEE	The Institute of Electrical and Electronics Engineers, Inc. USA
ITIC	Information Technology Industries Council
LTI	Linear Time Invariant
μC	Micro Controller

NRS	South African Standard
PAF	Parallel Active Filter
PF	Passive Filter
PCC	Point of Common Coupling
PID	Proportional-Integral-Derivative
PLL	Phase-Locked Loop
PPF	Parallel passive Filter
PPM	Parts Per Million
PQC	Power Quality Conditioner
PWM	Pulse Width Modulated
RMS	Root Mean Squared
$\boldsymbol{s} \triangleq \frac{d}{dt}$	Differentiation **operator**, Laplacian **operator**
SAF	Series Active Filter
SCC	Short Circuit Capability
SCR	Short Circuit Ratio
SCR	Silicon Controlled Rectifier
SMES	Superconducting Magnetic Energy Storage
SNDR	Signal to Noise and Distortion Ratio
SOLF	Second Order Low-pass Filter
SPF	Series Passive Filter
SSA	Small Signal Analysis
UPFC	Unified Power Flow Controller
UPQC	Unified Power Quality Conditioner
VLL	Vector-locked loop
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

NOTATION

Symbol	Description	Units
$a_O(t)$	Instantaneous amplitude of $x_O(t)$	
$A_O(t)$	Time variation of the prospective constant component in $a_O(t)$	
B_P	Amplitude of the phase-locked loop (PLL) output	
$C_h(t)$	Instantaneous amplitude of h^{th} harmonic component	
D_P	Distortion Power	
d_R	Reference input	
D_R	Constant reference input	
f_{sw}	Switching frequency	Hz
G	Integrator gain	
h	harmonic frequency index	
$i_{CC}(t)$	Current on the converter side of series injection	A
$i_{CL}(t)$	Current on the load side of series injection	A
$i_{RECT}(t)$	Rectifier input current	A
$i_S(t)$	Source current input to the Power-Shield	A
$i_{ST}(t)$	Total Source current input to the Power-Shield	A
I	RMS value of the current	A
I_h	RMS value of the h^{th} harmonic current	A
k	General **alpha-numeric** count index	
κ	Coupling coefficient for coupled coils/transformers	
m	Index for Inverter level	
n	Tuned frequency index for the filters	
P	Active Power	W
Q	Reactive Power	VAr
Q_F	Quality factor of the tuned filter	
R_S	Source resistance	Ω
S	Apparent Power	VA
T	Period of a periodic waveform	s
T_{sw}	Switching period	s
$u(t)$	Unit step function	
$v_{CC}(t)$	Compensating voltage on the converter side of series injection	V
$v_{CL}(t)$	Compensating voltage on the load side of series injection	V
$v_{PCC}(t)$	Voltage at PCC with reference to the source	V
$v_{PL}(t)$	Voltage on the left side of series injection	V
$v_{PR}(t)$	Voltage on the right side of series injection	V
$v_{RECT}(t)$	Rectifier input voltage	V

$v_S(t)$	Source voltage at the input to the Power-Shield	V
V_h	RMS value of the h^{th} harmonic voltage	V
$v_O(t)$	Rectifier output voltage	V
$x_I(t)$	Instantaneous value of input signal	
$x_O(t)$	Instantaneous value of output signal	
$x_E(t)$	Instantaneous value of error signal	
$X_E(t)$	Constant component in $x_E(t)$	
α	Firing angle of the rectifier	degrees
ϕ_h	Phase angle between two h^{th} harmonic quantities	rad
ω_m	The frequency of the modulating signal	rad/s
ω_n	Tuned frequency of the filter (signal/power)	rad/s
ω_c	Cut-off frequency of the SOLF (signal)	rad/s
ω_1	Frequency of the fundamental component	rad/s
ω_s	Frequency of the source	rad/s
$\overline{X}$	As a phasor, it represents a sinusoidal quantity X. It has a magnitude X and an angle $\angle X$. Thus $\overline{X} = X\angle X$, X may be voltage V or current I.	
$\overline{Z}$	As a complex number, it represents a magnitude Z and an angle $\angle Z$. Thus $\overline{Z} = Z\angle Z$, Z may be impedance $Z = R \pm jX$ – with Resistance R and reactance X or apparent power $S = P \pm jQ$ – with active power P, reactive power Q.	

Chapter 1

A Telescopic view of the Thesis

1.1 Introduction

The Electric Power has attained the status of a major driving force of civilization along with the Internet Technology, and while the latter is powered by the former there has been a growing trend in using the Internet and Internet-of-Things to control and manage the Power-Industry in the recent days. The application of Power-Electronics in the power chain – conversion, transmission and distribution, utilization – industrial, commercial, and residential has been continuously growing, attracted by the better efficiency, cost, size, reliability, and performance – steady-state and dynamic. But the application of power electronics has its deleterious effects of the switching-action, the very nature of the technology and of such load-frequency characteristics manifested by the conversion function the converters are expected to perform. The switching action in the converters generates lots of harmonics – voltage and current at the Point of Common Coupling (PCC). These harmonics are injected into the power system, which spread across it, sometimes even getting amplified. There are many nonlinear loads which draw nonsinusoidal currents from the utility source and there are some loads which are sensitive to the disturbances from the utility side. This can affect the operation of some of the other devices connected to the system.

One class of such loads is the current-source type of nonlinear loads or current-stiff nonlinear loads (CSNL). These loads are found in applications like the Current-Source Inverter driven Induction motor, Synchronous motor, and the Permanent magnet Synchronous motor, the rectifier fed DC Motor, the ubiquitous battery charging circuits in the constant-current charging mode, the electro-chemical processes, the Plug-in Electric Vehicles, the high energy magnet power applications, and the Superconducting

Magnetic Energy Storage (SMES) systems.

There is a need to limit the harmonic level – in voltage and currents and the reactive power drawn from the utility source at the PCC by such loads and also to maintain a good voltage to the load under consideration. The advancements in the integrated circuit technology leading to better power-electronic-switching-devices and control circuits (analog and digital) has made it possible to achieve this.

1.2 Motivation, Objectives, and Scope

1.2.1 Motivation

This work is motivated by the fact that there are stringent regulatory norms being considered for implementation by the utility as well as the consumers. International standards are developed with the active participation of all the stakeholders – the utility, the consumer, the equipment manufacturer, measuring instrument manufacturers, and the academia and researchers – who play the role of defining the quantities which shall be/ can be compensated. The violation of these norms may invite heavy penalties. This is all being done to improve, the efficiency of power conversion, throughput of the equipment, and its reliability and also to reduce the cost of manufacturing.

1.2.2 Objectives

This research work is towards achieving the following objectives:

- Conceptualization of a multifunction device – Power-Shield that can shield the source and the load from each other as far as the unwanted disturbances and pollutions are concerned.
- To arrive at a system with a combination of topology and control principle that is better suited for the current-stiff nonlinear loads (the load under consideration).
- Design the different components of the Power-Shield.
- Obtain and design new algorithms for extraction of the compensating quantities.
- Obtain new switching techniques for current control of the Parallel Active Filter (PAF).

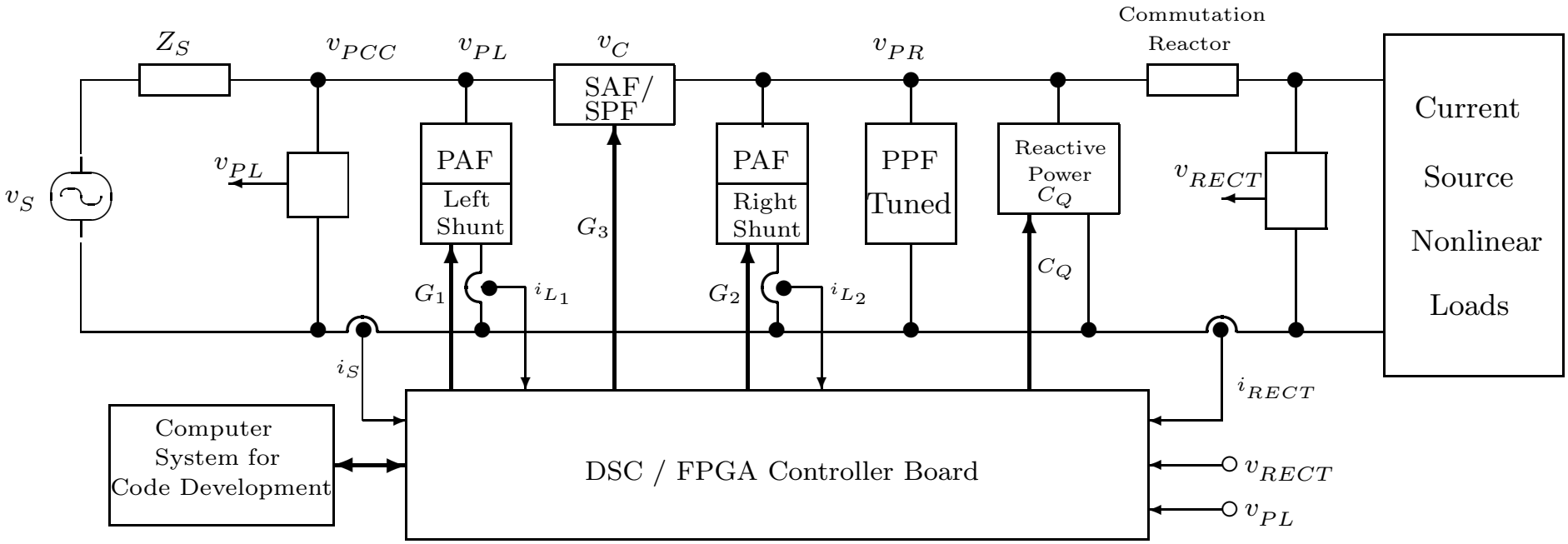
- Apply a systematic procedure for obtaining dynamic and steady-state model, so that a reliable analysis can be carried-out.

1.2.3 Scope

This work is concerned with the selection of a suitable topology and control principle for a Power Quality Conditioner (PQC) for the Current-Stiff Nonlinear Loads (CSNL). Considering that the state-space based modeling and simulation methodology is to be adopted and the practical implementation aspects concerned, a single-phase fully controlled rectifier with R-L-E (Resistive (R), Inductive (L) and Voltage source (E), where the voltage source is the back emf of a separately excited the DC motor feeding an alternator on a lamp load) load is chosen. The work involves – the basis for arriving at the selected topology and the control principle for the load concerned, the design of the converters and passive components, and modeling and simulation for assessing the performance of the overall system. The Voltage Source Converters (VSC) are used as compensators. Two algorithms for the extraction of the compensating quantities (voltage or current) and an improved technique for hysteresis control are also proposed and incorporated in the simulation model. The hardware (power circuit and signal conditioning) necessary for implementation of the complete system on a Digital Signal Controller (DSC) or a Field Programmable Gate Array (FPGA) platform is developed. The proposed system can be adopted for retrofitting or even for new solutions. The experimental results from the Passive Filter implementation and those exhibiting the inverter capability are presented.

1.2.4 The Topology under consideration

The Power Quality enhancement for Current-Source Type of nonlinear load is considered. The objective is to meet the requirements from the utility side without compromising the requirements from the load side. The structure of the compensator is given in Figure 1.1. The bank of Parallel Passive Tuned Filters for harmonics and the Capacitor for Reactive Power Compensation are placed in between the load and the Active Filter System – consisting of a Series Filter with Parallel Active Filters (PAF) on either side of the Series Filter. This arrangement will facilitate experimentation in order to determine the most suitable topology which can meet all the Power Quality requirements under the situations of varying load and supply disturbances.



G_1, G_2, and G_3 are the Gating Signals for the Left-Shunt, the Right-Shunt, and the Series Active Filters respectively

Figure 1.1: The schematic of the Topology considered for exploration

1.3 Methods and the approach adopted

The issues related to the Current-Source nonlinear loads is probed leading to exploring some options to solve the problems therein. It involves the survey of the developments in the research area, the evaluation and comparison of the solutions already proposed, and suggesting alternative solutions. It involves mathematical modeling, analysis, design, simulation, building hardware prototypes, conducting experiments on the mathematical model and hardware prototype, and drawing conclusions with suggestions for future work in the area. The MATLAB® and Simulink® [MathWorks®(2006)] is extensively used in the simulation and MATLAB® is used in data analysis and report generation on the results from the simulation as well as the experimentation. The approach adopted is listed below:

- Survey: Topological
  - Current-Source type of nonlinear loads
  - Survey of the solutions to compensate for and shield the Current-Source type of nonlinear loads
  - Bringing out the requirements of the Topology for Filtering and Shielding
- Survey: Algorithms, Control, and Switching Techniques
  - Algorithms for extraction of compensating quantities
  - Control techniques
  - Converter Switching Techniques
- Contributions:
  - Two Algorithms for the extraction of the compensating quantities
  - Novel switching principle for the sampled hysteresis control
  - Topology for Power Quality Enhancement
  - Hardware implementation with Passive Filters
  - Development of the hardware necessary for the closed-loop control of the complete system

- Deciding on a minimal, general circuit structure which facilitates to conduct experiments to arrive at a suitable Topology – Power-Shield for Filtering and Shielding
- Deciding the Model Structure of the Utility and determining the parameters thereof
- Modeling of the complete circuit in state-space form
- Detailing of the computational components required:
  - Firing pulse generator for the Controlled rectifier
  - Controller for load-current regulation
  - Phase-locked loop (PLL) for the firing pulse generator and as a reference for the extraction of compensating signal
  - Controller for Active Power Filters (APF)
- Simulation:
  - Determining the Typical cases for simulation experiment
  - Deciding the Simulation Strategy: Simulation technique, collection of data
  - Conducting experiments with the selected cases
  - Discrete Fourier Series (DFS) analysis of the waveforms using Curve-fitting and equidistant sampling
- Real-time validation of the Novel extraction algorithms on dSPACE [dSPACE(1999)] platform
- Development of the hardware necessary for implementation:
  - Power Circuit: Fully Controlled Single-Phase Rectifier feeding a DC Motor driving an alternator with lamp load, Voltage Source Converter
  - Signal Processing: Voltage and Current Transducer circuits, Analog level shifters with anti-aliasing filters, digital level shifters
  - Test-zig for testing IGBT or MOSFET switches
- Hardware experiments
  - Determining the Typical cases for conducting experiments and testing.

1.4 Contribution

A scheme for mitigating the Power Quality disturbances to the Current-Stiff nonlinear loads and isolating the power system from the disturbances of the load is obtained. Through simulation study it is demonstrated that it meets all the requirements as a Power Quality Conditioner. The following contributions are made from the thesis:

- A single-phase system is modeled in state-space form and simulated in MATLAB®/ Simulink®. It is configured to be flexible to enable conducting various experiments. The multi-function power quality compensator – Power-Shield is determined through experimentation on the general topology considered. Its modeling, analysis, and design is carried out. The system is simulated and its performance is evaluated.

- Two algorithms for extraction of harmonics are proposed. Their performance is evaluated and they are incorporated in the Power-Shield. Their real-time performance is evaluated in dSPACE platform.

- A novel multi criteria based switching principle is proposed and tested. Its performance is compared with the existing techniques. It holds promise, as its overall performance is better than the existing algorithms.

- A single-phase prototype is implemented in hardware with the passive filter system. The experimental results are presented with analysis.

- The components required for implementation of the closed loop control – inverters, signal sensing, signal conditioning, and analog and digital interface circuits are developed and test results are presented.

- The work has resulted in two journal papers [Gonda and David(2012)] and [Gonda and David(2013)] and three conference papers [Gonda *et al.*(2009)], [Gonda *et al.*(2010)], and [Bhat *et al.*(2010)].

Mind map

The work falls into the area of a Power Quality Conditioner with a shunt compensator and a series compensator for reactive power and harmonic current compensation and mitigation of voltage disturbances. The related areas are – power theory, standards

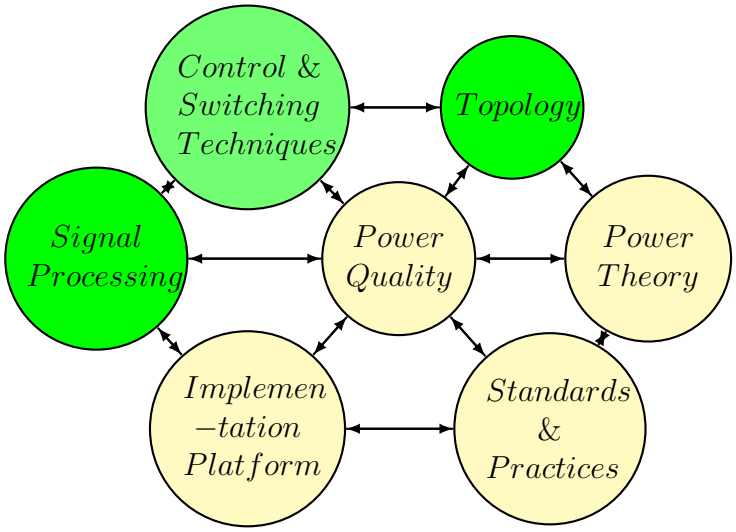


Figure 1.2: Mind map of the topic considered

for utility and the equipment, passive and active power filters, current and voltage type harmonics, different topologies, the direct or indirect compensation techniques, different types of controllers – like the classical PID (Proportional-Integral-Derivative) controllers, the soft computing – the Fuzzy and or the Artificial Neural Network (ANN) based. The work considered is better represented on the mind map as shown in Figure 1.2, where green indicates the areas of contribution and the depth of the colour the level of contribution.

1.5 Organization of the Thesis

In Chapter-2, a detailed literature survey is presented. The purpose of this chapter is to locate the problem under consideration in the realm of Power Quality Enhancement. The background material in the area of Power Theory and the Standards available for utility and consumer equipment are reviewed. The methods of extraction of the compensating quantity are studied and a classification is presented on the basis of – applicability to the number of phases (single-phase and/or three-phase systems) and the frequency domain or the time domain. Their characteristics are presented. The circuit topologies reported for mitigating the problems are compared and their limitations are brought out.

In Chapter-3 the compensating signal extraction techniques proposed are presented. The simulation results obtained from the algorithms proposed and their digital imple-

mentation in real-time on the dSPACE platform are presented. Their performances are analyzed and compared.

In Chapter-4 the comparative study of the hysteresis based switching techniques is presented. A new switching principle is proposed which considers the polarity of the *supply voltage* at the PCC in addition to the sign of the error in the hysteresis band. It also involves a three-level switching and incorporates the hysteresis control with a periodic sampling. It is shown to result in reduction in distortion as well as in the number of switchings per fundamental cycle.

In Chapter-5 the state-space modeling of the complete power circuit is presented. A procedure for estimation of the distribution system parameters is presented. The simulation of the complete system involving the topology under consideration, the extraction technique, the PLL, and the chosen principle of control and the method of switching is carried out. Simulation results are presented. The results obtained from the tests to explore the multi-function capability of the system is presented, leading to the determination of the Power-Shield.

In Chapter-6 all the components of the hardware developed – the inverter module, the passive filter system, the loading arrangement, the test-zig, the signal conditioning cards, the gate drive cards, the sensing cards, the power supply for the boards, digital I/O cards for signal matching are presented and explained. The design details of the hardware are given. The results of the experiments with passive filters is presented along with the analysis and conclusions.

The conclusions and the scope for future work are given in Chapter-7.

Chapter 2

Power-Quality compensator for Current-Source type of nonlinear loads: An Overview

2.1 Introduction

The quality of electrical power supplied by the utilities has been deteriorating in the recent days and has issued alarms to demand for quality power. The demand for quality power is driven by two factors: while the power system is getting polluted by the increasing number of power electronics based drives and devices, the increased sophistication of the industrial drives is demanding a clean power. This is triggered by the factors like – loss of revenue due to malfunctioning of the equipment as well as increased requirements of maintenance and replacement of the equipment. This has led to the development of various standards across the globe. In this Chapter the general issues related to the Electric Power Quality are discussed. The topics related to the Current-Source type of nonlinear loads is reviewed and a survey of the various technological developments towards the compensation for such loads is presented. The Chapter ends with a conclusion on the findings leading to the problem definition and the scope of the thesis.

2.2 Power Quality, Power Theory, and International Standards

Power Quality is a term used to broadly encompass the entire scope of interaction among electrical suppliers, the environment, the systems and products energized, and the users of those systems and products. It is more than the delivery of *clean* electric power that complies with industry standards. It involves the maintainability of that power, the design, selection, and the installation of every piece of hardware and software in the electrical energy system. Starting from the generation plant to the utility customer, the power quality is a measure of how the elements affect the system as a whole. There are many factors which affect the quality of power, the following list is comprehensive though may not be complete:

2.2.1 Electric Power Quality Problems

Frequency variation:

The electrical equipment are designed normally to work at rated supply frequency (50 Hz). The allowable variation around the rated frequency and the nature of permissible variations for a given equipment are specified [Baggini(2008)].

Voltage variation:

Just like the frequency, the nominal voltage at which the utility promises to supply power is also fixed. The variation in voltage may be classified into: long term small deviation, Continuity of Supply, Voltage Sag and Swells, Transient over voltages, Voltage Unbalance, Voltage fluctuation and flicker [Baggini(2008), Bollen(2000)].

Current and/or voltage Unbalance:

Unbalance in the supplied voltage or the current that is drawn from the supply are not desired for the load and for the supply respectively [Baggini(2008), Bollen(2000)].

Current and/or voltage Harmonics:

Harmonics in either the source voltage or the load current have detrimental effects on the loads as well as the power system – leading to a total pollution of the grid [Acha and Madrigal(2001), Arrillaga and Watson(2003)].

Resonance:

There can be amplification of either the voltage or the current, the fundamental or the harmonics under certain conditions. If this is not damped, it can lead to the destruction of the equipment on the grid – the loads and the components of the power system [Acha and Madrigal(2001), Arrillaga and Watson(2003)].

Earthing:

Proper earthing of electrical equipment is important for the safety of the equipment as well as that of the personnel operating it. Improper earthing can lead to tripping of the load, causing loss of production [Baggini(2008)].

Electro-Magnetic Compatibility issues

The presence of a load can affect the operation of other loads in the system. Thus it is necessary to make sure that the load is insensitive to possible disturbances on the line and also design an equipment so that it does not cause problems to the rest of the loads on the network. The word compatibility refers to compliance with respect to both – susceptibility and interference [Baggini(2008)].

2.2.2 How to resolve Electric Power Quality issues?

The deviation from a quality power may lead to losses and accidents. It involves money and safety issues, hence connected with legal and insurance claims. The resolution of the claims requires the quantification of the disturbance, time-stamping, and the source(s) thereof. While the first two can be determined with the necessary accuracy – thanks to the development in the areas of sensors, signal processing, and communication, determining the source of disturbance is a very complex issue [Srinivasan(1996), Sasdelli *et al.*(1998)],[Ortiz *et al.*(2005), Li *et al.*(2004)]. It is also equally difficult to define parameters, to quantify the violation, which are judicious and fair to all the stakeholders concerned, under the situations when harmonics and unbalance exists in the system. Another important area is *Power Theory*, a brief account of which is given in Section 2.2.3. All these factors have led to the setting up of standards across the globe, with the active participation of all the stakeholders concerned – the consumer, the utility, the equipment manufacturer, the academia and/or

the research community, and the monitoring equipment manufacturers. They are, the IEEE (Institution of Electrical and Electronics Engineers), the IEC (International Electrotechnical Commission), the CIGRE (International Council for Large Electric Systems), the ITIC (Information Technology Industry Council), the EN (European Norm) etc., including the National Standards worldwide [Heydt(2000)].

2.2.3 Power Theory

Understanding the phenomenon of electric power transfer under the situations of unbalance and harmonics is a complex issue. It has many dimensions. Identification and quantification of various quality parameters of Electric Power Quality is being attempted through the study of power theory. It is hoped that it will help us in the following in a general context, with those specific to the thesis given in *italics*:

- *to fix responsibility of the pollution.*
- *to explain the compensation process and hence in choosing the type of the filter – Active and/or Passive; to decide the type and share of absorption by passive and active filter; designing (structure) the filters and its rating.*
- *to identify what are the disturbances and define them for quantification.*
- *as a framework for estimation of the utilization of the components of power delivery system and the load equipment.*
- for the purpose of Tariffication, measurements, and to develop standards.
- to equipment manufacturers.
- in understanding the energy flow phenomenon – with academic interest.

Power definitions:

In general the active (mean) electrical power is

$$P = \frac{1}{T} \int_0^T v \cdot i \cdot dt. \tag{2.1}$$

In an ideal power system, the voltages and currents are (purely) sinusoidal with a frequency of 50 Hz or 60 Hz. However, nonideal characteristics of real-life power system

components and nonideal loads will cause distortion. Currents and voltages will be nonsinusoidal and will contain harmonics. In most cases, the currents and the voltages will still be (approximately) periodic with a fundamental frequency of 50 Hz or 60 Hz. If the voltage and current both are periodic functions of time with the same period T, the voltage and current can both be expressed as a Fourier series and the power can be defined as,

$$P = \Sigma V_h I_h \cos\phi_h \tag{2.2}$$

where h is the order for which both current and voltage harmonics exist and ϕ_h is the phase angle between V_h and I_h. Further for a special case when both the voltages and currents are sinusoidal, the active power P can be expressed by the familiar equation, $P = VI\cos\phi$. **Apparent and reactive powers, on the other hand, are not based on a single, well defined, physical phenomenon as the active power is**. They are conventionally defined quantities that are useful under sinusoidal or near sinusoidal situations. For sinusoidal voltages and currents reactive power is defined as $Q = VI\sin\phi$. The apparent power is defined as $S = VI = \sqrt{P^2 + Q^2}$, where V and I are the RMS values of voltages and currents. Under nonsinusoidal situations there is more or less an agreement on the usage of $S = VI$. There are quite a few theories proposed, under nonsinusoidal situations as an extension on the fundamental reactive power theory, and are explained below to give a feel for the complex nature of the problem.

Reactive Power Definition Proposed by Budeanu [IEEE Std 1459-2000(2000)]

The active power in a nonsinusoidal, but periodic environment is defined as

$$P = \Sigma P_h = \Sigma V_h I_h \cos\phi_h. \tag{2.3}$$

Therefore, the reactive power can be defined by,

$$Q = \Sigma Q_h = \Sigma V_h I_h \sin\phi_h \tag{2.4}$$

which is proposed by Budeanu and is based on the frequency domain approach. However, this equation does not comply with the power triangle equation $S^2 = P^2 + Q^2$,

since the apparent power S is defined by the RMS values of the voltage and current,

$$S^2 = V^2 I^2 = (\Sigma V_h)^2 (\Sigma I_h)^2 \geq (\Sigma V_h I_h \cos\phi_h)^2 + (\Sigma V_h I_h \sin\phi_h)^2 . \tag{2.5}$$

Therefore a quantity named distortion power, D_P, was added by Budeanu as defined below,

$$D_P^2 = S^2 - P^2 - Q^2. \tag{2.6}$$

The distortion power mainly consists of the cross-product of the voltage- and the current-harmonics of different orders and will be reduced to zero if the harmonics are reduced to zero, i.e. under sinusoidal conditions.

Definition Proposed by S. Fryze [Page(1980)]

The reactive power definition proposed by S. Fryze is based on the time domain analysis. The current is divided into two parts. The first part, i_a, is a current of the same wave-shape and in *phase-shift* (time-shift to be more correct) as the voltage is, and has an *amplitude* such that $I_a \cdot V$ is equal to the active power P, where I_a and V are RMS values of i_a and supply voltage v respectively. The second part of the current is just a residual term named i_r. The two currents will then be determined by the equations,

$$i_a = \frac{P}{V^2} \cdot v; \qquad \text{and} \qquad i_r = i - i_a. \tag{2.7}$$

The reason for this division is that the current i_a is the current of a purely resistive load that, for the same voltage, would develop the same power as the load measured on. Thus, if i_r can be compensated, the source will see a purely resistive load and the *power factor* will be equal to unity. It can easily be shown that i_a and i_r are orthogonal and then the RMS values can be determined by

$$I^2 = I_a^2 + I_r^2. \tag{2.8}$$

In fact, (2.7) gives the only possible amplitude of i_a if it should be orthogonal to the residual term i_r and have the same wave-shape as v. The apparent power can then be obtained as the product of the RMS current and the RMS voltage

$$S^2 = V^2 I^2 = V^2 (I_a^2 + I_r^2). \tag{2.9}$$

The advantage of this definition is that it does not introduce any additional power component (like D_P) under nonsinusoidal conditions. However the design of compensators to eliminate harmonics is simple in frequency domain using tuned filters.

Definition proposed by Kusters and Moore [Kusters and Moore(1980)]

This definition of reactive power, is again based on the time domain approach. It expands the definition according to Fryze by a further separation of the residual current into two orthogonal components. This separation is made dependent on whether the load is predominantly capacitive or inductive. The three currents are then named as active current, inductive or capacitive reactive current and the residual reactive current, which results in an apparent power sum:

$$S^2 = P^2 + Q^2 = P^2 + Q_c^2 + Q_{cr}^2 \qquad \text{or} \qquad = P^2 + Q_l^2 + Q_{lr}^2 \tag{2.10}$$

where Q_c is the capacitive reactive power, Q_l is the inductive reactive power and $Q_{c/lr}$ corresponds to the residual reactive power. In comparison with the Fryze's decomposition, the definition by Kusters and Moore has the advantage that it identifies the part of the current that can be compensated with a shunt capacitor (for Q_c) or a shunt inductor (for Q_l). The residual reactive power $Q_{c/lr}$ can be compensated only by means of active filters.

The power theories [Marshal *et al.*(1992), Czarnecki(1987)] are broadly classified into either belonging to frequency-domain based or to time-domain based, as proposed by Budeanu and Fryze respectively. They may be applied to – single-phase or three-phase, sinusoidal or nonsinusoidal, balanced or unbalanced, periodic or non-periodic [Czarnecki and Lasicz(1988)] etc. There are also other theories proposed – like the Poynting Vector based and Currents Physical Components by Czarnecki [Czarnecki(2010), de León and Cohen(2006)], FBD-Method [Depenbrock(1993)], Tenti's Power theory, Akagi's Instantaneous power theory [Akagi *et al.*(2007)] etc.

Thus the above discussion makes it clear that a knowledge of Power Theory is very much necessary in deciding the compensation for reactive power and harmonics in power systems – the area of work considered in this thesis. It must be noted that, power factor and reactive power have been used to

determine the tariff and hence the type and size of the compensators to minimize the cost of power. There can also be unbalance in the supply-voltage or in the currents drawn from the supply. This factor also has to be considered in the definition of those quantities. Hence, a definition, that is technically justifiable, fair, transparent, easily understandable, and agreeable to/by all stakeholders concerned must evolve. This has been and is being highly debated and the IEEE has come up with its standards, the IEEE Std 1459-2000 on Power Definitions [IEEE Std 1459-2000(2000)] which has defined several parameters to quantify the deviations from normal sinusoidal and balanced situations.

2.2.4 Effects of Harmonics

The harmonics are sinusoidal voltages or currents of frequencies that are integer multiples of the frequency at which the supply system is designed to operate (termed the fundamental frequency; usually 50 Hz or 60 Hz). They combine with the fundamental voltage or current, and produce waveform distortion. The harmonic distortion exists due to the nonlinear characteristics of the devices and the loads on the power system. With rapid development of power electronics technology, various electronic equipments are used widely in industrial applications and transmission or distribution systems such as AC/DC static power inverters, adjustable motor drives and switching power supplies. These electronic equipment impose nonlinear loads to the supply mains and they can usually be modeled as current sources that inject harmonic currents into the power system. Voltage distortion results as these currents cause harmonic voltage drops across the system impedance.The magnitude of the voltage distortion depends on the source impedance and the harmonic voltages produced. If the source impedance is low then the voltage distortion will be low. If a significant portion of the load becomes nonlinear (harmonic currents increase) and/or when a resonant condition prevails (system impedance increases), the voltage distortion can increase dramatically. The harmonic contamination, increased reactive power demand, and Power system voltage fluctuations are some of the adverse affects of these nonlinear loads. Harmonic contamination has become a major concern for power system specialists due to its effects on sensitive load on the power distribution system. Effects of harmonics can be broadly classified as:

- Heating effects caused in the equipment
- Disruption of the normal operation of the equipment

Heating effect

The heating effect is due to multiple physical phenomenon. The harmonic currents will increase the RMS value of the current resulting in additional I^2R losses. Harmonic currents will also invite skin effect and contribute for the additional loss due to increase in effective resistance. The harmonic current flowing in magnetic and dielectric components increase the core and dielectric losses. It also adds to the friction losses in motor loads because of the harmonic torques. The way these effects occur in different loads is explained in the following:

1. *Lamps:*

   A significant portion of the system load has impedance characteristics consisting of passive resistance or RL networks. These include, for example, incandescent lighting and resistance type heating. With constant fundamental voltage, the per unit increase in power due to voltage distortion for this class of loads is limited to the distortion factor squared. Incandescent lamp is one of the devices of this load group, which is most sensitive to increased heating effects.

2. *Motors and Generators:*

   The effect of harmonics on the motors and generators is to cause extra losses, which in turn overheat the machine. In case of low power rating machines these harmonics also produce torque pulsations which further increase heating, due to the increased friction. The overall effect of these harmonics is to reduce the life of the machine.

3. *Transformers:*

   The effect of harmonics on transformer is two fold: firstly the current harmonics cause an increase in copper loss and core loss, secondly there will be insulation stresses and possible resonance (at the harmonic frequency) between transformer winding and line capacitance. The overall effect of losses is a need for a transformer with a higher rating.

Disruption

Disruption is defined as the abnormal operation or failure of equipment due to voltage or current harmonics, other than thermal or insulation effects.

1. *Switch-gear:*

   Harmonic component in the current waveform can affect the current interruption capability of the switchgear. The problem is that the harmonic components can result in high $\frac{di}{dt}$ magnitude at the zeros, making interruption more difficult. The circuit breaker failure has been attributed to the inability of the blowout coils to operate adequately in the presence of several harmonics. As the blowout coil assists in the arcs movement into the arc-chamber where the interruption takes place, its inefficient operation prolongs arcing and eventually results in break failure.

2. *Fuses:*

   A significant level of harmonic current in a fuse causes excess heating, which can cause drift in the time-current characteristics of the device. This is particularly noticeable during low magnitude faults.

3. *Metering devices:*

   Harmonic current affects metering and instrumentation particularly if resonance condition occur which cause high harmonic voltage on the circuit. Induction disc devices such as Watt-hour meter and Over-current relays are designed to monitor only fundamental current, but harmonic currents from the nonlinear loads and/or phase unbalances caused by harmonic distortion can cause erroneous operation of these devices.

4. *Power converters and Electronic loads:*

   A large class of equipment utilize energy in some form other than at the incoming line frequency, and requires rectification or frequency conversion. External distortion can affect the operation and performance of either the power converter or the converter load. The severity of these effects is complicated by the fact that the converter generally is a source of distortion as well. The disruption of these types of loads may be divided into two categories – disruption of the con-

verter operation and disruption of the converter load operation. The converter disruption can result from the shifting of firing angles resulting from harmonics, and from SCR or transistor failure due to high $\frac{di}{dt}$ and $\frac{dv}{dt}$ or over heating effects. Disruption of load could result from transmittal of incoming harmonic through the converter load side filter.

5. *Protective relays:*

   System harmonics affect relays in various ways leading to possible mal-operation of the relay. The relays that depend upon crest voltages and/or current or voltage zeros for their operations are obviously affected by harmonic distortion on the wave.

6. *Effect on communication system:*

   Inductive coupling and interference with telephone lines causes a lowering of quality of the transmitted message.

7. *Interface with program circuits and carriers:*

   In load management control, it is customary to use a carrier in the power line to control the various elements of the load management units along the feeder. It is found that the carrier modulator-demodulator stage experienced a very high level of interference at specifically one frequency used by one of the channels.

The above presentation has indicated the problems of harmonics in power system. But these are not directly linked to Tariffication and Compensation techniques, however they cannot be tolerated because of the ill-effects it has on the performance and operation of the components of the power delivery and the conversion system. Hence the injection of harmonics has to be discouraged, and there has to be guidelines for the same. This has led to the development of another standard, the IEEE Std 519-1992 on Power System Harmonics [IEEE Std 519-1992(1992)] and the [IEEE Std 519-2014(2014)] with the revision. It has suggested guidelines for meeting the power quality parameters at the PCC. The IEC 61000 Series [IEC 61000 Series(1990)] is an alternative to the issues concerned with harmonics. The EN 50160 is a European Standard for dealing with the supply requirements for the European utilities [EN 50160(1994)]. This is approved by the European

Committee for Electrotechnical Standardisation (CENELEC) in 1994 and is mandatory across Europe. South Africa has implemented *Quality of Supply Standard* NRS 048 since July 1, 1997 [NRS 048(1997)].

2.2.5 Measures of Power Quality

The following are some of the power quality parameters concerned with the presence of current and or voltage harmonics and unbalance in power system:

1. *Distortion Factor (DF):* The degree of source current distortion may be quantified by a term *Distortion Factor (DF)*. It is defined as the ratio of the RMS value of the fundamental current to the RMS value of the total current as follows:

$$DF = \frac{I_{s1}}{\sqrt{I_{s1}^2 + \sum_{h=2}^{\infty} I_{sh}^2}} \tag{2.11}$$

   where I_{sh} is the h^{th} harmonic source current; $h = 1$ for fundamental.

2. *Displacement Power Factor (DPF):* The displacement power factor is defined as the ratio of the *average power* to the *product of fundamental RMS voltage and the fundamental RMS current* as follows:

$$DPF = \frac{P_1}{V_s \cdot I_{s1}} = \frac{V_s \cdot I_{s1} \cdot cos\phi}{V_s \cdot I_{s1}} = cos\phi. \tag{2.12}$$

3. *Power Factor (PF):* The line power factor is defined as the ratio of *average power* to the *product of supply RMS voltage and supply RMS current.* It is expressed as:

$$\begin{aligned} PF &= \frac{P_1}{V_s\sqrt{I_{s1}^2 + \sum_{h=2}^{\infty} I_{sh}^2}} && (2.13)\\ &= \frac{V_s \cdot I_{s1} \cdot cos\phi}{V_s\sqrt{I_{s1}^2 + \sum_{h=2}^{\infty} I_{sh}^2}} && (2.14)\\ &= cos\phi \cdot \frac{I_{s1}}{\sqrt{I_{s1}^2 + \sum_{h=2}^{\infty} I_{sh}^2}} && (2.15) \end{aligned}$$

   where use is made of (2.11) and (2.12) in (2.13). Hence,

$$PF = DPF \cdot DF. \tag{2.16}$$

   The tacit assumption of an ideal supply voltage conditions must be noted in the

above definitions. It has a significance in revenue metering and power factor correction.

4. *Total Harmonic Distortion (THD_V)* for the voltage is defined as,

$$THD_V = \sqrt{\sum_{h=2}^{\infty} \left(\frac{V_h}{V_1}\right)^2} \tag{2.17}$$

where, V_h = RMS value of the h^{th} harmonic voltage.

5. *Total Harmonic Distortion (THD_I)* for the input current is defined as,

$$THD_I = \sqrt{\frac{I_s^2 - I_{s1}^2}{I_{s1}^2}} = \sqrt{\frac{I_s^2}{I_{s1}^2} - 1}. \tag{2.18}$$

It has general purpose applications. Note the similarity between (2.18) and (2.17). They are two different forms of definition of THD. While THD_V is directly defined in the standards, THD_I is sometimes indirectly calculated using the formula, given the individual harmonic content in the current. As per the standard it is TDD that is important for the current and is expressed as in (2.19) as a function of THD_I.

6. *Total Demand Distortion (TDD):* Total Demand Distortion is a measure of the THD_I taking into account the supply circuit rating. As the circuit rating varies the TDD varies for a given load, giving lower TDD for a circuit with a higher rating. It is expressed as,

$$TDD = \frac{\text{Fundamental load current}}{\text{Circuit rating}} \cdot THD_I. \tag{2.19}$$

7. *Current Crest Factor (CF_I):* This is a measure of the peak input current $I_{s(peak)}$ as compared with its RMS value I_s. It is defined as:

$$CF_I = \frac{I_{speak}}{I_s}. \tag{2.20}$$

CF is taken into consideration to specify the peak current ratings of devices and components, especially the semiconductor devices.

8. *Voltage Crest factor (CF_V):*

$$CF_V = \frac{V_{peak}}{V_{RMS}}. \tag{2.21}$$

This is a measure of the Dielectric stress requirement.

9. *K factor*: Harmonic currents cause additional losses in the converter transformers and hence they have to have a higher rating. This is related to the K factor (as defined in the USA) defined as follows,

$$K = \sum_{h=1}^{H_{max}} \left(\frac{hI_h}{I}\right)^2. \tag{2.22}$$

This is used by the designers to specify a transformer with a higher rating.

10. *Telephone Influence Factor (TIF)* [Arrillaga and Watson(2003)]: This quantity is a measure of the emission of electrical signal and is the related to Audio circuit interference. It is defined as,

$$TIF = \sqrt{\sum_{h=1}^{H} \left(\frac{w_h X_h}{X_{RMS}}\right)^2} \tag{2.23}$$

where, H is the maximum harmonic order to be considered, X_h is the single frequency RMS voltage or current, X_{RMS} is the RMS value of the total waveform (line to neutral) and w_h is the harmonic weighting factor. w_h is related either to the,

C-Message weighting factor (C_h) (by Bell Telephone Systems and Edison Electric Institute, used in USA and Canada), which is defined as,

$$w_h = C_h \cdot 5 \cdot h \cdot f_1 \tag{2.24}$$

or to the

Psophometric weighting factor (p_h) (by the CCITT Geneva, used extensively

in Europe), and is defined as,

$$w_h = p_h \cdot h \cdot f_1/800 \tag{2.25}$$

where f_1 is the fundamental frequency (50 Hz). In practice there is not much difference between C_h and p_h over the complete range of frequency of interest.

11. *$I \cdot T$ and $kV \cdot T$ products:* These are defined to take into account the rated Voltage or the Current of the environment in which the telecommunication line is running. They are defined as,

$$I \cdot T = \sqrt{\sum_{h=1}^{H} (w_h X_h)^2} \tag{2.26}$$

where $X_h = I_h$ and similarly the k$V \cdot T$ product gets defined with $X_h = V_h$.

12. *Arithmetic (S_A) and Vector (S_V) Apparent Power*: When there is unbalance in the three-phase system, then defining the Apparent power can be ambiguous. The Arithmetic Apparent Power (S_A) is the arithmetic sum of the individual phase apparent powers, while the Vector Apparent Power (S_V) is the vector sum of the individual phase apparent powers. They need not be same in general.

13. *Line Unbalance factor (K_- or K_0)*: This is defined to give an estimate of the unbalance in the three-phase circuit and is expressed as,

$$K_- = \frac{X_-}{X_+} \tag{2.27}$$

for the negative sequence quantities and

$$K_0 = \frac{X_0}{X_+} \tag{2.28}$$

for the zero sequence quantities. The quantity X here may indicate the voltage or the current. Only fundamental quantities are considered in the definition.

14. *Flicker factor (F)*: The flicker of the (Incandescent) lamps due to voltage fluctuation causes discomfort to the human eyes. It depends on the bus voltage regulation and the sufficiency of short circuit capacity. The quantity F as de-

Table 2.1: Harmonic Voltage Limits [IEEE Std 519-1992(1992)]

Bus Voltage	Maximum Individual Harmonic Component (%)	Maximum THD (%)
69 kV and below	3.0	5.0
115 kV to 161 kV	1.5	2.5
Above 161 kV	1.0	1.5

fined in the following is used to estimate the level of discomfortness,

$$F = \frac{\Delta V}{V_N} \cong \frac{\Delta S}{S_{SC}}. \tag{2.29}$$

Here, ΔV and ΔS correspond to the magnitude of the fluctuating voltage or the load and V_N to the nominal voltage and S_{SC} to the short-circuit power of the feeding network.

2.2.6 Philosophy of IEEE Std 519-1992

The utility is responsible for maintaining the quality of the voltage waveform.

The customer is responsible for limiting the harmonic currents injected onto the power system.

2.2.7 IEEE Std 519-1992 Harmonic Voltage Limits

Harmonic Voltage Limits – It is the responsibility of the utility to supply power with a voltage meeting the harmonic levels as specified in Table 2.1.

2.2.8 IEEE Std 519-1992 Harmonic Current Limits

Harmonic Current Limits: It is the responsibility of the customer to limit the harmonics injected into the utility. Unlike in the case of voltage harmonics the levels of harmonics tolerated is considered with respect to the nominal load current, which is taken as the load current over a defined period of time. The limits are as specified in Table 2.2.

Table 2.2: Harmonic Current Limits [IEEE Std 519-1992(1992)]

SCR $=\frac{I_{SC}}{I_L}$	$h < 11$	$11 < h < 17$	$17 < h < 23$	$23 < h < 35$	$35 < h$	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20 - 50	7.0	3.5	2.5	1.0	0.5	8.0
50 - 100	10.0	4.5	4.0	1.5	0.7	12.0
100 - 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

h – harmonic order;
Values shown are in percentage of *average maximum demand load current*;
SCR $\triangleq$ Short Circuit Ratio (utility short circuit current I_{SC} at PCC divided by customer average maximum demand load current I_L);
TDD $\triangleq$ Total Demand Distortion (uses maximum demand load current as the base, rather than the fundamental current (used for computation of THD));
PCC $\Rightarrow$ measurements taken at the point-of-common-coupling.

2.2.9 Sources of Distortion

As already mentioned, it is the connection of nonlinear loads to the supply that are the most detrimental to power quality in utility networks. The use of power electronic converters at all power levels – from the low power supplies to high power dynamic loads such as mill drives and locomotives at the MW level contributes much to the distortion on the power network. To this can be added arc furnaces, electrochemical plants, and or other nonlinear loads. The power network is subjected to harmonics due to solid-state power conversion systems such as:

- Drive control systems in industries and in traction
- HVDC power conversion and transmission
- Inter-connection of wind and solar power converters with distribution systems
- Static-VAR compensators, which have largely replaced synchronous condensers as continuously variable-VAR sources
- Cycloconverters used for low-speed, high-torque AC machines
- Pulse-burst-modulated heating elements for large furnaces

Classification of Harmonic Sources

The harmonic source due to solid-state power controllers are classified into two types:

- Current-Source type of harmonics sources – Harmonic Current Sources **(HCS)**
- Voltage-Source type of harmonics sources – Harmonic Voltage Sources **(HVS)**

Harmonic Current Sources (HCS)

The loads where the harmonic content depends mainly on the characteristics of the load and is less dependent of the AC side parameters are called as Harmonic Current Sources **(HCS)**. The best example for such a load is a rectifier with a large smoothening inductor on the output side. The supply current waveform in that case will not be affected much by the source voltage waveform or the source impedance. The load thus injects a heavy harmonic current into the supply side.

Harmonic Voltage Sources (HVS)

A load like the rectifier with a large output capacitor, has been assumed to behave like a Voltage- source type of harmonic source and is called as Harmonic Voltage Source **(HVS)**. In such a load the supply current shape depends much on the AC side parameters, whereas the voltage at the Point of Common Coupling (PCC) has been considered to be a square-wave. This square-wave is the source of Voltage Harmonic at the PCC.

In this thesis the compensation for current-source type of nonlinear loads is considered. A detailed survey of such loads is presented in the next Section.

2.3 Current-Source Loads and their specifications

Many loads need very high, of the order of kilo amperes, constant and ripple-free current for driving the loads and lay very stringent specifications on the quality of the current waveform. This translates into a stiff alternating current (a (quasi) square) waveform from the utility source. In this section few such loads are introduced and their characteristics and specifications are studied [Rodriguez *et al.*(2005)].

2.3.1 Thyristor-Controlled-Rectifiers feeding DC motors

A DC motor has the most important characteristics that it will never pull-out on loading and hence are very well used in traction, crane, or lift kind of applications. They are fed from a controlled rectifier and, the acceleration and deceleration are controlled by regulating the armature current of the motor, viz the output current of the controlled rectifier. The ripple in the current reflects as ripple torque and leads to vibration and it leads to fast wear and tear of the rotating parts, also causes discomfort to the passengers if used for transportation. The normal speed-control is obtained by the firing angle control and a full four-quadrant operation is possible. The constant output current of the rectifier unfolds as an alternating current source as far as the utility side is concerned. The power demand will be met by changing the firing angle. The current shape being fixed, the amplitude and the time-shift with respect to the reference waveform will vary depending upon the duty the motor is called to serve – acceleration or running at different speeds [Leonard(1985), Dewan *et al.*(1984), Krishnan(2002), Dubey(1989)].

2.3.2 Thyristor-Controlled-Rectifiers feeding CSI drives

Current Source Inverters find applications in several industries like mining applications where VSI drives suffer from voltage reflection, arising due to the long length of the cables from the converter-end to the motor-end and the associated voltage doubling effect. Such inverters are used as drives for Induction Motors, Synchronous Motors, and Permanent Magnet Motors [Leonard(1985), Dewan *et al.*(1984), Krishnan(2002), Dubey(1989), Bose(2002)].

2.3.3 Thyristor-Controlled-Rectifiers feeding Magnet Power-Supplies

The magnet power supply is used in nuclear physics [McCarthy and Wolf(1985)]. It is required to generate and store magnetic field beams for a period in excess of 24 hours with the ripple tolerance of less than 10 PPM (0.001%). The ratings range from 550 V, 300 A or 350 V, 1300 A or 1000 V, 1500 A. This is obtained from a multi-pulse controlled rectifier structure from the source-side and a low-pass (L-C or L-C-L) filter on the output side of the controlled rectifier.

2.3.4 Thyristor-Controlled-Rectifiers for Electro- chemical and metallurgical processes

Battery charging and electro- chemical and metallurgical works require constant current. In the case of battery, the charging current has to be maintained constant during constant-current-charging mode with a stringent specification on the ripple to reduce the heating and loss of battery life. In other electro- chemical and metallurgical processes it is mainly the magnitude of the current with a wide range in kilo amperes for each applications [Rodriguez *et al.*(2005), Edward and W.(1968), Walker(1970)].

2.3.5 Superconducting Magnet Energy Storage Systems

The Superconducting Magnetic Energy Storage Systems (SMES) are being used for storage of electric energy for emergency purposes. While a ramping-up current source is required during storage, the power back-up is provided by drawing energy from the SMES through the Current-Source Inverter operated either in a six-step mode or PWM mode. But seen from the source side it acts as a Current-Source [Wang *et al.*(2013), Zhang and Ooi(1993)].

2.3.6 Charging of Plug-in Electric Vehicles

The growing trend of using electric or hybrid electric vehicles has attracted installations of charging stations along the residential and distribution power grids. This requires that the charging current be regulated which seen from the supply side acts as a Current-Source Nonlinear loads [Gomez and Morcos(2003), Turker *et al.*(2014)].

2.3.7 Definition: Current-Source Nonlinear Loads

These types of loads present themselves as loads drawing a source current (response) with a shape independent of the source (excitation) voltage waveform of the utility. Thus they are like current sources connected to the utility. Hence they are called as Current-Source loads. They contain current harmonics, the harmonic order and the relative amplitude depending on the type of the load. Since the current (response) contains frequency components in addition to those present in the voltage (excitation) (which

is (supposedly) to be sinusoidal), they are classified as Current-Source Non-linear loads (CSNL).

2.3.8 Source side requirements for the loads

The input voltage to the drives indicated in this Section is expected to be sinusoidal at or closer to nominal frequency and voltage. However there is always a deviation from this condition and there will be voltage variations and the input may also contain harmonics. This can affect the operation of the drives and hence it is necessary to compensate for such disturbances from the supply side by means of a multi-function series compensator, either in the form of a Series Active Filter (SAF) or a compensator like a Dynamic Voltage Restorer (DVR) in combination with a series passive filter (SPF).

2.4 Components of a Power-Quality Compensator

A Power Quality compensator is composed of several components. They are mainly:

- the compensator power circuit consisting of:
  - the passive compensator
  - the active compensator.
- the appropriate sensors to measure the quantities required to operate the compensator.
- the techniques or algorithms to extract the compensating quantities.
- the switching technique for the switched mode active filter.
- the controller to reduce error and improve the speed of response.
- a protection and monitoring system to monitor all the variables – analog and digital for the safe operation of the over all system and finally
- the computer system (DSC/ FPGA/ μC platform) to implement the desired functions listed above.

The developments in each of these areas is briefly reviewed in the following Section.

2.5 Topologies of a Power-Quality Compensator

2.5.1 Multi-pulse Multi-phase input rectifier

Traditionally the input current shaping nearing sinusoidal has been achieved by using multi-pulse multi-phase rectifiers. An input transformer with a complex set of carefully selected number of secondary sections with appropriate number of turns on each winding and the Star-Delta phase shifting is used for the purpose. Series connections on the secondary side gives better DC voltage and parallel connection on the primary side gives a smoother overall current. This is a scheme in which the harmonics **generation** by the load at the PCC is minimized. It is very rugged and hence reliable; but the size, cost, space, and efficiency are of concern. Several schemes are discussed in [Paice(1996), Tanaka *et al.*(1998)].

2.5.2 Passive Filters

Passive Filters are widely used to control harmonics, especially the 5^{th} and 7^{th} harmonics. Most filters consist of series L and C components that provide a single-tuned notch with a low-impedance ground path [Das(2004), Czarnecki and Ginn-III(2005), Volkov(2002), El-Saadany *et al.*(2000)].

Advantages:

The Passive Filters (PF) have advantages of being simple, cheaper, and efficient compared to the Active Filters (AF). But AFs become attractive at lower frequency range, due to the reduced switching speed required. However the higher amplitudes of harmonics at the lower-frequency-end can result in increased losses, compared to the increased switching-frequency required at the higher harmonic frequencies, with lower magnitudes.

Disadvantages:

Some of the problems associated with passive filters are:

- Their effectiveness diminishes over time as their capacitors age, resulting in the decrease of the value of the capacitance and thus raising their notch frequency.

- They attract harmonic currents from all sources in the network - new, known, and unknown and they may become overloaded.
- Parallel resonance between the power system and the passive filter causes the amplification of harmonic currents on the source side at a specific frequency.
- The passive filter may engage in series resonance with the power system, so that voltage distortion produces excessive harmonic currents flowing into the active power filter.

Hence taking into considerations the viability, advantages, disadvantages and cost of passive filters the concept of active filters came into existence.

2.5.3 Switched mode rectifiers

PWM rectifiers [Chattopadhyay and Ramanarayanan(2004)] have been used for high power factor and low THD current inputs. But its rating and losses are higher; it is a series regulator, which acts as a controlled throttle and hence decides the reliability of the overall system.

2.5.4 PWM Current-Source rectifiers

PWM Current-Source-Rectifiers with input capacitor filters, AF, various modulation techniques have been reported in [Zargari *et al.*(1994), Kwak and Toliyat(2006)] and [Rockwell Automation(2014)].

2.5.5 Active Filters

The passive filters have been in use due to their simplicity. However there are concerns of voltage and/or current amplification at some frequencies and the losses. The active filters are being considered now-a-days with the availability of the technology. There has been a lot of research into the selection of topology for Current-Source type of nonlinear loads. After an initial conceptualization of harmonic current injection by Bird *et al.,* [Bird *et al.*(1969)], Ametani [Ametani(1976)], and the work by Gyugyi *et al.,* [Gyugyi and Strycula(1977), Stacey and Strycula(1976)] using active devices in the linear zone, the active filtering techniques using switching devices became feasible only during the early part of 1990s [Akagi(1996)]. Several papers by Peng [Peng(2001),

Peng(1998)] and Akagi [Akagi *et al.*(1990)] contributed greatly to the technology. Novel techniques were also presented by [El-Habrouk *et al.*(2000), Cheng *et al.*(1998)], [Peng *et al.*(1993), Zamil and Torrey(2001), Fujita and Akagi(1998)].

2.5.6 Hybrid Filters

Hybrid filters are developed to reduce the size of the Active Filters, but requires a bulky passive filter and a voltage-matching transformer. But they can only compensate for the harmonics and not for the reactive power. They are basically used for enhancing the performance of the passive filters and to protect the passive filter from power resonance. A transformerless hybrid filter with a 7^{th} harmonic tuned filter in series with an AF, feed-forward control for 5^{th} harmonic, series line reactor at the input of a rectifier with capacitor at the output is given in [Srianthumrong and Akagi(2003)]. A variant of the hybrid filter with an AF in series with a passive (L-C) filter and employing voltage mode control for a load with the diode rectifier with capacitor is presented in [Jou *et al.*(2005), Rastogi *et al.*(1995)]. It claims of good features of PAF and Hybrid Filters in terms of size, cost, and performance parameters, but is complex to implement and there are no reports of this topology applied to Current-source type of nonlinear loads.

2.5.7 Unified Power Quality Compensator

The Unified Power Quality Conditioners (UPQC) are also developed in line with the FACTS device UPFC (Unified Power Flow Controller) to mitigate the effects of source disturbance on the loads and pollution of the utility by the loads. A complex system with an Active Rectifier, Series Active Filter, and a Shunt Active filters is also reported [Jimichi *et al.*(2008), Graovac *et al.*(2007), Fujita and Akagi(1998)]. It involves three converters connected to the common DC bus and a series transformer, adding to the total rating of the system. A detailed survey is reported in [Khadkikar(2012)]. The commercialization of the topologies is limited by the higher rating requirements of the series and the shunt converters and the hence the cost.

2.5.8 Current-Source versus Voltage-Source Active Filters

The Active Filters can be implemented through the Current-Source or Voltage-Source. The comparative evaluation of these are presented in [Routimo *et al.*(2007)] and [Benchaita *et al.*(1999)].

2.5.9 Design of PAF and SAF

The design of converters has been considered to some extent in the literature [Vilathgamuwa *et al.*(2003), Neilsen *et al.*(2001), Zamil and Torrey(2001)]. The design and implementation of Active Filters is also reported in the literature [Jimichi *et al.*(2008), Green and Marks(2003)].

2.6 Compensating quantity extraction Technique

The compensating current extraction is an important task in the implementation of harmonic filtering – passive and/or active filtering, series and/or shunt compensation. The compensating current is to be injected into the line to make the mains current and/or the load voltage sinusoidal without harmonics and achieve unity power factor. Several techniques have been proposed in the literature. The compensating current extraction techniques are reviewed in this Section and it may be noted that it is easy to derive the techniques for voltage compensation (in many cases) therefrom. The power theory analysis, if done, will reveal the result of the compensation.

2.6.1 Extraction Techniques

The Instantaneous Reactive Power Theory presented by [Akagi *et al.*(1984)] and [Akagi *et al.*(2007)] continues to be one of the best algorithms. It is an example of the *direct techniques*. Some *indirect techniques* suggested by [Singh *et al.*(2007), Chatterjee *et al.*(1999), Chattopadhyay and Ramanarayanan(2003)] are also available. The techniques given by [Allmeling(2004), Mossoba and Lehn(2003), Rao *et al.*(2008)], [Ovaska and Vainio(2004), Moreno *et al.*(2004), Bhattacharya *et al.*(1998)], as well as [Marks and Green(2002), Soares *et al.*(2000)] are novel and innovative. Many algorithms, which fall in the class of *line-synchronized*, have been proposed in the literature [Karimi-Ghartemani(2006), Shiguo and Zhencheng(1995)].

Compensating current extraction techniques for a three-phase active power filter

The compensating technique should be able to provide better compensation and give a better profile of the compensated mains current under different conditions like:

- Mains Voltage unbalance in phase and amplitude.
- Mains voltage distortion.
- Unsymmetrical/Unbalanced load.
- Under transient conditions.

The various Compensation Techniques (Reference current extraction techniques) for three-phase three-wire active power filter available in the literature are:

- Instantaneous active and reactive power theory (p-q theory).
- Instantaneous active and reactive current method (i_d-i_q method).
- Synchronous Reference frame method
- Extension p-q theory.
- Synchronous Detection method
  - Equal Resistance Synchronous Detection Method
  - Equal Current Synchronous Detection Method
  - Equal Power synchronous Detection method

2.6.2 Instantaneous Active and Reactive Power (p-q) theory

In 1983, Akagi. et al. proposed the instantaneous active and reactive power theory, commonly known as p-q theory [Akagi *et al.*(1984), Jou(1995)], though an earlier definition to this is made by Lyon [Lyon(1933)]. The p-q theory is based on instantaneous values in three-phase power systems with or without neutral wire, and is valid for steady state or transitory operations, as well as for generic voltage and current waveforms. The p-q theory consists of an algebraic transformation (Clarke's transformation) of the

three-phase voltages and currents in the a-b-c coordinates to the α-β coordinates, followed by the calculation of the p-q theory instantaneous power components and hence calculating the compensating currents by using the instantaneous power components. These p and q components are further split into average and oscillating components. Then depending upon the requirement based on the power theory the components of p and/or q are chosen. Then an inverse transformation gives the currents in the three phases to be compensated. The disadvantages of this theory is that it cannot compensate for the unbalanced condition of the mains.

2.6.3 Modified (extension) p-q theory

The p-q theory since its proposal has been applied in the control of three-phase active power filters. However, power system voltages being often unsymmetrical, control in unsymmetrical voltage system using the p-q theory does not provide good performance. Hence to overcome the inabilities of p-q theory under unbalanced conditions, Extension p-q theory was proposed which gives better mains voltage profile even for the unsymmetrical voltage system [Komatsu and Kawabata(1997)]. The performance of this method is better than p-q theory under unbalanced condition of the mains.

2.6.4 Instantaneous Active and Reactive Current i_d-i_q Method

In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. The mains voltage v_i and the polluted load currents i_l are initially calculated in α-β coordinates, as calculated in the instantaneous active and reactive power theory. Then, the d-q load current components are derived from the synchronous reference frame.

Instantaneous active and reactive load currents i_{l_d} and i_{l_q} can be decomposed into oscillatory and average current components. The fundamental current of positive sequence is transformed to constant quantities, which constitutes the average current components. All higher order current harmonics including the fundamental current of negative sequence are transformed to non constant quantities and undergo a frequency shift in the spectra, and so, constitute the oscillatory current components. These assumptions are valid under symmetrical and sinusoidal mains voltage conditions. Eliminating the average current components by high pass filter the currents

that should be compensated are obtained. The main disadvantage of instantaneous active and reactive current method is that it cannot compensate for the unbalanced condition of the mains.

2.6.5 Synchronous reference frame method

In this method the measured load currents are transformed into the rotating reference frame (d-q frame) that is synchronously rotating at the line voltage. The line frequency components of the load currents become constant quantities and the harmonic components are frequency shifted in the d-q reference frame by ω_s – the line frequency. A low-pass filter in the d-q frame, with a cutoff at ω_s can be used to extract the constant components. If the phase of the d-axis current is locked to the a-phase voltage e_a of the a-b-c coordinates with a PLL, then the I_d^{dc} component represents the fundamental real current and I_q^{dc} represents the fundamental reactive component. By subtracting these quantities from the I_{l_d} and I_{l_q} quantities the harmonic content is obtained. These quantities can then be used to develop the compensating quantities for the active filter by transforming back to α-β co-ordinates and then to a-b-c coordinates. The main advantage of Synchronous reference frame method is there is no need to supply voltage information. However the method cannot compensate for the unbalanced condition of the mains [Marques(1998)].

2.6.6 Synchronous detection Method

Methods such as instantaneous power theory are used to detect reactive and harmonic current components, and to determine proper compensating current components to be fed back to the system. When the voltage source is significantly unbalanced, great errors may result from the calculation formulae by direct application of the instantaneous power theory; hence this algorithm has been proposed to overcome the inabilities of the other compensating techniques under unbalanced conditions. The Synchronous detection method was widely used in communication systems [Chen *et al.*(1994*b*), Chen *et al.*(1994*a*)] and [Valouch *et al.*(1999)]. In three phase circuits the synchronous detection method is proposed to calculate the per phase voltage and current and determine the compensation current to be injected into the system. It provides the capability to balance line currents and voltages, achieves unity power fac-

tor, and eliminates harmonic currents in the load side. To the problem of unbalanced three phase systems the average compensating current in each phase is determined by three different approaches as viewed from the source side. They are,

Equal Current Synchronous Detection method

In this case the compensating currents of each phase are appropriately calculated under the assumption that source line currents are equal after compensation. It gives a better profile of the line current after compensation [Chen *et al.*(1994*a*)] and [Chen *et al.*(1994*b*)].

Equal Power Synchronous Detection method

This approach based on the assumption that each phase shares equal real power of the total demand after compensation [Chen *et al.*(1994*b*)]. The necessary phase currents of the source to meet this condition are calculated and subtracted from the load phase currents to obtain the compensating currents.

Equal resistance Synchronous Detection Method

This method is based on the assumption that effective resistance presented to all the phases are equal after compensation [Chen *et al.*(1994*b*)]. Accordingly the compensating currents are calculated.

Key features of Synchronous Detection Methods

- All the three methods of the synchronous detection principle namely – equal current approach, equal power approach, and equal resistance approach give a better profile of the mains current after compensation under balanced condition of the supply and balanced/unbalanced condition of the load.

- Equal Resistance Synchronous Detection Method provides a better profile of mains current after compensation even under phase and magnitude unbalanced condition and distorted condition of the mains.

2.6.7 Sinusoidal subtraction method

The sinusoidal subtraction [Round and Ingram(1997)] algorithm is based on Fourier analysis. It calculates the real part of the fundamental load current and is on per phase basis. The algorithm is capable of maintaining the input power factor of the mains close to unity and forces the mains current to be sine wave even under distorted or non distorted supply voltage. It is based on Fourier analysis. Any suitable implementation can be used to evaluate the in-phase component. This does not have any feedback.

2.6.8 Adaptive noise cancellation

In adaptive noise cancellation (ANC) [Shiguo and Zhencheng(1995)] based active power filter, a primary input containing the corrupted signal (the load current) and a reference input (system voltage) are correlated. The signal correlating completely with the system voltage is adaptively filtered out and subtracted from the load current to get the compensating signal. This algorithm is not sensitive to variation in supply frequency, however has feedback, which can lead to instability.

This technique is a synchronous extraction technique and the signals are locked in phase and amplitude to the line signals, using the PLL and amplitude locking. This class of algorithms are discussed further in Chapter 3.

2.6.9 Notch filtering

In the notch filtering [Marques(1998)] method the load current is filtered by a notch filter, which filters out the fundamental while leaving the harmonic components. A single notch filter with a bandwidth of 5 Hz has good isolating characteristics. The filter can significantly contribute to reduce the output THD and can recover from a step change transient, in 10 fundamental cycles. The load current is filtered to leave the harmonics. The harmonic currents are subtracted from the load current and are injected into the power line. This algorithm is applied on per phase basis. A disadvantage of the algorithm is that, it will not be able to compensate for the reactive power component present in the load current. It is possible to design a digital linear phase FIR filter, with a plan to account for the delay in the next cycle.

2.6.10 Performance of compensating algorithms

The active power filtering algorithms discussed in this Section above have been simulated in MATLAB® and Simulink®. The nonlinear load is a three-phase uncontrolled rectifier fed from 400 V, 50 Hz, AC supply. Output has an LC filter with L = 10 mH and C = 100 μF and the load is a resistance of 5 Ω/10 Ω switchable, at a convenient instant of time, as desired, to show the effect of dynamic variation of load on the algorithm. Input current of the three-phase uncontrolled rectifier is fed to the three-phase active power filter algorithms. The simulation is run for 5 s, with a load change from 28.92 kW (10 Ω) to 57.84 kW (5 Ω) at 3 s. Following cases are considered for performance analysis:

Case-1: Under balanced supply and load

Case-2: Under balanced supply conditions with a 100% sudden load change

Case-3: Under unbalanced supply voltage conditions (only magnitude unbalance: V_a = 250 V, V_b = 230 V and V_c = 220 V)

Case-4: Behavior of algorithms under unbalanced source (phase and magnitude: $V_a = 250\angle 0°\text{V}$; $V_b = 230\angle -130°\text{V}$; $V_c = 220\angle 125°\text{V}$)

Case-5: Behavior of algorithms under source unbalanced and distorted supply (v_D) conditions (V_a = 250 V, V_b = 230 V and V_c = 220 V with a distortion of 5^{th} and 7^{th} harmonics given by $v_D = v_5 + v_7$ where $v_{5m} = 20\sqrt{2}$ V and $v_{7m} = 30\sqrt{2}$ V, added to all phases)

The summary of the results of simulations for the cases considered are presented in Table 2.3. The following observations are made:

- There is a clear advantage in terms of the speed of response in the Synchronous Extraction (ANC) and Sinusoidal Subtraction methods compared to the transformation based methods and Notch filtering.
- All the compensating algorithms found in the literature perform well under balanced conditions of the mains and balanced/unbalanced load.
- The transformation based methods and Notch filtering methods cannot generate the correct compensating quantities under the unbalanced condition of mains.

This comparative study of these algorithms is reported in the literature [Gonda *et al.*(2009)].

Table 2.3: Summary of results of simulations for the cases considered

Algorithm	Case-2	Case-3	Case-4	Case-5
Equal resistance synchronous Detection Method	0.65 s	Good	Good	Good
Equal Power synchronous Detection Method	0.65 s	Good	Good	Good
Equal Current Synchronous detection Method	0.65 s	Good	Good	Good
Instantaneous active and reactive power theory (p-q theory)	0.50 s	Fails	Fails	‡
Modified (extension) p-q theory	0.50 s	Good	Good	‡
Instantaneous active and reactive current method (i_d-i_q method)	0.45 s	Fails	Fails	‡
Synchronous Reference frame method	0.45 s	Good	Good	‡
Adaptive noise cancellation	0.05 s	Good	Good	Good
Sinusoidal subtraction method	0.02 s	Good	Good	—
Notch filtering	0.20 s	Not good	Not good	Not good
‡ – For such cases the compensating currents are such that the source currents will be sinusoidal after ideal compensation				

2.7 Switching Techniques for the Active Filters

Pulse width modulation (PWM) methods are employed in order to determine the instantaneous switching states of the Voltage Source Converters (VSC) [Juan.W.Dixon *et al.*(1994)]. Realization of harmonic free utility interface applications by parallel or series active filters is characterized by the following current regulator requirements for the inverter:

- Non-sinusoidal multiple frequency current tracking.
- Ability to operate with low inverter output filter inductances.
- High $\frac{di}{dt}$ reference current tracking and high current regulator bandwidth for tracking of high frequency harmonics.
- Minimization of low as well as high frequency current errors.
- Desired implementation by a constant switching frequency PWM scheme.
- Maintain predictable current ripple bounds.
- Avoid phase interactions and limit cycles in current.

- Low sensitivity to inverter output filter inductance L_f error and voltage V_f estimation error in current regulator.
- Low sensitivity to analog/digital implementation issues such as sample and hold delays, inverter dead time delays.
- Ability to implement higher inverter switching frequency without DSC or μC limitation of computational delays.
- Allow a simple and cost-effective implementation
- Low switching losses.
- Good utilization of DC power supply, that is to deliver a higher output voltage with the same DC supply.
- Good linearity in voltage and or current control.
- Low harmonics contents in the output voltage and/or currents, especially in the low-frequency region.

Different methods of switchings are discussed in the following.

2.7.1 Hysteresis Current Control

The hysteresis current control (HCC) technique has proven to be the most suitable solution for all the applications of current controlled voltage source inverters where performance requirements are more demanding, such as active filters and high- performance ac power conditioners [David M.E. Ingram(1997)]. Hysteresis PWM refers to the technique where the output is allowed to oscillate within a predefined error band, called as *hysteresis band*. This is a method of controlling a voltage source inverter so that an output current is generated which follows a reference current waveform. This method controls the switches in an inverter asynchronously to ramp the current through the link inductor up and down so that it follows a reference. This technique does not require any information about the inverter load characteristics. As long as the reference signal is known and the inverter output voltage is not saturated, the inverter output will always follow the reference.

Performance

Hysteresis current control is the easiest control method to implement, characterized by unconditional stability, very fast response, and good accuracy. On the other hand, the basic hysteresis technique exhibits also several undesirable features, such as variable switching frequency and heavy interference among the phases in case of three-phase systems with isolated neutral, but additional circuitry can be used to limit the maximum switching frequency.

2.7.2 Space Vector Modulation

Space Vector Modulation (SVM) technique [Espinoza *et al.*(1996)] and [Mendalek and Al-Haddad(2000)] is most widely used for voltage source inverters. This method is based on the fact that the number of states for a voltage space-phasor is given by m^k, where m – the number of levels and k – the number of legs of the inverter. Thus, for a 2-level 3-phase inverter there are 8 possible states (vectors) of the voltage space-phasor, amongst which two are zero. It is possible to generate the desired voltage space-phasor, by switching between adjacent two vectors in a given sector and a suitable zero vector. The method then needs the calculation of different time durations (T_1, T_2, and T_0; with T_1+T_2+T_0=T_s) in a switching cycle T_s. This technique requires the computation of the modulating signal and hence there can be problem of instability because of the feed forward nature of the calculations involved.

Performance

This method is very well suitable for digital implementation and gives the highest possible fundamental voltage for a given DC bus voltage. Unlike the hysteresis control this method of switching requires the reference voltage to be calculated and hence the model of the system is required. This also implies that the response is sensitive to variations in the system parameters. The switching frequency can be optimally selected based on the requirement of speed of response and losses in the converter.

2.7.3 SVM based HCC

This is a new concept of current control techniques which combines the Hysteresis Current Control and the Space vector Modulation [Kwon *et al.*(1998), Marei *et al.*(2002),

Espinoza *et al.*(1996)]. This control algorithm overcomes the disadvantage of the HCC and SVM control if working individually, that is high switching number of HCC and time consuming of SVM. This technique also works on the principle of tracking a reference voltage vector in a given sector based on the principle of SVM but uses Hysteresis Control technique to achieve that objective.

2.7.4 Carrier based Modulation

The carrier based modulation [Mohan and Robbins(2002)] is based on the comparison between a carrier signal of suitably higher frequency that determines the switching frequency and a modulating signal decided by the current trajectory to be followed. Like the space-phasor modulation this technique also requires the computation of the modulating signal. There can be problem of instability because of the feed forward nature of the calculations involved.

2.7.5 Predictive current control

Predictive control of VSI drives has been widely considered in the power electronics industry [Corts *et al.*(2008)]. The method requires the estimation of the system parameters. It is possible to determine the appropriate voltage vector to minimize the error, given the constraints from the switching states of the converters. Predictive control has been used in APF applications [Marks and Green(2002)]. The deadbeat control attempts to achieve the tracking of the reference quantity with one cycle delay. It has found applications in the control of VSI [Kukrer(1996)] and in applications for current control [Corts *et al.*(2008)].

2.7.6 Unified Constant Frequency Integration Control

This technique suggested by Smedley [Smedley *et al.*(2001), Qio *et al.*(2004)] is an elegant *indirect method* of control of converters wherein the determination of the compensating quantities and switching are integrated together. It has very good dynamic and steady-state performance.

2.8 Conclusion and Problem Definition

A thorough review of the necessary aspects of a Power Quality Compensator namely – power theory, compensator quantities' extraction techniques, the topology of the compensator, the switching techniques, and the feedback control techniques is presented. This study led to the following observations:

- It is found that not much attention is devoted in the literature to the suitability of the topologies for any type of nonlinear load and more so with the current source type of nonlinear loads. Hence detailed study is proposed to be conducted to arrive at a suitable topology – a combination of SAF, SPF, PPF, and PAF.

- From a Power Theory point of view it is more meaningful to consider the time-domain approach and extraction technique must extract the compensating current to have the same shape as that of the source voltage (Note: single-phase being under consideration), and the voltage for the series compensator to be of necessary shape and magnitude to meet the load requirement. The IEEE Std. 519: 1992 is used as a reference.

- Among the extraction techniques, it is found that the methods based on synchronous extraction perform better than other methods and hence focus is laid on searching for better algorithms in that direction.

- It is decided to adopt the hysteresis control for the compensating current injection considering its superiority over other methods in terms of ease of implementation and stability aspects. However considering the problem of switching frequency and voltage levels during switching, attempts are planned to devise better switching to reduce the number of switchings and the voltage swing.

These are presented in detail in the following chapters.

Chapter 3

Novel Algorithms for extraction of compensating quantities

3.1 Introduction

The extraction of harmonics and/or the fundamental from a distorted waveform is an important process in the implementation of custom power-devices. Several schemes have been proposed in the literature. Among these, the algorithms based on synchronous (with respect to the supply voltages) extraction (both in phase and amplitude) have certain advantages compared to the others. Amplitude-locked loops (ALL) have been in use in signal-communication systems but are limited to sinusoidal inputs. There is a need – for fast and rugged algorithms to synchronously extract harmonics and/or the fundamental from a distorted waveform, in many power system applications. In this chapter two novel schemes, are proposed for synchronous extraction of harmonics and/or the fundamental from a distorted periodic waveform. The operation of the algorithms, their performance, and design aspects thereof are briefly discussed. The real-time hardware implementation details of the algorithm on a real-time hardware-emulation platform – a dSPACE Modular system (configured around the DS1006 processor board) is discussed and the results are presented.

3.1.1 Brief review of synchronous extraction techniques

The extraction of harmonics or the fundamental component of voltages and/or currents is one of the main tasks in the implementation of custom power-devices. The techniques

available for this purpose broadly fall into single-phase and three-phase categories. They can also be classified into open-loop techniques and closed-loop techniques. A comparative evaluation of some of these methods can be found in [Gonda *et al.*(2009)]. The importance of efficient extraction and the applications thereof are covered extensively in [Akagi *et al.*(2007)]. The closed-loop techniques have the distinct advantage of being capable of holding the extracted signals synchronized (zero-deviation in amplitude and phase (time shift, to be more precise)) to that in the input, which is very important in all applications connected to the utility grid.

Phase- and amplitude locking have been in use in the field of signal-communication for the purpose of amplitude modulation or demodulation. In the year 1991, a vector-locked loop (VLL) was presented by DaSilva in a patent [Marcus K. DaSilva(1991)], wherein peak detection is used for magnitude determination. A scheme for amplitude-locking, has been presented by Pettigrew in a patent [Pettigrew(1994)] filed in the year 1994. Both the aforementioned schemes assume the input to be a sinusoid and hence cannot directly be used for extracting harmonics from distorted inputs. Moir [Moir(1995)] has presented an analysis of the scheme given by Pettigrew.

In the area of synchronized filtering of a non-sinusoidal (distorted) waveform, the scheme presented in 1995 by Luo, et al. [Shiguo and Zhencheng(1995)], has the desirable feature of staying locked to the PLL (phase-locked loop) reference while being simple to understand and to implement. However, its settling-time is a function of the integrator gain and an increase in the gain to improve the dynamic performance, leads to an increased distortion in the filtered output. In the year 2002 a VLL for synchronous extraction of harmonics was presented [Karimi-Ghartemani and Iravani(2002)]. An improved scheme was presented [Karimi *et al.*(2003)], wherein a low-pass filter is introduced in cascade with the integrator, which improves the steady-state response and allows for a higher gain – thereby reducing the settling-time.

In the following Sections the operation of the proposed schemes are explained; the approximate transient analysis and LTI model development, the steady-state analysis including the performance on tracking the variation and with distortion are presented. The steady-state and transient performances are discussed. Design considerations are dealt with and the results from off-line simulation and real-time implementation are presented.

3.2 Algorithm-1: A Novel Algorithm

3.2.1 Introduction – Structure of the algorithm

The structure of the proposed algorithm is as shown in Figure 3.1. It has two locked-

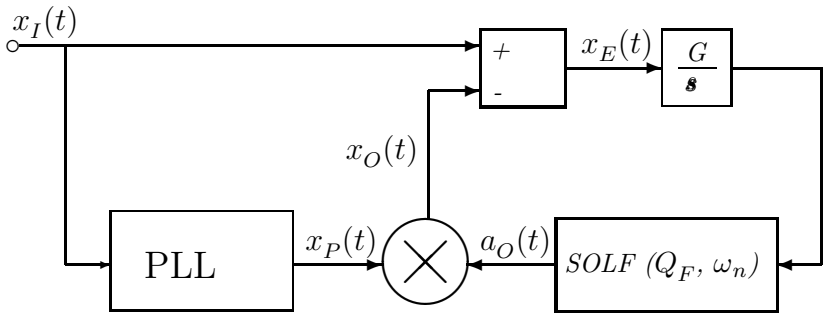


Figure 3.1: The Block diagram of a proposed VLL

loops: a phase-locked loop for phase and frequency synchronization, and a novel amplitude-locked loop for the fundamental amplitude determination, thus leading to the name Vector Locked Loop (VLL). The Second Order Low-pass Filter (SOLF) used here has the standard form as given in (3.1)

$$F(s) = \frac{1}{\frac{s^2}{\omega_n^2} + \frac{s}{Q_F \omega_n} + 1}. \tag{3.1}$$

The characteristics of the SOLF are as shown in Figure 3.2.

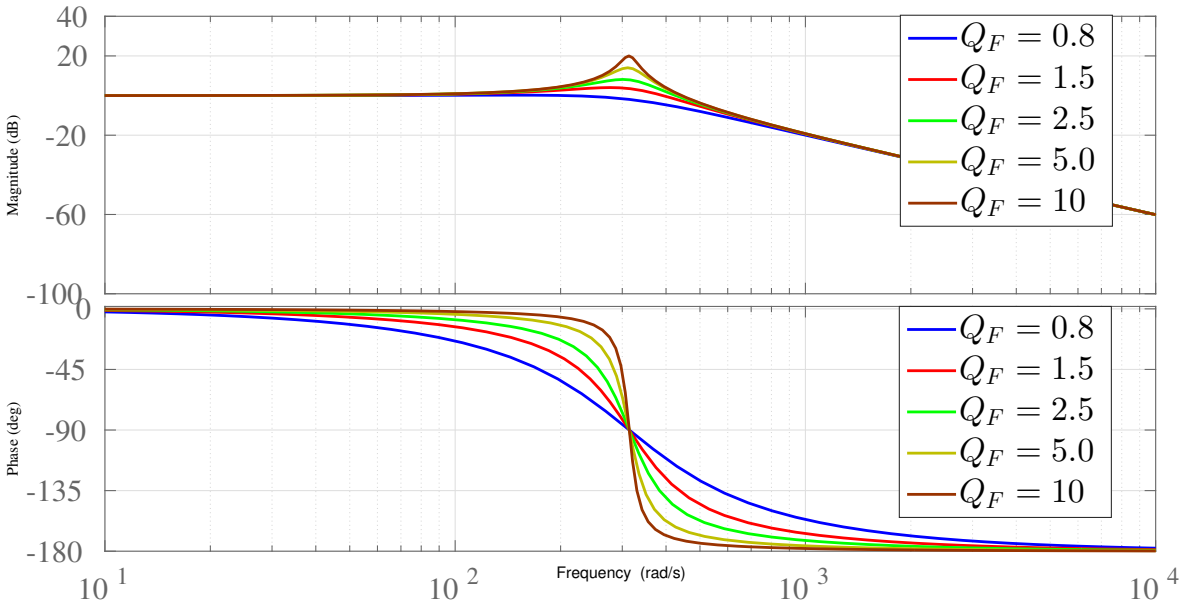


Figure 3.2: Characteristics of the SOLF

Consider the input,

$$x_I(t) = \sum_{h=1}^{\infty} C_h \sin(h\omega_1 t + \phi_h), \tag{3.2}$$

a periodic waveform with no constant component. The output of the PLL (pre-tuned to a free-running frequency of ω_1) which is purely sinusoidal is in phase with the fundamental component of the input. Thus,

$$x_P(t) = B_P \sin(\omega_1 t + \phi_1). \tag{3.3}$$

The essential idea is to compare the instantaneous values of the input, $x_I(t)$ and the output, $x_O(t)$ (scaled version of $x_P(t)$) and to adjust the scaling factor ($a_O(t)$) by a feedback in order to minimize the error. The integrator and the second-order low-pass filter (SOLF) are chosen such that the above operation is performed only on the fundamental component of $x_I(t)$, thereby desensitizing the loop to all the harmonics. Therefore in the steady-state, the output $x_O(t)$ exactly locks on to the fundamental component of $x_I(t)$ (both phase and amplitude) and the signal $x_E(t)$ is the sum of all harmonic components in $x_I(t)$. In other words, $a_O(t)$ settles to a constant (A_O) such that $A_O B_P$ is the amplitude of the fundamental component of $x_I(t)$. The integrator gives the additional advantage of zero steady-state error.

In this section, an approximate analysis of the transient operation of the loop and subsequently, an approximate linear time-invariant model for the proposed VLL are presented. It should be noted here that the parameters chosen for the SOLF achieve the following, which are important and necessary in the operation of the algorithm:

1. Along with the integrator it contributes to a 60 dB/decade attenuation of the harmonics in $x_E(t)$ thereby producing a more or less clean constant value at a_O in the steady-state.

2. In cases where Q_F is greater than 1, it helps in amplifying the residual fundamental by a gain depending on the choice of Q_F, which determines the peak of the magnitude plot at ω_n, thus selectively enhances the loop-gain.

3. It also provides 90° phase-lag at ω_n which is required for achieving 180° phase-lag for optimum negative feedback.

The features 2 and 3 are very crucial and distinct from a flat frequency response. It must be noted from Figure 3.2 that a large value of Q_F will make the gain and phase very sensitive for variation of ω_1 around ω_n, which will affect the optimal conditions of operation of the scheme. These will be explained in the following section.

3.2.2 Approximate Transient Analysis

It can be seen that the proposed VLL is a periodically time-varying system since the multiplier may be visualized as an amplifier whose gain varies periodically with time as does $x_P(t)$. An exact and rigorous analysis of such a system would involve the use of complex transforms [Desoer and Kuh(2009), Balabanian and Bickart(1969)] at the expense of an intuitive feel for its working. Therefore an approximate analysis which gives a better insight into the working of the loop is presented here. Assume, for simplicity, that $x_I(t)$ is a pure sinusoid with frequency ω_1, amplitude $C_1(t)u(t)$, and $\phi_1 = 0$. Assuming the PLL amplitude B_P as unity, the amplitude of $x_O(t)$ is now $A_O(t)$ which can be seen as the time-variation of the prospective constant component in $a_O(t)$. The following analysis is performed for a step change of magnitude C_1, in the input amplitude. The PLL is assumed to be fast enough and have attained steady-state for the purpose of analysis.

At any instant during the transient, the error signal in the loop is,

$$\begin{aligned} x_E(t) &= x_I(t) - A_O(t)x_P(t) \\ &= C_1 \sin(\omega_1 t) - A_O(t) \sin(\omega_1 t) \\ &= [C_1 - A_O(t)] \sin(\omega_1 t). \end{aligned} \tag{3.4}$$

This error signal is a sinusoid of frequency ω_1 which, after passing through the integrator and low-pass filter, undergoes a phase-shift of ϕ_1 and a gain of $\frac{G}{\omega_1}G_F$, where G_F is the gain of the SOLF at any input frequency ω_1. Therefore the signal $a_O(t)$ may be expressed as,

$$a_O(t) = \frac{G}{\omega_1}G_F[C_1 - A_O(t)] \sin(\omega_1 t + \phi_1). \tag{3.5}$$

This signal then gets multiplied by $x_P(t)$ to produce a constant component and a $2\omega_1$

component in $x_O(t)$. Mathematically,

$$x_O(t) = \frac{G_F G}{\omega_1}[C_1 - A_O(t)]\sin(\omega_1 t + \phi_1)\sin(\omega_1 t). \tag{3.6}$$

This can be resolved into a constant component and a $2\omega_1$ component as shown in (3.7),

$$x_O(t) = \frac{G_F G[C_1 - A_O(t)]}{\omega_1}\left[\frac{\cos(\phi_1) - \cos(2\omega_1 t + \phi_1)}{2}\right]. \tag{3.7}$$

Since $x_O(t)$ appears in $x_E(t)$, $x_E(t)$ contains a constant component, a ω_1 component, and as well as a $2\omega_1$ component. The $2\omega_1$ component is assumed to be sufficiently attenuated by the low-pass filter and hence has little effect on the loop operation. However, the constant component is of prime importance since it is responsible to drive the integrator to the requisite value. After accounting for the inversion of $x_O(t)$ at the subtracter, the constant component $X_E(t)$ in $x_E(t)$ is given by,

$$X_E(t) = -\left(\frac{G_F G}{2\omega_1}\right)[C_1 - A_O(t)]\cos(\phi_1). \tag{3.8}$$

Since this signal directly feeds the integrator, it sets the rate at which the integrator output changes and therefore decides how fast $A_O(t)$ reaches C_1. Notice that, the difference $[C_1 - A_O(t)]$ must result in a constant error component with the same sign, so as to ensure corrective action through negative feedback. From (3.8), it follows that $\cos(\phi_1)$ must be negative and as large as possible (in magnitude) to achieve negative feedback and minimum settling-time respectively. The optimal criterion which meets the above requirements is $\cos(\phi_1) = -1$ or $\phi_1 = \pm 180^\circ$ which leads to,

$$\phi_1^{opt} = \underbrace{\text{SOLF lag}|_{\omega_1=\omega_n}}_{-90^\circ} + \underbrace{\text{integrator lag}}_{-90^\circ}. \tag{3.9}$$

For values of ω_1 different from ω_n (within certain limits), the loop performs sub-optimally. The permissible range of ω_1 is discussed in Section 3.2.6 based on stability analysis.

3.2.3 Approximate LTI model

This section describes the evolution of an approximate *time-invariant* model for the proposed VLL. The effect of variations in the fundamental input amplitude identified by $C_1(t)$ is considered here. The model facilitates the selection of parameters – G and Q_F. It takes into account only the effect of the constant component produced by the fundamental error signal. The effects of higher frequencies are neglected on the assumption that they are sufficiently attenuated by the SOLF-integrator combination.

At any instant of time, the constant component in $x_E(t)$ is given by (3.8). When ω_1 is sufficiently close to ω_n, $G_F \approx Q_F$ and $\phi_1 \approx -180°$. This implies,

$$X_E(t) = \frac{Q_F G}{2\omega_1}[C_1(t) - A_O(t)]. \tag{3.10}$$

Taking Laplace Transform on both sides, (3.10) can be written as:

$$X_E(\boldsymbol{s}) = \frac{Q_F G}{2\omega_1}[C_1(\boldsymbol{s}) - A_O(\boldsymbol{s})]. \tag{3.11}$$

From Figure 3.1, we also get,

$$A_O(\boldsymbol{s}) = \frac{G}{\boldsymbol{s}} F(\boldsymbol{s}) X_E(\boldsymbol{s}). \tag{3.12}$$

Substituting for $X_E(\boldsymbol{s})$ from (3.11) in (3.12) and rearranging, we get,

$$A_O(\boldsymbol{s}) = \frac{GQ_F}{2\omega_1}\frac{G}{\boldsymbol{s}}\left[\frac{1}{\frac{\boldsymbol{s}^2}{\omega_n^2} + \frac{\boldsymbol{s}}{Q_F\omega_n} + 1}\right][C_1(\boldsymbol{s}) - A_O(\boldsymbol{s})]. \tag{3.13}$$

A little observation of (3.13) with defining $G_I(\boldsymbol{s}) = \dfrac{G}{\boldsymbol{s}}$ will suggest a LTI model as shown in Figure 3.3.

On further simplification, the closed loop gain is obtained as,

$$\frac{A_O(\boldsymbol{s})}{C_1(\boldsymbol{s})} = \frac{1}{\frac{\boldsymbol{s}^3}{G^2Q_F\omega_1/2} + \frac{\boldsymbol{s}^2}{G^2{Q_F}^2/2} + \frac{\boldsymbol{s}}{G^2Q_F/(2\omega_1)} + 1}. \tag{3.14}$$

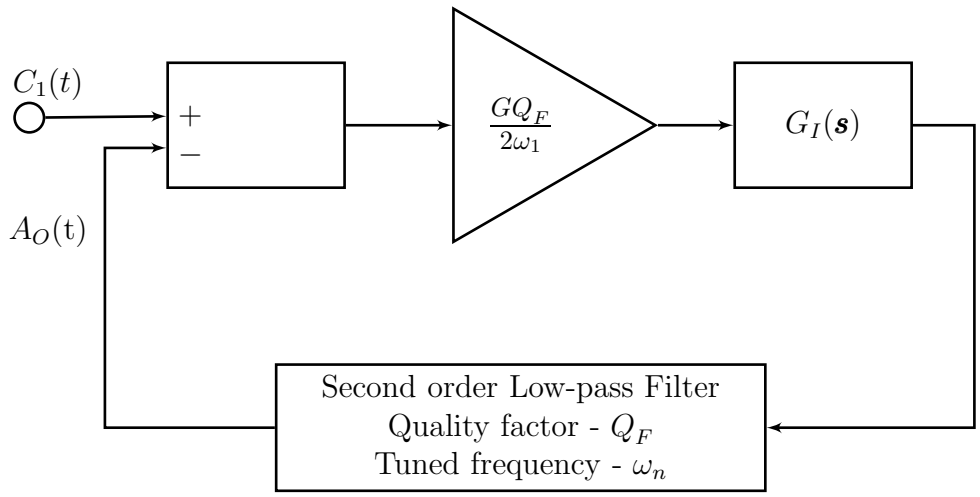


Figure 3.3: Simplified model of the VLL for perturbations on $C_1(t)$

From (3.13) we can write,

$$A_O(\boldsymbol{s}) = \frac{QG}{2\omega_1} G_I(\boldsymbol{s}) F(\boldsymbol{s})(C_1(\boldsymbol{s}) - A_O(\boldsymbol{s})) \tag{3.15}$$

which can be simplified to,

$$\frac{A_O(\boldsymbol{s})}{C_1(\boldsymbol{s})} = \frac{\frac{Q_F G}{2\omega_1} G_I(\boldsymbol{s}) F(\boldsymbol{s})}{1 + \frac{Q_F G}{2\omega_1} G_I(\boldsymbol{s}) F(\boldsymbol{s})} \tag{3.16}$$

$$= \frac{G_e(\boldsymbol{s})}{1 + G_e(\boldsymbol{s})} \tag{3.17}$$

– a unity gain feedback system, where $G_e(\boldsymbol{s}) = \frac{Q_F G}{2\omega_1} G_I(\boldsymbol{s}) F(\boldsymbol{s})$. It can be represented as shown in Figure 3.4.

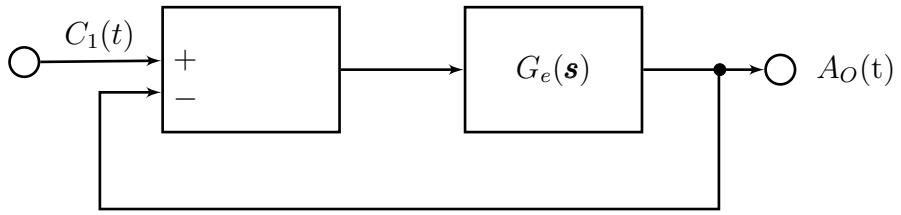


Figure 3.4: Simplified Unity Gain Closed loop equivalent of the proposed VLL

3.2.4 Steady-state analysis

In the steady-state, one may assume that the amplitude of the VLL output closely follows that of the fundamental of the input. In other words, the signal $a_O(t)$ will be

predominantly a constant quantity, closely tracking $C_1(t)$. Based on this assumption the following analyses are presented.

Analysis for Amplitude Modulated Inputs

When the input amplitude is modulated at sufficiently low frequencies (ω_m), the output amplitude manages to follow it closely. It is assumed that $a_O(t)$ contains only the modulating frequency (ω_m) and a constant (C_0). However, in reality, $a_O(t)$ also contains a ripple of frequency $(\omega_1 - \omega_m)$ and $(\omega_1 + \omega_m)$, which when multiplied by $x_P(t)$ are, in turn, responsible for the sustenance of the ω_m component in $a_O(t)$. The linear time-invariant model developed in the previous section *exactly* represents the system for such inputs. The feedback architecture presented in Figure 3.4 will enable the designers in the application of LTI control system techniques for optimizing its tracking abilities.

Note that (3.14) is applicable to any type of input amplitude function $C_1(t)$. As a special case, to show the effect of amplitude modulation, consider an input modulated by,

$$C_1(t) = C_0 + C_m \sin(\omega_m t), \tag{3.18}$$

where C_0 is the constant part of $C_1(t)$ and C_m is the amplitude of the sinusoidal modulation with modulation frequency ω_m.

Now (3.14) can be represented as shown in Figure 3.5, where $\dfrac{A_O(\boldsymbol{s})}{C_1(\boldsymbol{s})} \triangleq G_c(\boldsymbol{s})$ – the closed loop gain, with some input $x(t)$ of the exponential class with frequency $\boldsymbol{s_1}$ and the corresponding output $y(t)$. According to the theory of linear time invariant

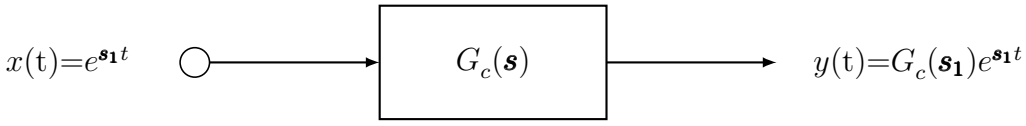


Figure 3.5: Response of Linear Time Invariant Systems to exponential inputs

systems, the steady-state responses of LTI systems to exponential excitations are, the scaled and phase-shifted versions of the inputs, wherein the scale factor is equal to the magnitude of $G_c(\boldsymbol{s})$ evaluated at the input frequency and the phase-shift is equal to

the argument of $G_c(\boldsymbol{s})$ at that frequency [Haykins(2009)]. Accordingly,

$$\begin{aligned} A_O(t) &= G_c(\boldsymbol{s})C_1(t) && (3.19)\\ &= G_c(\boldsymbol{s})(C_0 + C_m \sin(\omega_m t)) && (3.20)\\ &= C_0 + |G_c(j\omega_m)|C_m \sin(\omega_m t - \angle\theta) && (3.21)\\ &= C_0 + C_m \sin(\omega_m t - \angle\theta) && (3.22) \end{aligned}$$

since $|G_c(j\omega_m)| \cong 1$ for the practical values of the design and the system parameters and $\theta = \angle G_c(j\omega_m)$. From (3.14) the output amplitude lags the input by,

$$\theta = \tan^{-1}\left[\frac{2Q_F\omega_m}{\omega_1}\left(\frac{\omega_1^2 - \omega_m^2}{G^2{Q_F}^2 - 2\omega_m^2}\right)\right]. \tag{3.23}$$

3.2.5 Ripple factor in the Output Amplitude

Ideally in the steady-state, the signal $a_O(t)$ must be a constant of magnitude C_1. However, in the presence of the harmonics, $a_O(t)$ contains the constant C_1 and the attenuated versions of the harmonics in $x_I(t)$. Since $x_O(t)$ follows the fundamental in $x_I(t)$, $x_E(t)$ contains only the sum of all the harmonics present in $x_I(t)$. The harmonics are attenuated by the integrator and the SOLF, leaving an RMS ripple in $a_O(t)$ which may be quantified w.r.t. C_1 by,

$$\text{Ripple Factor of } a_O = \frac{G\sqrt{\sum_{h=2}^{\infty}\frac{|F(h\omega_1)|^2}{(h\omega_1)^2}C_h^2}}{C_1}. \tag{3.24}$$

3.2.6 Stability analysis

The LTI model developed in Section 3.2.3 cannot be used to find values of critical G, for a given Q_F, since it takes into account only the effect of constant value caused by the ω_1 component in the loop. For larger G, the $2\omega_1$ component in (3.7) cannot be neglected despite attenuation by the SOLF. The surviving $2\omega_1$ component gets multiplied by $x_P(t)$ to produce ω_1 and $3\omega_1$ components. This ω_1 component appears alongside the original ω_1 component (due to the error $C_1(t) - A_O(t)$) thereby giving the effect of an increased constant loop-gain. The exact calculations of these higher order effects can be quite tedious and hence the stability analysis is carried out by conducting the

experiments with Q_F as a parameter. The result is plotted as shown in Figure 3.6 for $\omega_1 = \omega_n = 100\pi$ rad/s. The stable and unstable regions are marked and the designer has to keep this in mind while choosing G in relation to Q_F or vice-versa. Further, the

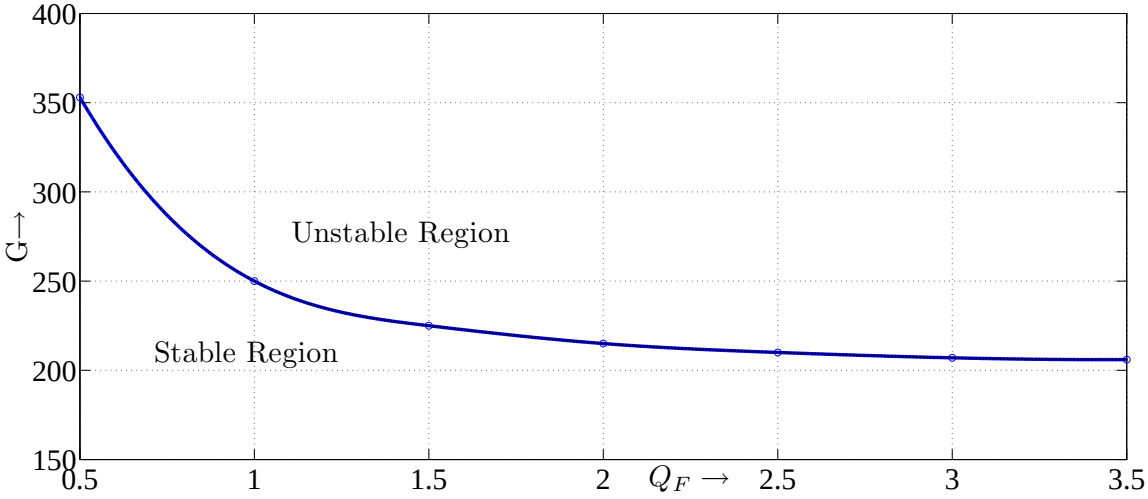


Figure 3.6: Limits of stability with Q_F as a parameter

system is stable only for a range of ω_1 below the nominal value (ω_n). Note that, if ω_1 is decreased to such an extent as to make the attenuation of the $2\omega_1$ component in (3.7) negligible, the effective loop gain increases by the same process as explained earlier. However, this does not apply when ω_1 is increased beyond ω_n. In such situations, the $2\omega_1$ component is still attenuated sufficiently in relation to ω_1 and hence its effect is neglected. However, higher settling times and suboptimal responses are observed due to the fact that $|\cos(\phi_1)| < 1$ and $G_F < Q_F$ in (3.8). Therefore the proposed VLL has a lower limit on ω_1 (for given G and Q_F) due to stability restrictions, whereas the upper limit is dictated by the settling time requirements.

3.2.7 Design considerations

In this section, a few thumb-rules are presented for designing the proposed VLL. The designer may arrive at a more optimized VLL by fine-tuning the system through computer simulations after following these general rules.

PLL Design

The PLL performance can be optimized by well established techniques [Egan(2007)]. Note that the proposed VLL output will be of the same frequency and phase as that of

the output by the PLL. Therefore it is necessary to design the PLL with a free-running frequency close to the fundamental frequency component in the input.

Choice of G

A properly designed system would be able to closely follow changes in frequency and amplitude of the fundamental input. In other words, the phase-lag in amplitude must be as small as possible. Therefore from (3.23), it follows that the denominator $\omega_1(G^2{Q_F}^2 - 2\omega_m^2)$ must be as large as possible. This may be achieved by utilizing a very large gain G. Since θ is small for such a system, we use the approximation that $\tan^{-1}\theta = \theta$. Therefore (3.23) now becomes,

$$\theta \approx \frac{2Q_F\omega_m}{\omega_1}\left(\frac{\omega_1^2 - \omega_m^2}{G^2{Q_F}^2 - 2\omega_m^2}\right). \tag{3.25}$$

Further note that $\omega_1 \gg \omega_m$. Also, since G is chosen to be large enough to make the denominator of (3.25) high,

$$\theta \approx \frac{2\omega_1\omega_m}{G^2Q_F}. \tag{3.26}$$

Using (3.26) the sensitivity of θ with respect to G is as follows,

$$\frac{\partial\theta}{\partial G} = \frac{-4\omega_1\omega_m}{Q_F}\frac{1}{G^3}. \tag{3.27}$$

From (3.27), it follows that the sensitivity of the phase-lag to variations in G is low when G is large. Therefore in practical systems, it is advisable to include a high gain in the loop for quicker response, small phase-lag and to increase the overall robustness of the system.

Choice of Q_F

Using (3.26), the sensitivity of θ with respect to variations in Q_F is obtained as follows,

$$\frac{\partial\theta}{\partial Q_F} = \frac{-2\omega_1\omega_m}{G^2}\frac{1}{{Q_F}^2}. \tag{3.28}$$

From (3.28) one may conclude that sensitivity of phase-lag to variations in Q_F is low when Q_F is high and that a high value of G already ensures low sensitivity. However,

it is not advisable to have a very large Q_F since the system becomes highly oscillatory and settling-time increases. Also, a higher Q_F translates to a lower range of ω_1 over which $\phi_1 \approx -180^\circ$ (criterion for optimal performance). Therefore the quality factor of the SOLF has a dominant effect on the settling time of the system and also on the dynamic range of input frequency.

3.2.8 Simulation results

Extensive simulation studies were conducted on the proposed VLL using MATLAB® and Simulink®. Various features of the system with $\omega_n = 100\pi$ rad/s, $Q_F = 2$, and $G = 180$ were explored for different inputs.

Response to Step Input

The simulation results of the VLL and its LTI model for a step change of +0.5 in the fundamental input amplitude, $C_1(t)$ at $t = 0.2$ s are shown in Figure 3.7 and Figure 3.8. The purpose of this test is to estimate the settling time of the system and to compare it with the response from the LTI model. The input for the proposed VLL is,

$$x_I(t) = 0.5[u(t) + u(t - 0.2)]\sin(100\pi t). \tag{3.29}$$

Hence the input to the LTI model is $C_1(t)$ which is,

$$C_1(t) = 0.5[u(t) + u(t - 0.2)]. \tag{3.30}$$

It is observed that the output settles to steady-state within 2% error in about 60 ms. As observed in Figure 3.8, the settling times are matching for the system and its LTI model.

Response to Input Amplitude Modulation

The VLL performance was also investigated for an amplitude modulated sine-wave as given in (3.18) with $C_0 = 1$, $C_m = 0.2$ and $\omega_m = 4\pi$ rad/s. Thus with, $C_1(t) \triangleq [1 + 0.2\sin(4\pi t)]$ and

$$x_I(t) = C_1(t)\sin(100\pi t) \tag{3.31}$$

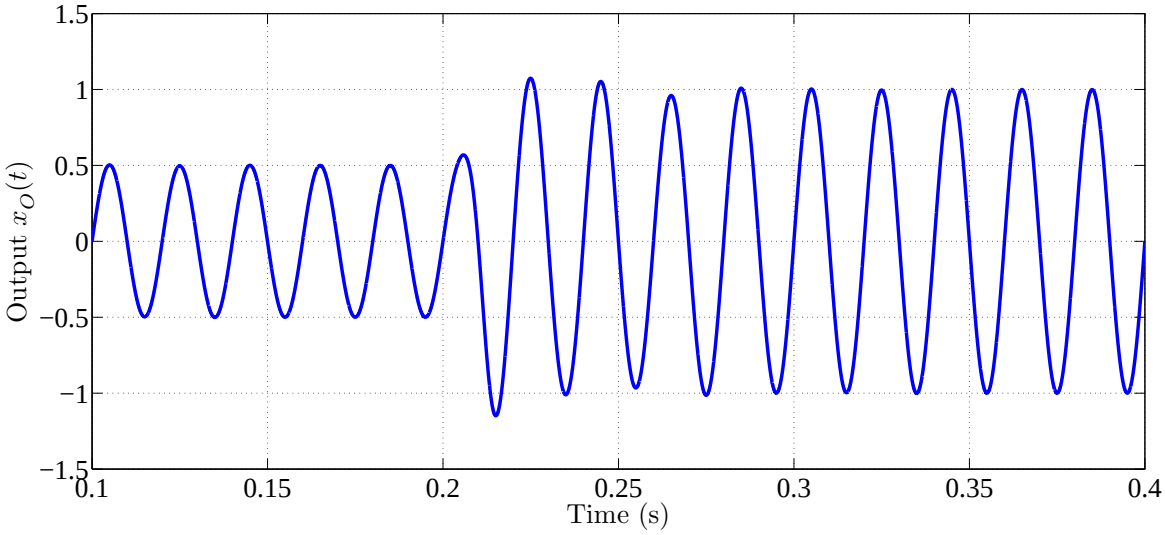


Figure 3.7: Simulation result of $x_O(t)$ of the actual system to a step change in the amplitude of $C_1(t)$

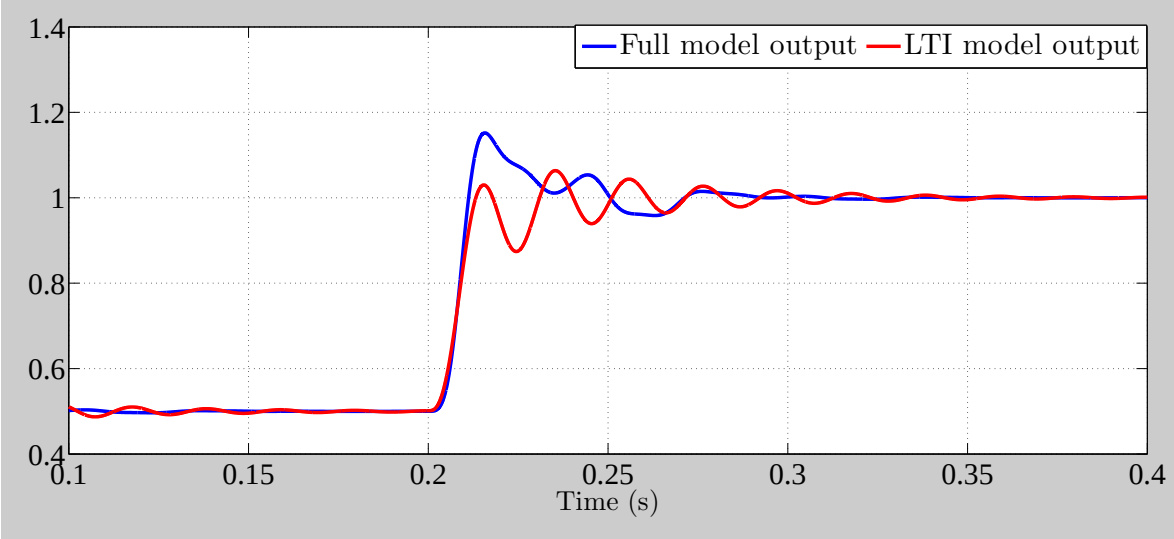


Figure 3.8: Comparison of $a_O(t)$ of the LTI model response and that of the actual system to a step change in the amplitude of $C_1(t)$

the Figure 3.9 displays an area zoomed to around one and a half cycle of the modulating signal in order to clearly show the negligible phase lag in $a_O(t)$ and also the exactness of the LTI model. It is useful to remember that $a_O(t)$ is the instantaneous amplitude of the output, to meaningfully interpret the results. The Discrete Fourier Series (DFS) analysis of $a_O(t)$ output from the VLL revealed the presence of 48 Hz and 52 Hz components as predicted in Section 3.2.4.

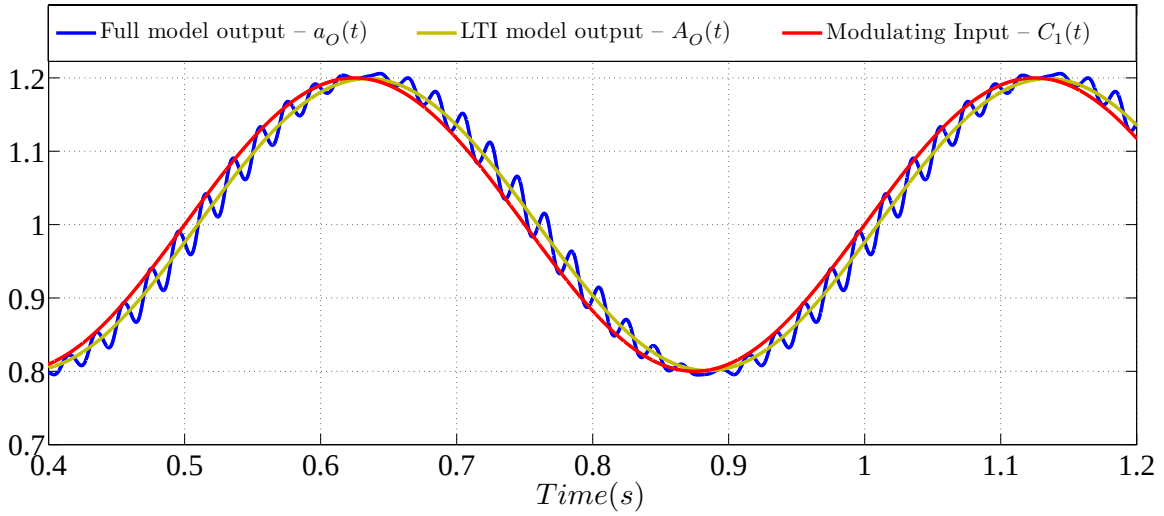


Figure 3.9: Comparison of $a_O(t)$ of the LTI model response and actual system output amplitude to an input whose amplitude is modulated

Frequency sweep

The scheme gives satisfactory performance under conditions of varying supply frequency. It is tested for supply frequency variation in the range of 30 Hz to 60 Hz at a rate of 5 Hz/s. The frequency is maintained constant at 50 Hz until 1 s. It is then decreased to 30 Hz over a duration of 4 s and then ramped-up to 60 Hz over a duration of 6 s. It is observed that the scheme tracks the variation in frequency and produces a clean fundamental of amplitude equal to $4/\pi$ – the value corresponding to the fundamental in the input square-wave of unit amplitude. The clippings of the results over a duration of 40 ms captured at different instants of time during the variation of frequency are as shown in Figure 3.10.

Harmonic Attenuation

Studies on distortion of the output in the presence of harmonics in the input signal are shown in Figure 3.11, Figure 3.12, and Figure 3.13. The applied input is a square wave of unit amplitude and frequency 50 Hz. Figure 3.11 and Figure 3.12 show the VLL outputs which are the extracted fundamental component and harmonics of the square wave, respectively.

A DFS of x_I and x_O are taken and the results are presented in Figure 3.13. It can be observed that the amplitude of fundamental components of x_I and x_O are perfectly matched and that the harmonic amplitudes in x_O roll-off at a rate approximately equal

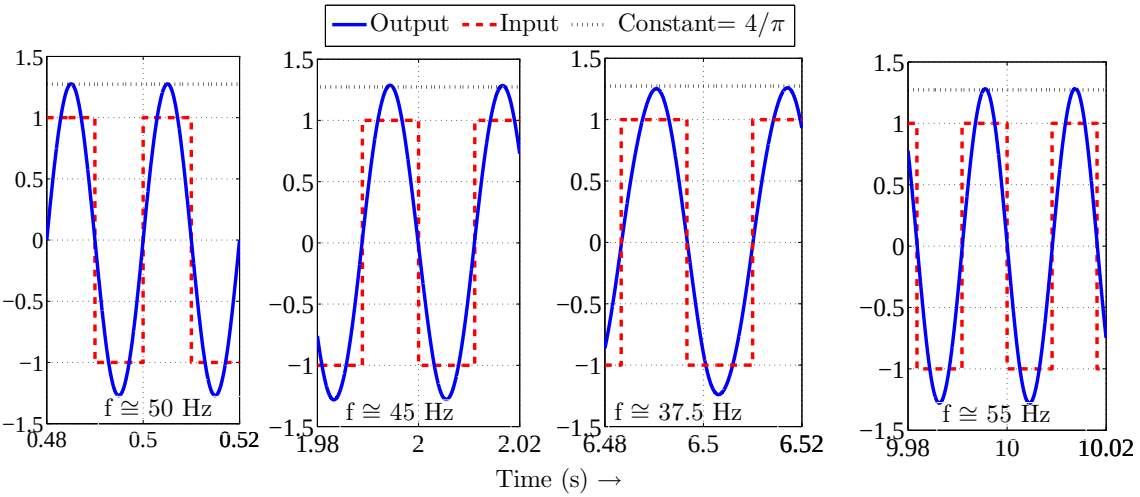


Figure 3.10: Result of frequency sweep at a rate of 5 Hz/s at different instants during the sweep duration

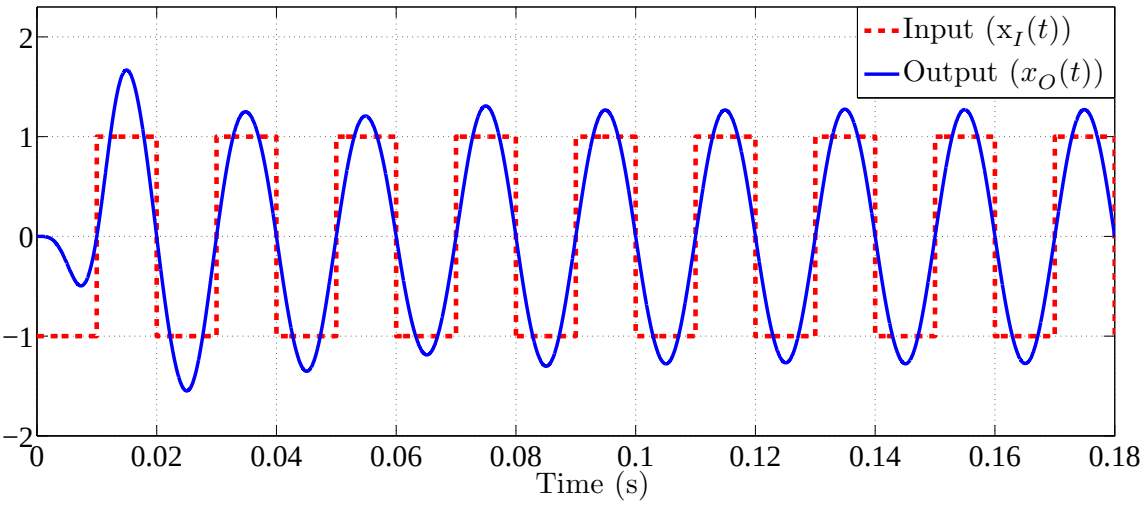


Figure 3.11: Output for square wave input

to 80 dB/dec. However, the VLL does introduce a small amount of distortion at the output which is evident by the presence of even harmonic components in the DFS plot, despite their absence in the input.

Noise Rejection

Simulation studies on the noise rejection capabilities of the VLL were conducted. Figure 3.14 shows the input, which is a sine wave of 100π rad/s with band-limited white-noise, and the corresponding output. For the input with a signal-to-noise-and-distortion ratio (SNDR) of 7 dB, the output SNDR was observed to be at 26.3 dB.

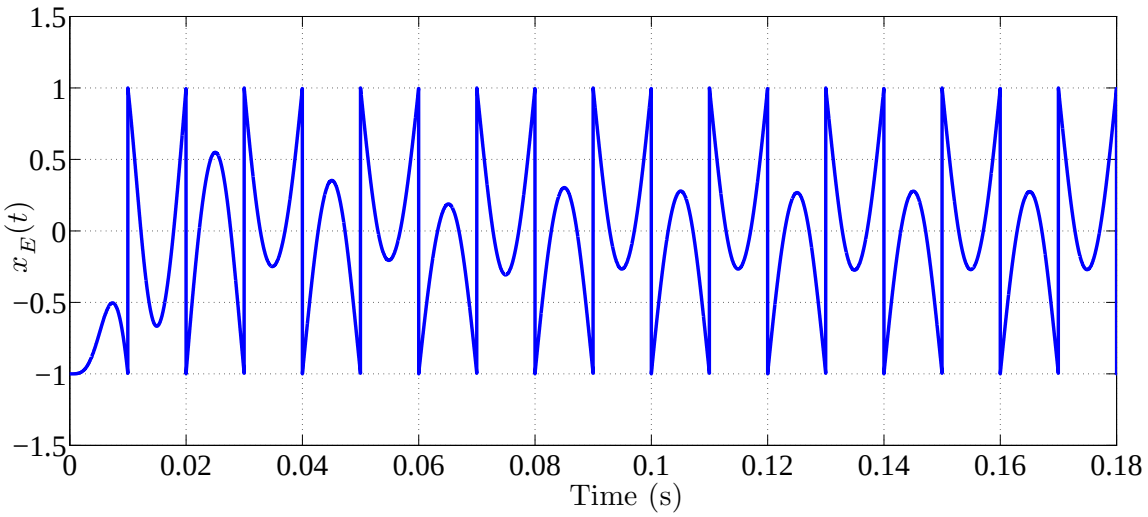


Figure 3.12: Harmonic output for square wave input

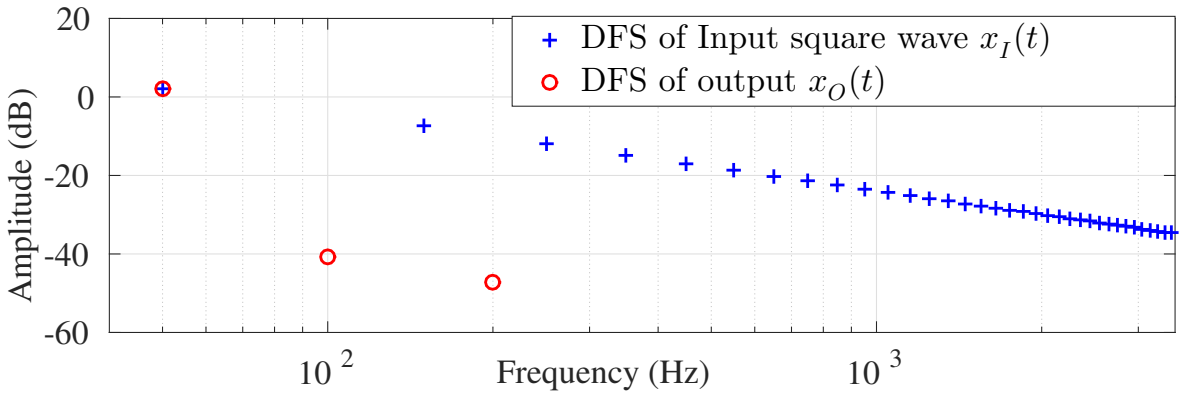


Figure 3.13: Frequency spectrum analysis for a square wave input

Response to Square-wave Input: Alternate Parameter-Set

The VLL is tested for a better set of parameter values, G=180 and Q=0.95 with ω_n=100π rad/s. The response is as shown in Figure 3.15. It is observed that the output settles to steady-state within 2% error in about 30 ms.

3.2.9 Conclusions

A novel scheme for obtaining synchronized selective-frequency amplitude-locking on distorted signals is presented. An intuitive explanation of the working of the loop is presented. A comprehensive LTI model for the system is developed to facilitate the design process. It is found that the model truly represents the actual system as far as the settling time, steady-state response, and modulation properties are concerned. However the stability behaviour is not captured in the LTI model for the obvious reason

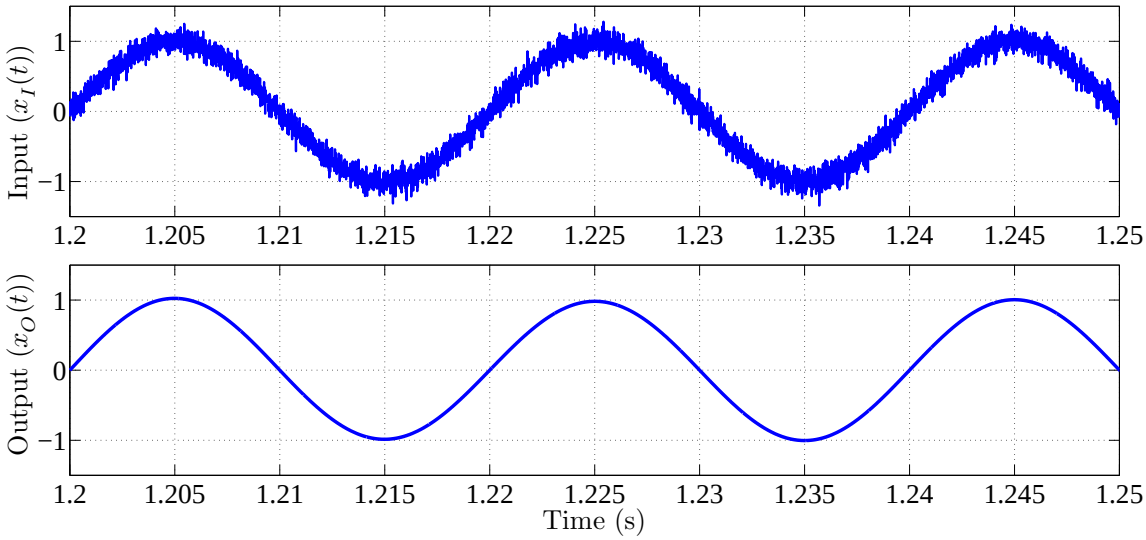


Figure 3.14: Performance under noisy conditions

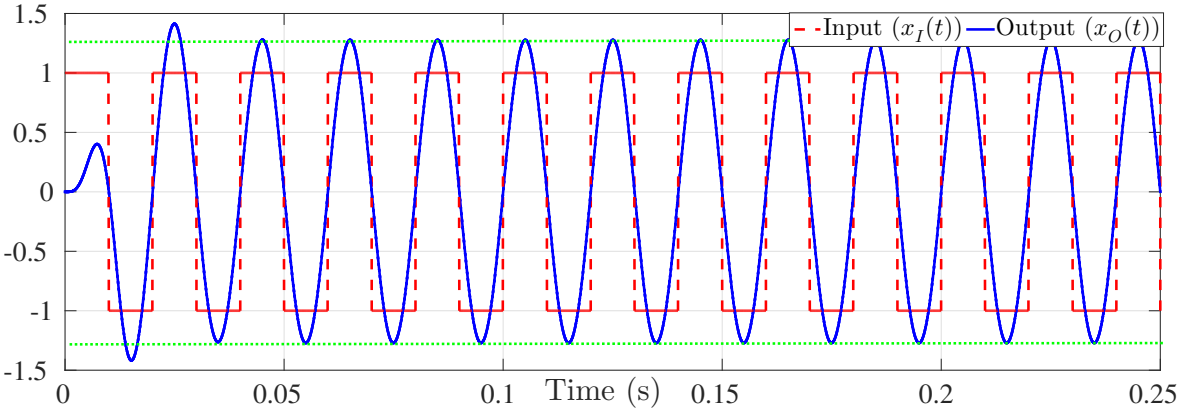


Figure 3.15: Simulation result of $x_O(t)$ of the actual system to a Square-wave Input applied at $t = 0$ s.

that the actual scheme is time-variant. Hence stability margin is determined by means of experiment. Clear explanations are given for the selection of G and Q_F. Performance claims are supported by simulation results. The features of the proposed scheme are as follows:

- it has features similar to a PLL.
- the performance can be optimized by appropriate choice of G and Q_F.
- the transient response is better (≈ 30 ms), has excellent insensitivity to harmonics, and noise rejection.
- the amplitude tracking is determined by the product of depth of modulation and the frequency of modulation.

- the scheme is a time-variant system.

It can find applications in:

- synchronous separation of the fundamental and harmonics in a distorted periodic waveform.
- amplitude and frequency tracking
- noise rejection.
- amplitude demodulation/peak detection.

3.3 Algorithm-2: Pettigrew's Adaptation

In this section another algorithm for the extraction of harmonics is presented. It is obtained by an adaptation of the Pettigrew's [Pettigrew(1994)] scheme using its demodulation property. The above adaptation involves: developing the mathematical framework to substantiate the extension and suggesting modifications to improve the performance parameters. A second-order-low-pass filter (SOLF) pre-tuned to a cut-off frequency (ω_c) with a flat frequency response has been used for improving the performance. Here a brief review of the analysis presented by Moir [Moir(1995)] is given in order to understand the operation of the scheme and to place the ensuing discussion in the proper perspective. The adaptation of the scheme to extract the fundamental is explained with the necessary mathematical proof. The design parameters influencing the performance parameters are identified. Design considerations are discussed and empirical rules for the design are presented. Simulation results are presented to validate the claims on the performance parameters of the algorithm.

3.3.1 Brief description of Pettigrew's ALL

The amplitude-locked loop (ALL) proposed by Pettigrew [Pettigrew(1994)] for amplitude demodulation, is shown in Figure 3.16. T. J. Moir [Moir(1995)] presented an analysis of the circuit. In the circuit shown in Figure 3.16, the output of the multiplier-M1 is,

$$y(t) = u^C(t)x_I(t). \tag{3.32}$$

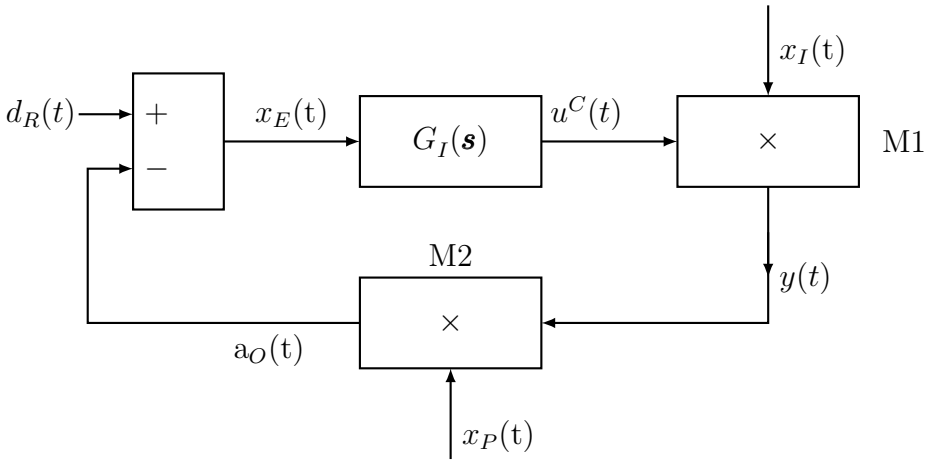


Figure 3.16: Block diagram of Pettigrew's ALL

Consider an input,

$$x_I(t) = c(t)\cos(\omega_1 t + \phi_i) \tag{3.33}$$

where $c(t)$ is the modulating signal and $\cos(\omega_1 t + \phi_i)$ being the carrier. For the purpose of analysis $c(t)$ and ϕ_i are considered initially as constants with $c(t) = C_1^0$ and ϕ_i^0, but in practice they may be time varying. It is assumed that $c(t) \neq 0$. The signal $x_P(t)$ is given by,

$$x_P(t) = B_P\cos(\omega_1 t + \phi_p) \tag{3.34}$$

obtained as the output derived from a PLL tuned to the carrier frequency ω_1. Let the output of the multiplier-M2 be,

$$a_O(t) = x_P(t)y(t). \tag{3.35}$$

When the ALL is 'in lock' the error signal $x_E(t)$, in the Laplace's domain is,

$$\begin{aligned} X_E(\boldsymbol{s}) &= D_R(\boldsymbol{s}) - A_O(\boldsymbol{s}) && (3.36)\\ &= D_R(\boldsymbol{s}) - X_P(\boldsymbol{s}) * Y(\boldsymbol{s}) && (3.37) \end{aligned}$$

where $*$ denotes convolution. With the approximation of ignoring $2\omega_1$ terms in $x_E(t)$, and considering $G_I(\boldsymbol{s}) = \dfrac{G}{\boldsymbol{s}}$ and $B_P = 1$ it is shown by Moir [Moir(1995)] that,

$$U^C(\boldsymbol{s}) = \frac{G}{\boldsymbol{s} + C_1^0 \dfrac{G}{2}\cos(\phi_p - \phi_i^0)} D_R(\boldsymbol{s}). \tag{3.38}$$

With step input of magnitude D_R for $d_R(t)$ and with $x_E(t)$ converging to zero in steady state, the response is,

$$u^C(t) = \frac{2D_R}{C_1^0 \cos(\phi_p - \phi_i^0)}. \tag{3.39}$$

If $\phi_i^0 = \phi_p$, is ensured, then,

$$u^C(t) = \frac{2D_R}{C_1^0} \tag{3.40}$$

i.e., $u^C(t)$ becomes the scaled inverse of the amplitude C_1^0 – the modulating signal of the input $x_I(t)$. Then from (3.32) and (3.33),

$$y(t) = 2D_R \cos(\omega_1 t + \phi_i^0) \tag{3.41}$$

which is a scaled version of the carrier $\cos(\omega_1 t + \phi_i^0)$, where $2D_R$ is the scalar, as decided by the amplitude reference $d_R(t) = D_R$. Note that $y(t)$ is devoid of the modulating signal C_1^0, hence is amplitude demodulated version of $x_I(t)$. Equation (3.41) shows that the system has the ability to remove the modulating signal leaving only the carrier. Then $u^C(t)$ becomes the scaled inverse of the amplitude of the modulating signal of the input. Although the analysis is only true for constant modulating signal C_1^0, it is intuitive that for the time-varying case, $c(t)$ with the frequency and depth of modulation within the tracking range,

$$u^C(t) = \frac{2D_R}{c(t)} \tag{3.42}$$

and $y(t)$ is still given by (3.41), and with $D_R = 0.5$, $y(t) = \cos(\omega_1 t + \phi_i^0)$ – the carrier devoid of the modulating signal $c(t)$.

3.3.2 Adaptation of Pettigrew's ALL for Fundamental/ harmonics extraction – Basic operation

Consider a signal input $x_I(t)$, a periodic waveform with a constant component C_O,

$$x_I(t) \;=\; C_O + \sum_{h=1}^{\infty} C_h \cos(h\omega_1 t + \phi_h). \tag{3.43}$$

The output of the PLL (pre-tuned to a free-running frequency of ω_1) which is purely sinusoidal and in-phase with the fundamental component of $x_I(t)$ is,

$$x_P(t) \;=\; \cos(\omega_1 t + \phi_1) \tag{3.44}$$

where $B_P = 1$ is considered. Now each term in (3.43), can be considered as the product of a modulated signal determined by the coefficient C_h and a carrier determined by ω_h. If there was only fundamental at ω_1 and with PLL tuned to ω_1, it is clear from (3.39) and (3.40) that C_1 can be obtained by the reciprocal of $u^C(t)$ and appropriately scaled due to the commanded amplitude D_R factor. It is also clear from (3.40) that D_R shall be chosen as 0.5. It is also true that $a_O(t)$, which is obtained as a multiplication of two in-phase sine-waves ($\phi_i = \phi_p$) of like frequency contains a constant, equal to half the product of each of the amplitudes. Hence in this scheme D_R shall be set as 0.5. It should be noted that $a_O(t)$ also contains $2\omega_1$ components, which is attenuated by the integrator in the $G_I(\boldsymbol{s})$. Additional attenuation can be achieved, as will be explained shortly.

Thus the product of $\dfrac{1}{u^C(t)} \triangleq c_O(t)$ and $x_P(t)$ recovers the input signal for this case of single frequency input. Therefore,

$$x_O(t) \;=\; c_O(t) x_P(t). \tag{3.45}$$

It should be noted that, under the steady-state, the fundamental amplitude of $y(t)$ shall be unity, until then the corrections will continue.

3.3.3 Principle of working for input with constant and harmonics

It should be noted that any component in $x_I(t)$ other than ω_1, including constant, will not produce a constant in $a_O(t)$, according to (3.35). Thus it will not affect the transient response of $u^C(t)$ and hence $c_O(t)$, as it is decided by the rate of charging the integrator which is determined by the constant component in $x_E(t)$. So, all such terms in (3.43), will not affect the transient response. However they have a direct bearing on the steady-state response of $c_O(t)$, and show up as ripple in it. However the steady-state and transient performances can be improved by inserting a low-pass filter $F(\boldsymbol{s})$, as shown in Figure 3.17. The SOLF, $F(\boldsymbol{s})$, has a similar structure as given

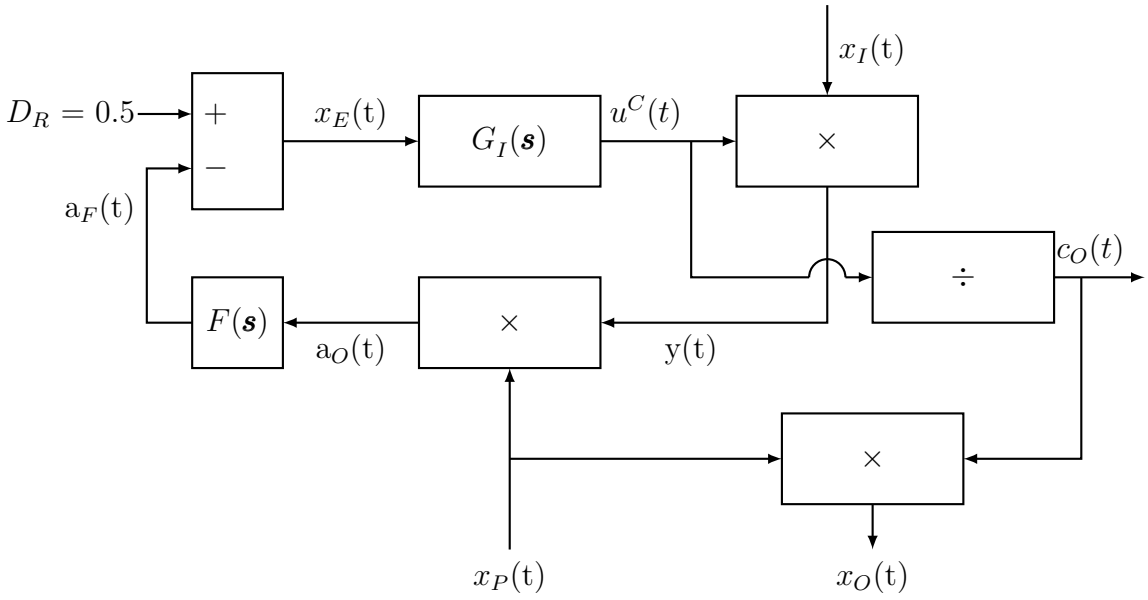


Figure 3.17: Block diagram showing the adaptation

in (3.1) and the characteristics shown in Figure 3.2. Ideally $F(\boldsymbol{s})$ should pass only the constant, blocking the fundamental (which may creep-in due to the presence of any constant in $x_I(t)$) and all the higher order harmonics. Hence the cut-off frequency (ω_c) should be considerably less than ω_1, and Q_F is relatively smaller. Then there will be faster attenuation of the harmonics in the loop and the settling-time improves along with improvements in the other performance parameters.

3.3.4 Small signal analysis

Now if we consider that the system is working under normal conditions in steady-state. The input $x_I(t)$ being of single frequency sinusoidal with constant amplitude C_1^0. Now our interest is to determine the effect of variation of $C_1(t)$ on the system operation and performance and hence to obtain a relation between the system parameters and the performance parameters. Under such a condition D_R (=0.5) and x_P are constants. Since our interest is only to see the effect of variation of $C_1(t)$, the system can be represented as shown in Figure 3.18. The scheme is a non-linear system and hence

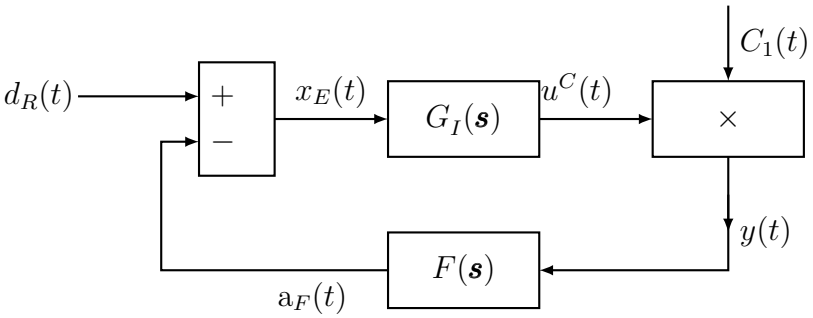


Figure 3.18: Pettigrew's ALL under perturbation on $C_1(t)$

the complete analysis is not considered here. It is not possible to obtain expressions/ formulae relating the parameters of the system (G, Q_F, ω_c) to the design parameters. However under the conditions of small signal variations on the amplitude of the fundamental $C_1(t)$ in $x_I(t)$ a linear model is attempted. Consider for a moment that the system is working under steady-state. The input $D_R = 0.5$, $x_P(t)$ is steady. Now let there be a small change in the amplitude of $C_1(t)$ from C_1^0, by an amount say $\Delta c_1(t)$. Now this change will set-up a new transient. The $a_O(t)$ will change, which results in a change in the error $x_E(t)$, driving a change in $u^C(t)$ until it settles to a value equal to $\dfrac{1}{C_1^0 + \Delta c_1}$. Under such a condition, the process of settling of $u^C(t) = u^{C^0} + \Delta u^C(t)$, to a new steady-state can be captured in the system shown in Figure 3.18.

The detailed analysis is given in Appendix E.1. If the disturbance input is $\Delta c_1(t) = \Delta c_1 \sin(\omega_m t)$, where Δc_1 is the amplitude of the sinusoidal disturbance with frequency ω_m, then the steady-state response is obtained as explained in Figure 3.5, as follows,

$$\Delta u^C(t) \;=\; \frac{-G u^{C^0} \omega_c^2}{|\boldsymbol{s}^3 + \frac{\omega_c}{Q_F}\boldsymbol{s}^2 + \omega_c^2 \boldsymbol{s} + G C_1^0 \omega_c^2|_{\boldsymbol{s}=j\omega_m}} \Delta c_1 \sin(\omega_m t - \phi_m) \qquad (3.46)$$

where ϕ_m is the phase-shift introduced by the denominator term $D(\boldsymbol{s}) = |\boldsymbol{s}^3 + \frac{\omega_c}{Q_F}\boldsymbol{s}^2 + \omega_c^2\boldsymbol{s} + GC_1^0\omega_c^2|$ at $\boldsymbol{s} = j\omega_m$. It must be noted that the response depends on the initial condition C_1^0 in addition to the parameters of the system. The magnitude and phase of $D(\boldsymbol{s})$, are given by,

$$|D(\boldsymbol{s})| = \sqrt{(GC_1^0\omega_c^2 - \frac{\omega_c}{Q_F}\omega_m^2)^2 + (\omega_c^2\omega_m - \omega_m^3)^2} \tag{3.47}$$

and

$$\phi_m = \tan^{-1}\left(\frac{\omega_c^2\omega_m - \omega_m^3}{GC_1^0\omega_c^2 - \frac{\omega_c}{Q_F}\omega_m^2}\right) \tag{3.48}$$

respectively.

Block diagram of the Small Signal Analysis

The analysis presented in Appendix E.1 further leads to an input-output relation between the small signal disturbance input ($\Delta c_1(t)$) and the corresponding response ($\Delta u^C(t)$). From (E.7), we can write it in the form,

$$\frac{\Delta u^C(t)}{\Delta c_1(t)} = \frac{G_P(\boldsymbol{s})}{1 + G_P(\boldsymbol{s})H_P(\boldsymbol{s})} \tag{3.49}$$

a feedback system, where $G_P(\boldsymbol{s}) = -G_I(\boldsymbol{s})F(\boldsymbol{s})u^{C^0}$ and a feedback gain, $H_P(\boldsymbol{s}) = -\left(\frac{C_1^0}{u^{C^0}}\right)$. It can be represented as shown in Figure 3.19.

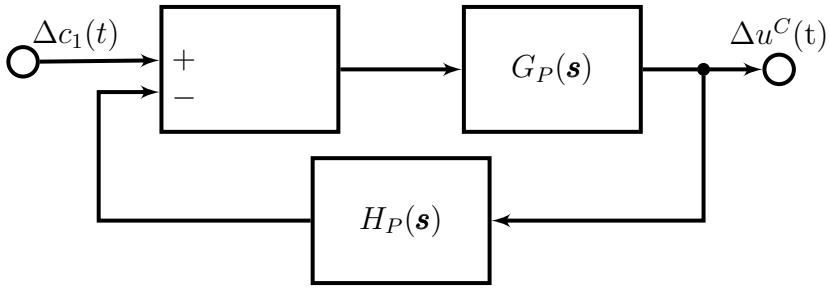


Figure 3.19: Small Signal equivalent of the proposed ALL

3.3.5 Design considerations

It is to be noted that the design parameters are: gain G and, cut-off frequency ω_c and Q_F for the filter $F(\boldsymbol{s})$. The performance parameters are: settling-time, harmonic

rejection, amplitude modulation, and noise rejection. Extensive simulation study is done and experiments are conducted to arrive at a good set of values for the design parameters. It should also be noted that there is a need to limit the lower level for $u^C(t)$, during the start-up to avoid division by zero. It can create the problem and also the amplitude $c_O(t)$ of the fundamental in $x_O(t)$, will start building from unrealistically large values, making the settling time unnecessarily larger. This limit can be chosen with the knowledge of the practical range of amplitude for the fundamental under the given circumstances.

PLL Design

This scheme works in association of a PLL. Note that the proposed ALL output will be of the same frequency as that output by the PLL. Therefore it is necessary to design the PLL with a free-running frequency close to the fundamental frequency component in the input. The PLL performance can be optimized by well established techniques.

Design of the circuit

The function of the low-pass filter is to attenuate the harmonics generated in $a_O(t)$ with the presence of higher order harmonics in $x_I(t)$ and as well as the second harmonic produced due to the interaction of the fundamental in $x_I(t)$ with $x_P(t)$. And it is also necessary that it does it as fast as possible. Hence it is found through experiment that a flat second-order-low-pass filter is a good choice and a suitable cut-off frequency of ω_c is selected. The transfer function of the low-pass filter is repeated here for reference and as given below:

$$F(\boldsymbol{s}) = \frac{1}{\dfrac{\boldsymbol{s}^2}{\omega_c^2} + \dfrac{\boldsymbol{s}}{Q_F\omega_c} + 1} \tag{3.50}$$

where ω_c is the cut-off frequency in rad/s. It is observed while tuning that an increase in gain G (for a fixed ω_c), results in an increase in steady-state error and a decrease in settling time. A similar relation holds good for a change in ω_c (for a fixed G). This makes tuning of the algorithm very easy, however the relations are not linear.

3.3.6 Simulation results

Extensive simulation studies were conducted on this scheme using MATLAB® and Simulink®. A simulation step-size of 10 μs is chosen. Various features of the system with $\omega_c = 70\pi$ rad/s, $Q_F = 0.85$, and $G = 118$ were explored for different inputs. A lower limit of 0.2 for $u^C(t)$ ($\equiv 5$ for C_1) was set. The results are presented in what follows.

Response to Step Input: The amplitude C_1

A square wave input of unit amplitude with a frequency of $\omega_1 = 100\pi$ rad/s, is applied to the circuit at $t = 0.1$ s. The settling-time indicated by the signals $u^C(t)$ and $c(t)$ is captured in the Figure 3.20. It can be observed that the system settles to final value within around 1.5 cycles, which much better than the existing schemes.

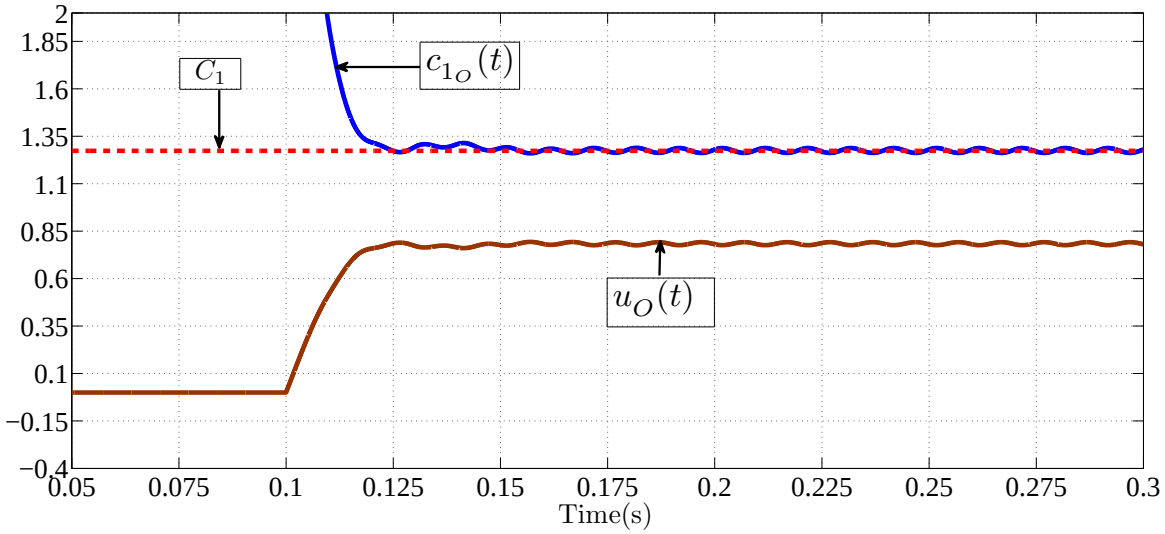


Figure 3.20: Step response showing settling time for a square wave input

Response to Step Input: The fundamental $x_1(t)$

The input square wave and the fundamental extracted signals are as shown in Figure 3.21. The expected fundamental amplitude $\left(\pm\frac{4}{\pi}\right)$ is also plotted to show the settling-time. It can be clearly seen that the fundamental settles within 1.5 cycles.

Response to Step Input: The Harmonics in $x_I(t)$

The harmonics extracted from the square wave is shown in Figure 3.22.

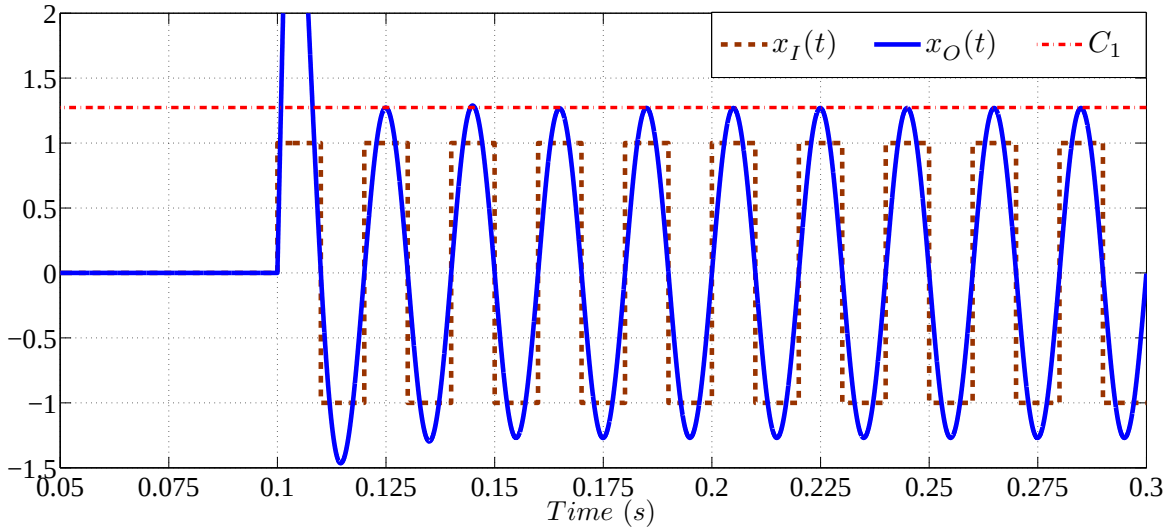


Figure 3.21: Output for a square wave input

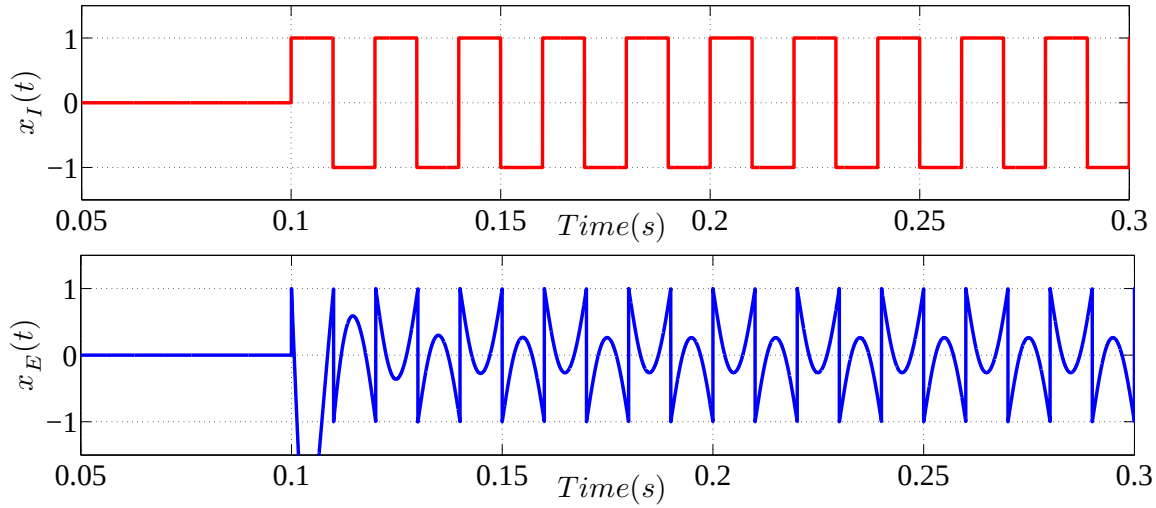


Figure 3.22: Harmonics extracted from a square wave input

Harmonics Attenuation for square wave input

A Discrete Fourier Series (DFS) analysis is conducted on the input square wave $x_I(t)$ and the output $x_O(t)$. The number of samples are chosen in such a way that the frequency bins are placed at 50 Hz intervals. The spectrum obtained is as shown in Figure 3.23. It can be observed that there is a drastic reduction in the harmonics in the output. This is a result of systematic tuning of the set of design parameters: G, Q_F, and ω_c.

Response to Input Amplitude Modulation

The performance of the scheme is verified for tracking a slow varying amplitude, as might happen in power system. This feature is also important for amplitude demodu-

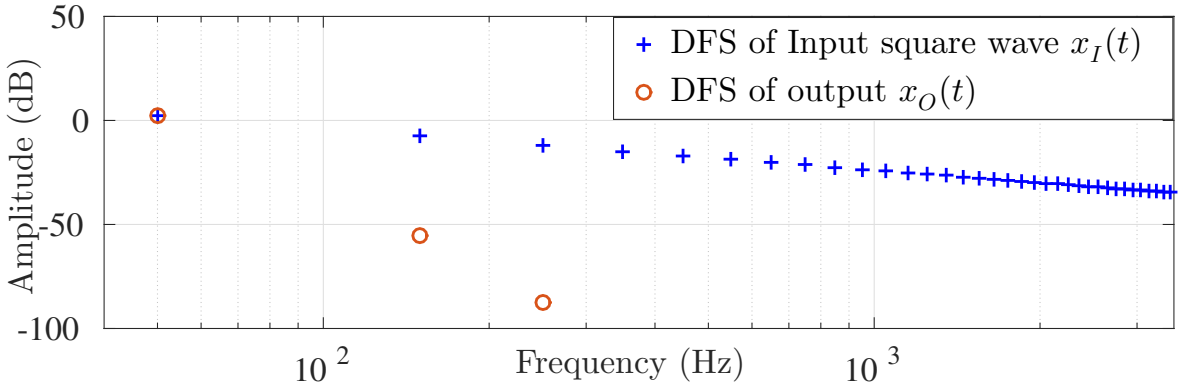


Figure 3.23: Frequency spectrum analysis for a square wave input

lation. The input considered is:

$$x_I(t) = C_1(t)\sin(100\pi t) \tag{3.51}$$

where $C_1(t) = [1 + 0.2\sin(4\pi t)]$. Figure 3.24 displays an area zoomed to around one cycle of the modulating signal in order to clearly show the negligible phase lag in input modulating signal and the output.

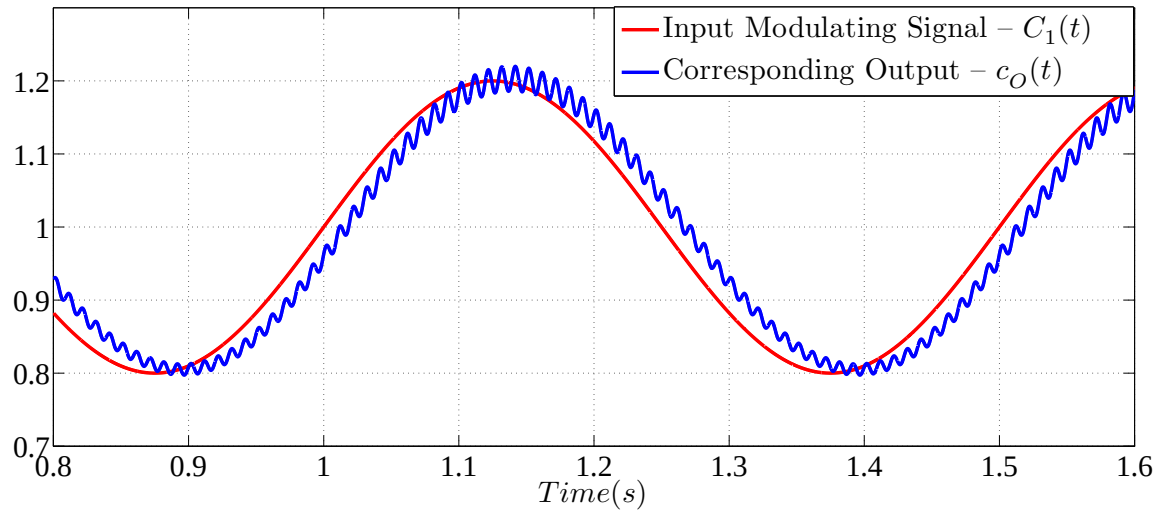


Figure 3.24: Output amplitude to an input whose amplitude is modulated

Response to Input with Noise

Figure 3.25 shows the input, which is a sine wave of 100π rad/s with band-limited white noise, and the corresponding output. For an input with signal-to-noise-and-distortion ratio (SNDR) of 6 dB, the SNDR of the output was observed to be 36.3 dB. It can be

clearly seen that the noise is severely snubbed in the output. It works very well under noisy environments.

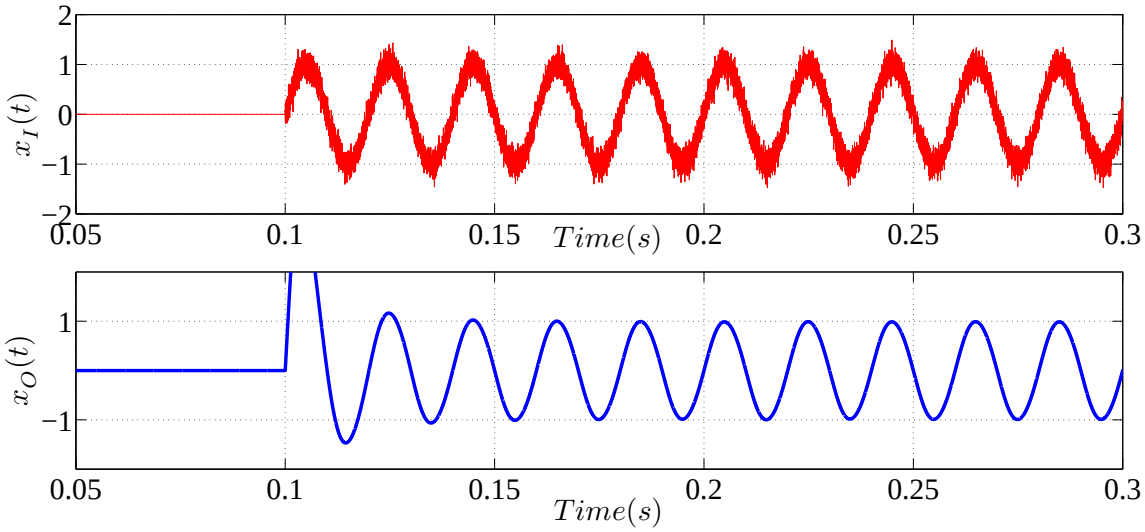


Figure 3.25: Output amplitude to an input whose amplitude is mixed with noise

3.3.7 Conclusions

It is proposed to validate the real-time implementation of a novel amplitude-locked loop. The scheme, an adaptation of the Pettigrew's ALL, suitable for extracting the selective frequency component in a distorted signal is considered. An intuitive explanation for the working of the scheme is presented. The design parameters – G, ω_c, and Q_F are identified. A procedure for the selection of these parameters is explained. The features of the proposed scheme are as follows: it has features similar to a PLL, the performance can be optimized by appropriate choice of G, ω_c, and Q_F, the transient response is good, and has low sensitivity to harmonics, and noise. It can find applications in: synchronous separation of fundamental and harmonics in a distorted periodic waveform (single-phase or three-phase), amplitude and frequency tracking, noise rejection, and amplitude demodulation/peak detection.

It is found that the output settles to within 1.5% error as early as $\cong$ 1.5 cycles and it remains in locked in amplitude and phase with the input, thereafter, for small variations. The DFS of the output showed very little traces of harmonics. The noise rejection property of the algorithm is tested with a noisy input signal having an SNDR of 6 dB. It is found that the SNDR on the output is 36.3 dB, proving its applicability in a noisy environment. The modulation performance is tested using a modulation

frequency of 2 Hz and relative depth of modulation of 0.2 units. It is found that, the output follows the input both in magnitude and phase very closely.

3.4 Real-time simulation – Introduction

In the last two sections the simulation results for the two algorithms proposed is presented. Simulations were run with a step-size of 10 μs and in the off-line mode. When implemented on a DSP or an FPGA the computations will be done at a higher sampling time and the processor word length effects can be significant. It is also necessary to be able to complete the necessary calculations within the step time. In order to ascertain their implementation on a digital processing hardware, they were tested on a real-time platform. In this section the hardware setup used for the experiment is explained and the test results from both the algorithms are presented.

3.4.1 Real-time emulation platform

The algorithm is to be tested on a real-time hardware-emulation platform – a dSPACE Modular system (configured around the DS1006 processor board) [dSPACE(1999)]. While such a system can be useful in different applications, here it is used for the purpose of development, testing, and validation of an algorithm for real-time implementation. This process becomes important, in cases like the algorithm under consideration where the kind of non-linearity does not permit an analytical solution and numerical techniques are the only alternatives. After testing and fine-tuning the parameters, in actual practice the algorithm may be implemented on any other hardware, like a microprocessor (μP), micro-controller (μC), Digital Signal Processor (DSP), or Digital Signal Controllers (DSC), or Field Programmable Gate Arrays (FPGA). Any system to be implemented in real-time has to be first modeled and simulated in a higher level language, like C/C^{++}/ Simulink®. This code or program is then cross-compiled into the object code of the processor housed in the hardware-emulation platform. It consists of three

main components – a hardware, a code development assistant, and a Graphical User Interface (GUI). The hardware, in general consists of a high-speed processor, analog- and digital input-output (I/O) devices or interfaces, and a communication arrangement between the host computer and the platform. The code development assistant is basically a cross-compiler. It provides facility for developing the model in a higher level language and cross-compiling it to the machine code corresponding to the processor in the hardware unit. The GUI helps in downloading the code thus developed onto the processor, controlling the execution of the program, and also serves as a virtual instrumentation (VI) unit. Each of these units are explained briefly in the following with reference to the system used in this case.

Hardware section – the DS1006 based Modular System

The dSPACE Modular System [dSPACE(1999)] suitable for real-time computations consists of – a DS1006-Processor board for calculating processing-intensive real-time models, a set of peripherals: a DS2002 – an analog to digital converter (ADC) board, a DS2101 – a digital to analog converter (DAC) board, a DS4003 – a digital I/O board, and other accessories for interconnections. All these components are housed in the PX10 expansion box with PHS bus, containing ten PCI slots with the provision for interconnection between the cards (using the PHS cable). The communication between the host computer and the Modular System is either through the cross-coupled ethernet cable (viz. RJ45) or the optical link. The DS814 housed in PX10 and the DS817 housed in the personal computer (PC) slot have provisions for this. The system is as shown schematically in Figure 3.26. Each of these components are briefly described in the following with their specifications.

DS1006 – a processor board: The board is built around the AMD Opteron®, x86-compatible 64-bit server, multi-core processor, running at 2.6 GHz. It provides 512 kB L2 cache per core and 6.0 MB shared L3 cache. The DS1006 also has

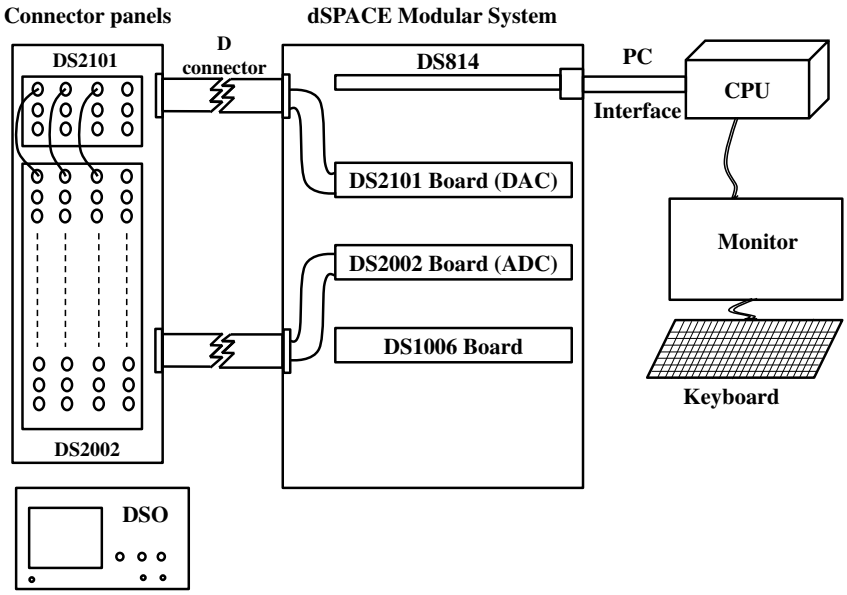


Figure 3.26: Schematic of DS1006-based Modular System

1.0 GB local memory for executing real-time models, 128 MB global memory per core for exchanging data with the host-PC, and 2.0 MB on-board boot flash memory, for automatic, host-independent booting of real-time applications.

DS2002 – a 32 channel ADC, with a conversion time of 3.8 μs for 12 bits conversion and input voltage range of $\pm$5 V or $\pm$10 V. There is also a Connector Panel CP2002 to facilitate connection of signals to the ADC board.

DS2101 – a 5 channel DAC board, with 12 bits resolution, output range $\pm$ 5 V, $\pm$ 10 V, or 0 to +10 V programmable, 3 μs settling time. There is also a Connector Panel CP2101 to facilitate connection of signals to the ADC board.

DS4003 – a 92 line programmable digital I/O board. The inputs and the outputs are TTL compatible.

When dSPACE Modular System is installed, a separate component will be added to the Simulink's Real Time Interface (RTI) Library. This library will contain ports for all the peripherals available on the Modular System. These ports are used for connecting the peripherals with the processor executing the program.

Code development assistant

In the Modular System considered a code-development-assistant system is achieved with a collaboration between the dSPACE and the MathWorks. With this arrangement the system to be studied is modeled in Simulink and tested. Then it is compiled to the machine code, using the *build* feature in simulation profile of the Simulink, by the target language compiler (TLC). If the emulation platform is installed, the TLC is installed and it adds necessary features to the simulation profile in MATLAB®. This provides for targeting the code to be developed, specific to AMD Opteron®. The code will be available in **.sdf** – a system description file. This code shall be downloaded to the processor for running in real-time.

Graphical user interface (GUI) and virtual instrumentation (VI)

The installation of the dSPACE modular system also installs the GUI and the VI for the system, together is called the Control-Desk [dSPACE(2001)]. It provides for – setting the emulation profile, downloading the **.sdf** file onto the processor and controlling the execution of the program. It also has a virtual instrumentation, through which it is possible to – control real-time inputs to the model, observe (in virtual meters (analog or digital) or in virtual scopes) the quantities of interest, and store the results of conducting the experiments.

Process of validation

Simulation

The algorithm to be tested is first simulated in Simulink®. The schematic is as shown in Figure 3.27. The edited algorithm is initialized with the parameters and the signals are assigned proper values. Appropriate simulation step-size (a fixed step-size is chosen, which is necessary for real-time simulation), and an appropriate numerical integration algorithm is selected (like the Runge-Kutta 4^{th} order). The algorithm is tested and checked for desirable performance parameters. Several repeated trials of

the experiments are conducted and the parameters of the system are adjusted until satisfactory results are obtained.

Real-time emulation

Now the model is set-up for real-time test on the real-time hardware-emulation platform – the dSPACE Modular system based on DS1006. The signal sources used above now work as signal generators in reality and are directed to the DACs on DS2101 board. These signals are connected externally to the ADC inputs available on DS2002 board. This is achieved by utilizing the ports provided in the RTI library of Simulink Tool-box. The ADC outputs are picked-up by the processor through the ADC output ports. Thus the emulation set-up is made ready.

Now the same simulation-profile used for the off-line simulation is used also for the emulation of the algorithm. However the duration of simulation is set to infinity, so that the real-time emulation results can be observed in a continuous time. The results are observed and any fine-tuning of the system parameters is done if found necessary. The final values of the system parameters arrived at are reported which can be used for implementation in a μC, μP, DSP, DSC, or FPGA. The whole process is depicted as shown in Figure 3.28.

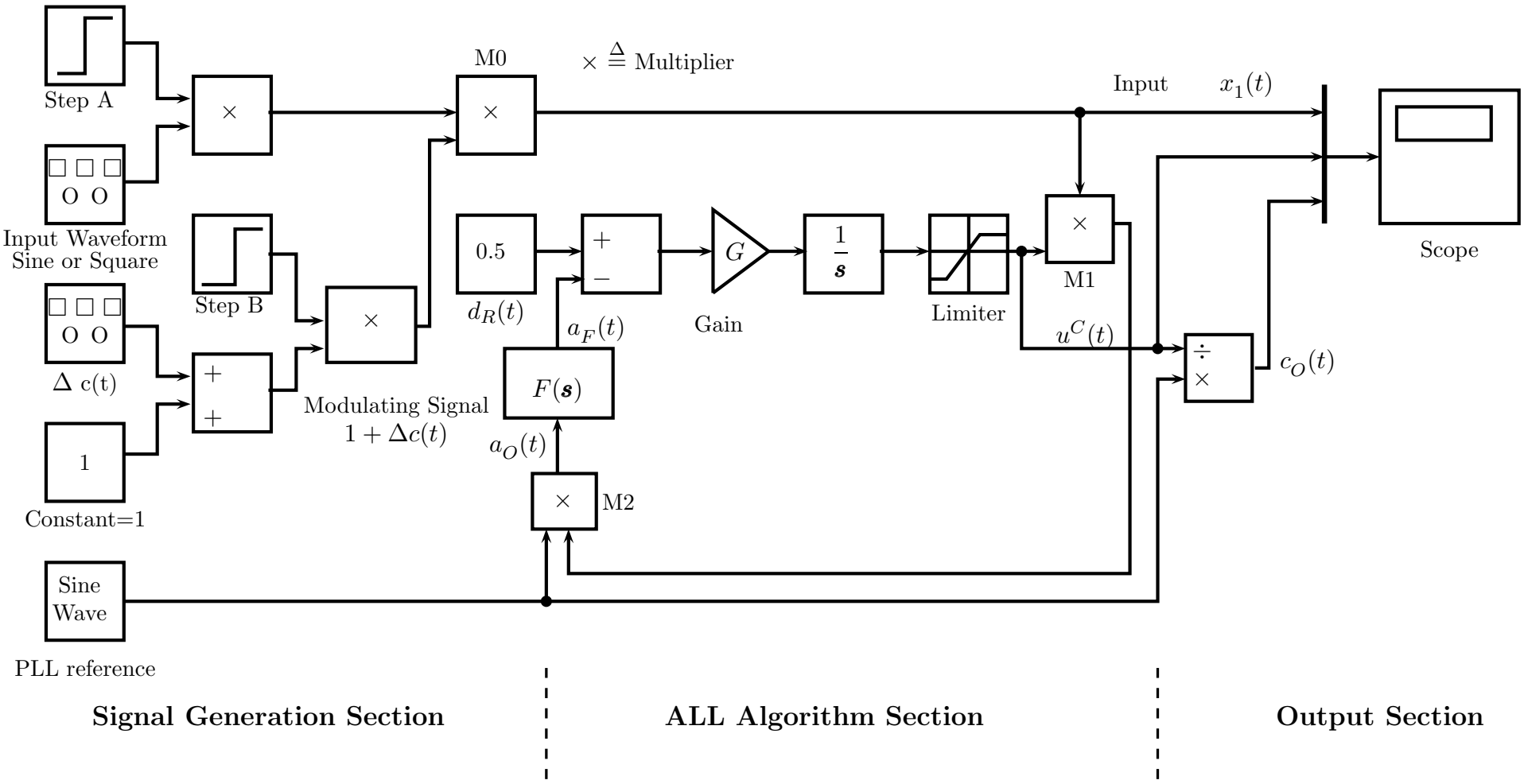


Figure 3.27: Simulink® schematic of the Algorithm-2

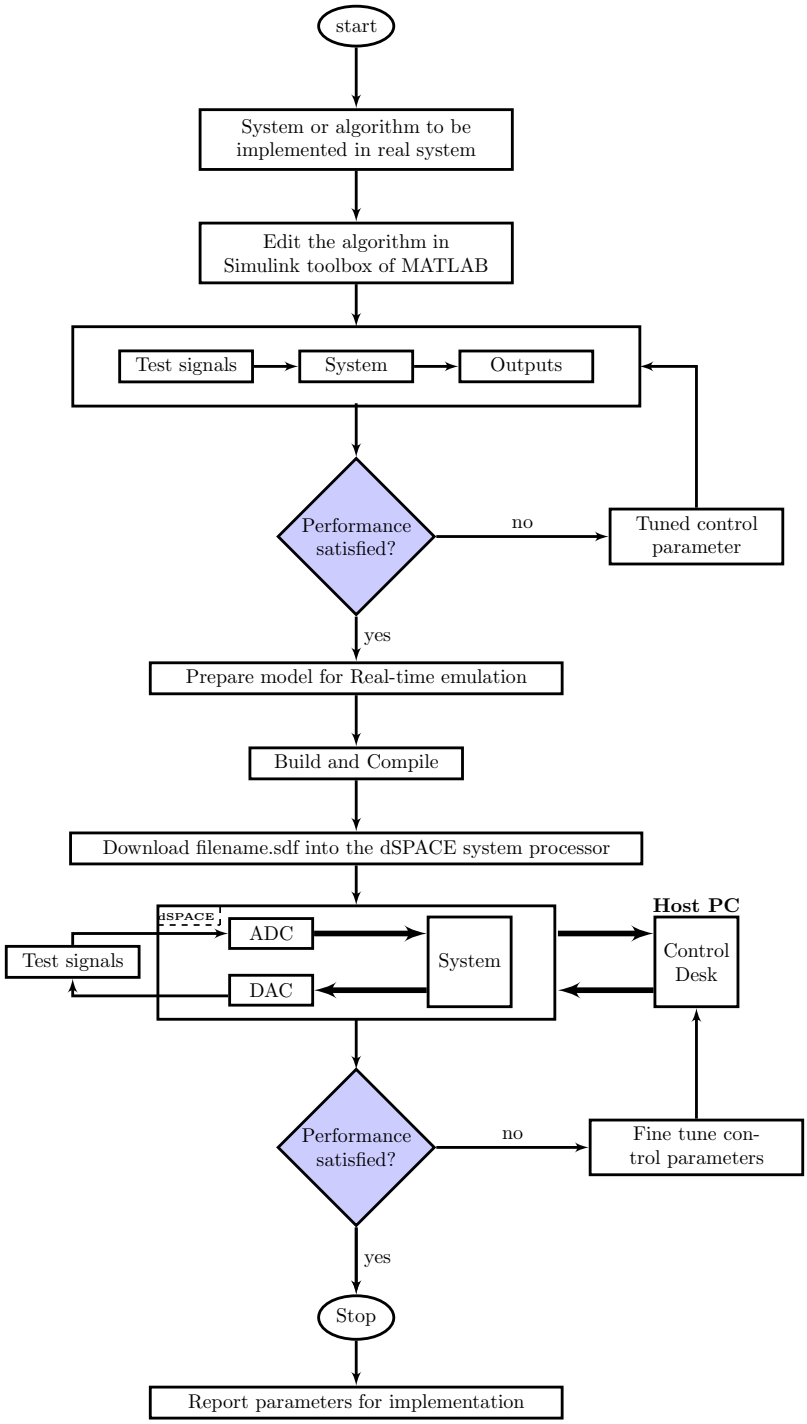


Figure 3.28: Schematic for the process of validating the algorithm on a real-time hardware-emulation platform

Experimental setup

Experimental setup is shown schematically in Figure 3.29. The algorithm to be verified in real-time is first simulated in MATLAB®/Simulink®. Input and output ports are appropriately selected from the RTI library, for the DS1006 Modular System. The ADC and DAC cards provide the necessary interface to the external system. MATLAB

generates the code for the system, which is downloaded into the processor in DS1006 board.

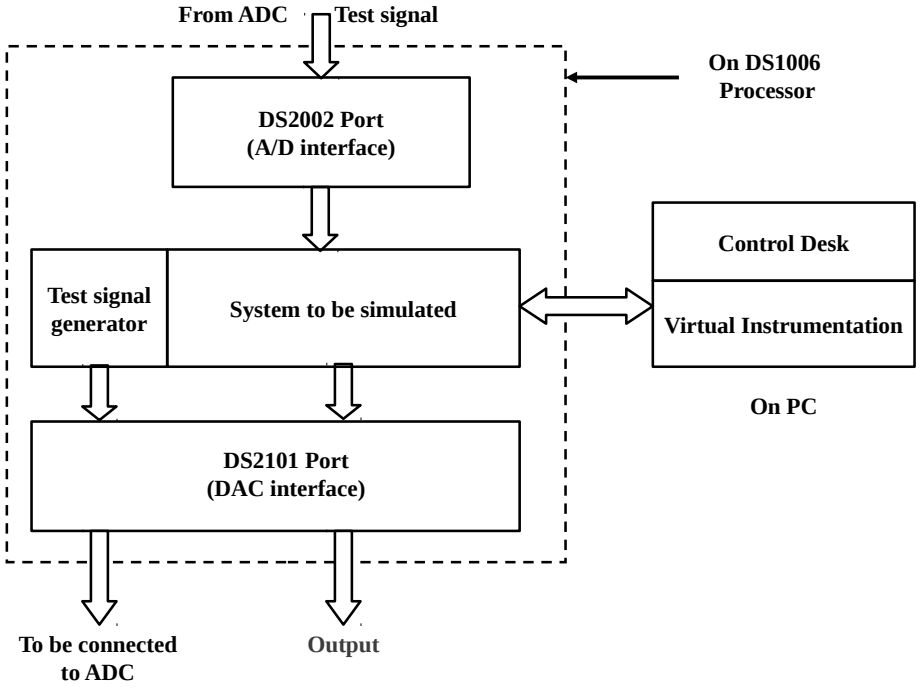


Figure 3.29: Real-time experimental setup schematic

3.4.2 Real-time simulation of Algorithm-1: Parameter Set-1

In this section real-time simulation results from the Novel Algorithm is presented. Extensive emulation studies were conducted on the scheme under consideration using MATLAB® and Simulink®. Various features of the system with $\omega_n = 100\pi$ rad/s, $Q = 2.0$, and $G = 180$ were explored for different inputs. The model of the algorithm is run on DS1006 with fixed step sizes of 20 μs, 50 μs, and 100 μs. With minor tuning of the controller parameters for each case, all cases gave satisfactory results, comparable with the off-line simulation results presented in Section 3.2. The results for a test with a step-size of 50 μs are presented, in Figure 3.30 to Figure 3.35. All results presented are screen-shots directly obtained from the Control-Desk of the Modular system.

Response to step-change in amplitude C_1

A sine-wave input of $C_1 = 0.5$ unit amplitude with a frequency of $\omega_o = 100\pi$ rad/s, applied to the circuit at $t = 0$ s is changed to $C_1 = 0.5$ unit at $t = 0.2$. The signal is

shown in Figure 3.30. The Figure 3.31 shows how the amplitude of the response settles.

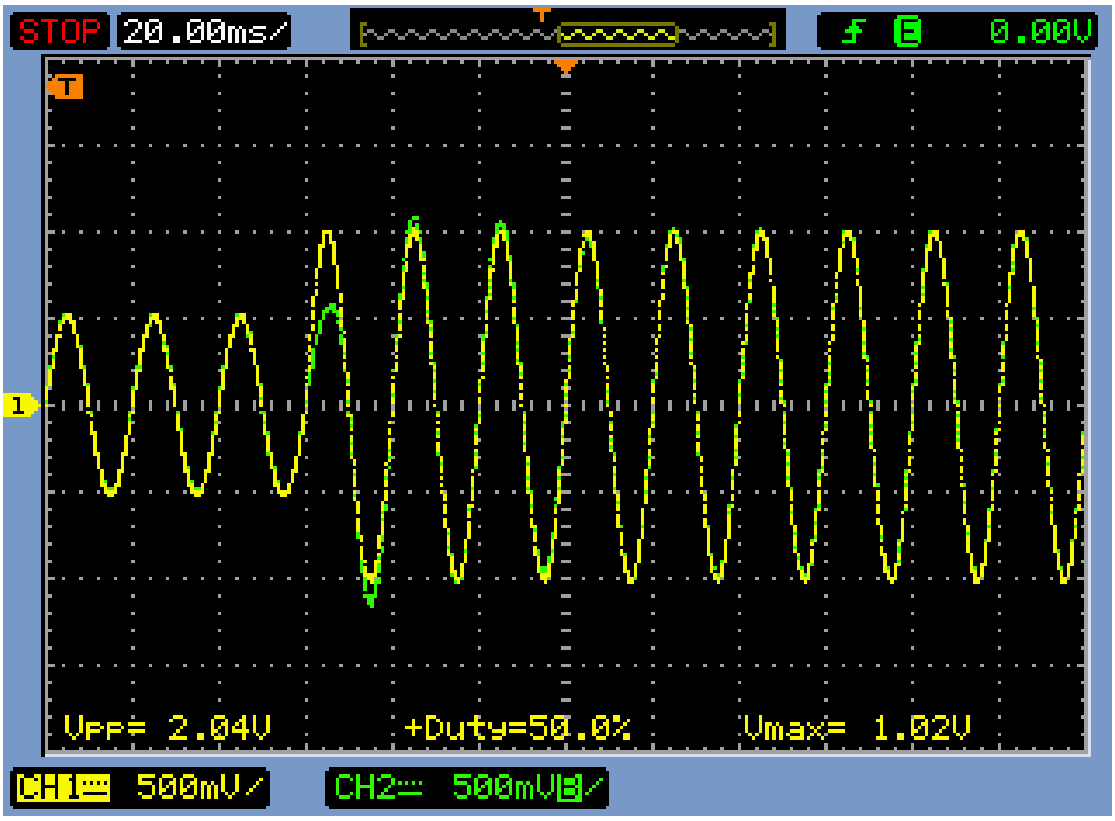


Figure 3.30: Sinusoidal input showing a step-change of 0.5 per unit in the amplitude at t=0.2 s; Legend: $x_1(t)$ – Yellow, $x_O(t)$ – Green.

The system settling-time indicated by the signals is captured here. It can be observed that the response in Figures 3.30 and 3.31 compare with that shown in Figures 3.7 and 3.8 respectively.

Response to square-wave input: The fundamental $x_1(t)$

For the square-wave input the fundamental extracted signal along with the input is shown in Figure 3.32. It can be clearly seen that the fundamental settles to final value before 1.5 cycles. This is as good as the best algorithms in this class [Karimi *et al.*(2003)]. It is also to be noted that the extracted fundamental is in synchronization with respect to the input square-wave and the steady-state error is less than 1.5%.

Response to step input: The harmonics in $x_I(t)$

The harmonic component extracted from the square-wave is shown in Figure 3.33.

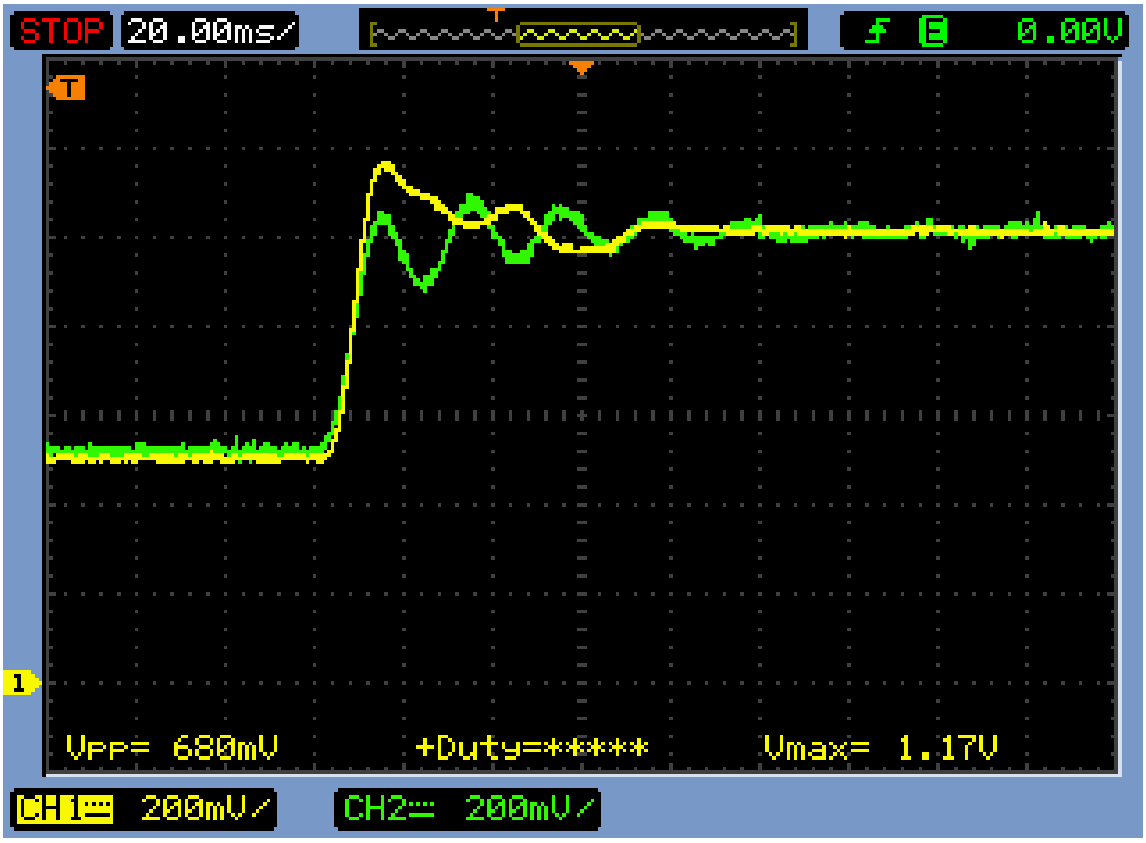


Figure 3.31: Step response showing settling time for a step-change in sine-wave input; Legend: Yellow – actual system output, Green – response from the LTI model.

Response to input amplitude modulation

The performance of the scheme is verified for tracking a slow-varying amplitude, as might happen in power system. This feature is also important for amplitude demodulation in other applications like in signal-communication systems. The input considered is:

$$x_I(t) \quad = \quad [1 + \Delta c(t)] \sin(100\pi t) = [1 + 0.2 \sin(4\pi t)] \sin(100\pi t). \qquad (3.52)$$

The modulating signal $\Delta c(t)$ (=$0.2 \sin(4\pi t)$ having a relative depth of modulation of 0.2 units, and a frequency of modulation of 2 Hz) is modulating the 50 Hz signal with an amplitude of 1.0 unit. The Figure 3.34 displays an area zoomed to around one cycle of the modulating signal in order to clearly show the negligible phase-lag between the output and the input modulating signal. It should be noted that the phase-angle must be measured between the input and the average of the output, where the ripples due to 50 ± 2 Hz should vanish. This shows the good tracking ability of the algorithm and is on a par with the competing algorithms in this category.

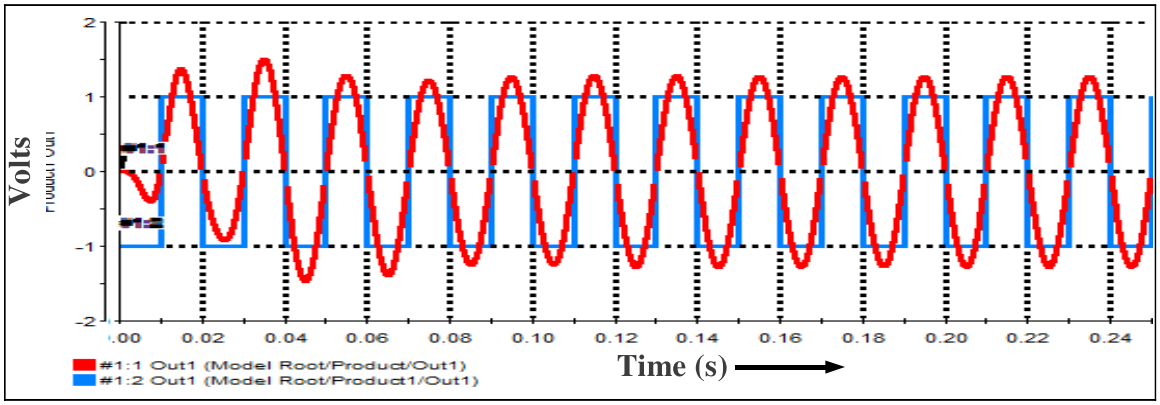


Figure 3.32: Output for a square-wave input, Legend: Blue – input; Red – output

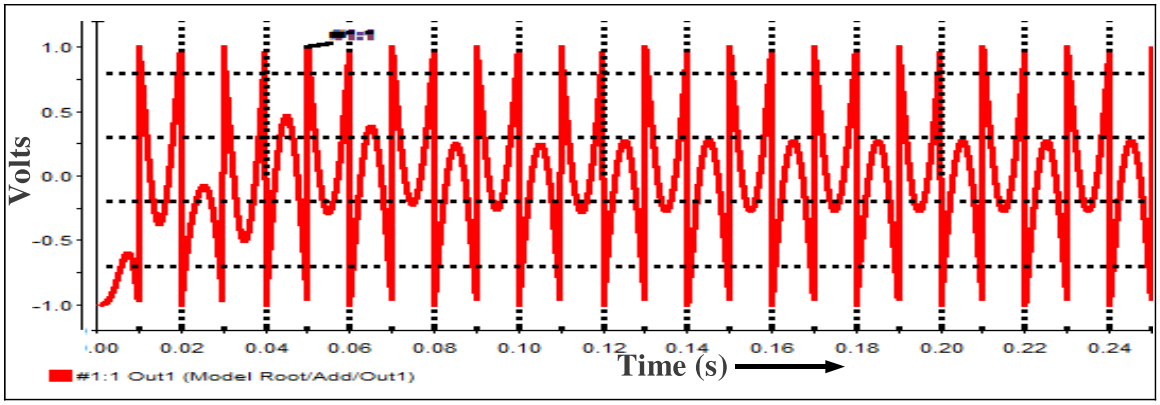


Figure 3.33: Harmonics extracted from a square-wave input

Noise rejection

Experiments are conducted to assess the noise rejection capabilities of the ALL. The Figure 3.35 shows the input, which is a sine wave of 100π rad/s with band-limited white noise, and the corresponding output. For an input with signal-to-noise-and-distortion ratio (SNDR) of 6 dB, the SNDR of the output was observed to be 36.3 dB. It can be clearly seen that the noise is severely attenuated in the output. It works very well under noisy environments.

3.4.3 Real-time simulation of Algorithm-1: Alternate Parameter Set

In this section the real-time simulation results from the Novel Algorithm obtained for a better set of parameters is presented. The set with $\omega_n = 100\pi$ rad/s, $Q = 0.95$, and $G = 180$ were explored for different inputs. The model of the algorithm is run on DS1006 with fixed step sizes of 20 μs, 50 μs, and 100 μs. The results for a test with a step-size of 50 μs are presented, for a sine-wave input applied to the full model and C_1

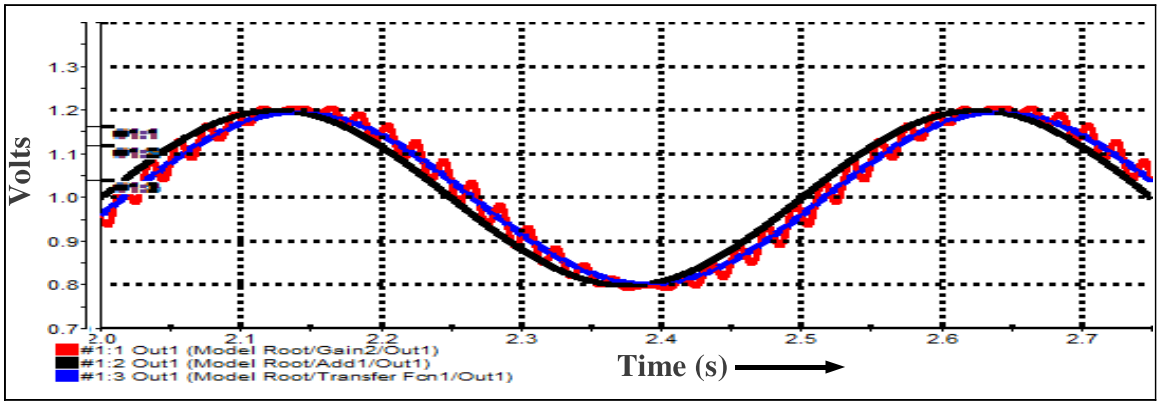


Figure 3.34: Output amplitude to an input whose amplitude is modulated Legend: black – input; red – output, blue – LTI equivalent output

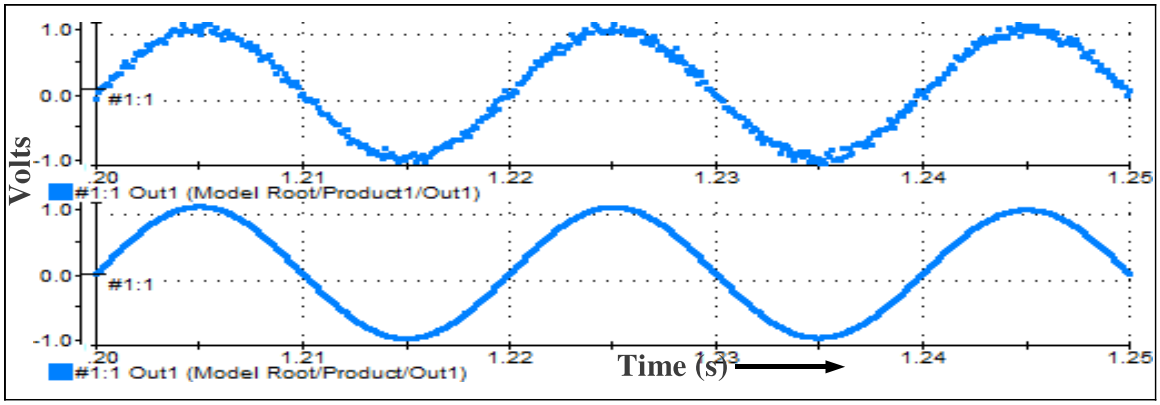


Figure 3.35: Performance under noisy conditions Legend: top – noisy input; bottom – filtered output

to its LTI equivalent. With a value of $C_1 = 0.5$ unit amplitude at $t = 0$ s is changed to $C_1 = 1$ unit at $t = 0.2$ s. The frequency $\omega_1 = 100\pi$ rad/s.

Response to step-change in amplitude C_1

The Figure 3.36 shows $x_1(t)$ and $x_O(t)$ for the full model. The Figure 3.37 shows how the amplitude of the response settles – comparing the full model response to the LTI equivalent. The system settling-time indicated by the signals is captured here. It can be observed that the system settles to the final value within around 1.5 cycles.

3.4.4 Real-time simulation: Algorithm-2

In this section real-time simulation results from the Pettigrew's algorithms is presented. Extensive emulation studies were conducted on the scheme under consideration using MATLAB® and Simulink®. Various features of the system with $\omega_c = 70\pi$ rad/s, $Q = 0.85$, and $G = 118$ were explored for different inputs. A lower limit of 0.2 for u ($\equiv$ 5 for C_1) was set. The model of the algorithm is run on DS1006 with fixed step sizes

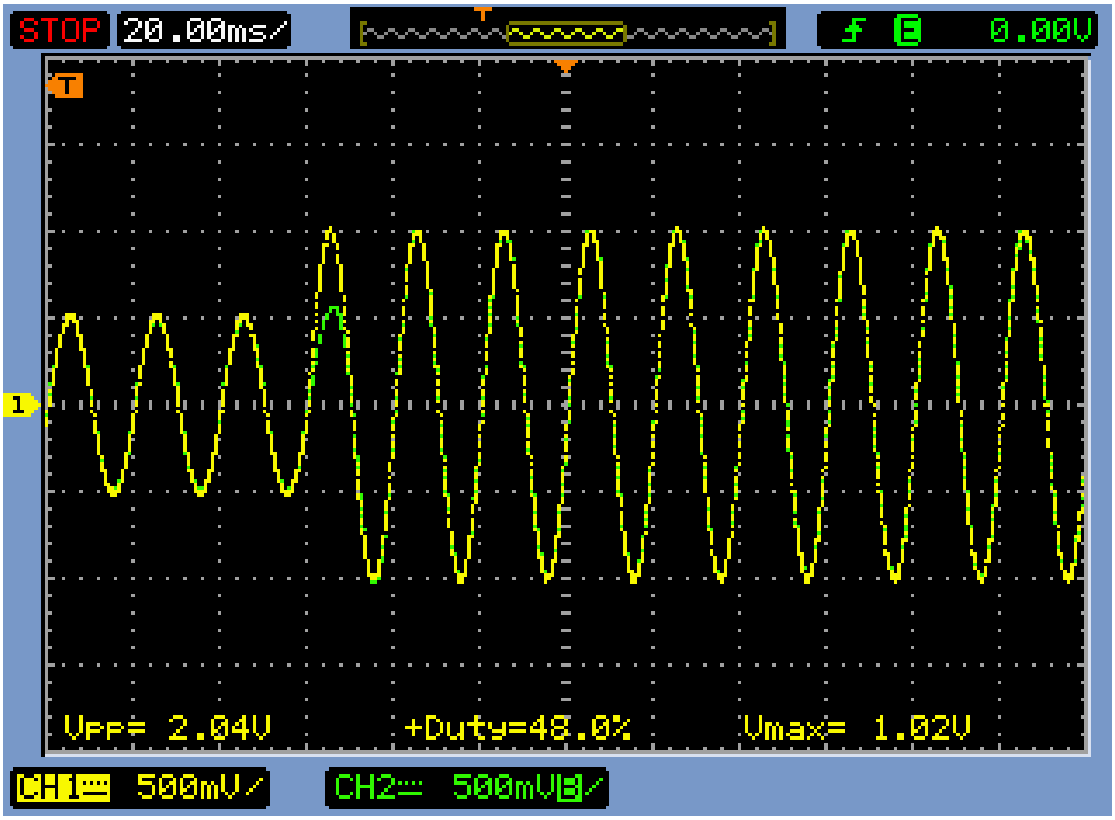


Figure 3.36: Sinusoidal input showing a step-change of 0.5 per unit in the amplitude at t=0.2 s; Legend: $x_1(t)$ – yellow, $x_O(t)$ – green.

of 20 μs, 50 μs, and 100 μs. With minor tuning of the controller parameters for each case, all cases gave satisfactory results, comparable with the off-line simulation results presented in Section 3.3. The results for a test with a step-size of 50 μs are presented, in Figure 3.38 to Figure 3.42. All results presented are screen-shots directly obtained from the Control-Desk of the Modular system.

Response to step input: The amplitude C_1

A square-wave input of unit amplitude with a frequency of $\omega_o = 100\pi$ rad/s, is applied to the circuit at $t = 0.1$ s. The settling-time indicated by the signals u and c is captured in the Figure 3.38. It can be observed that the system settles to final value within around 1.5 cycles, which is much better than the existing schemes. The expected fundamental amplitude ($=\frac{4}{\pi}$) is also plotted to show the settling-time.

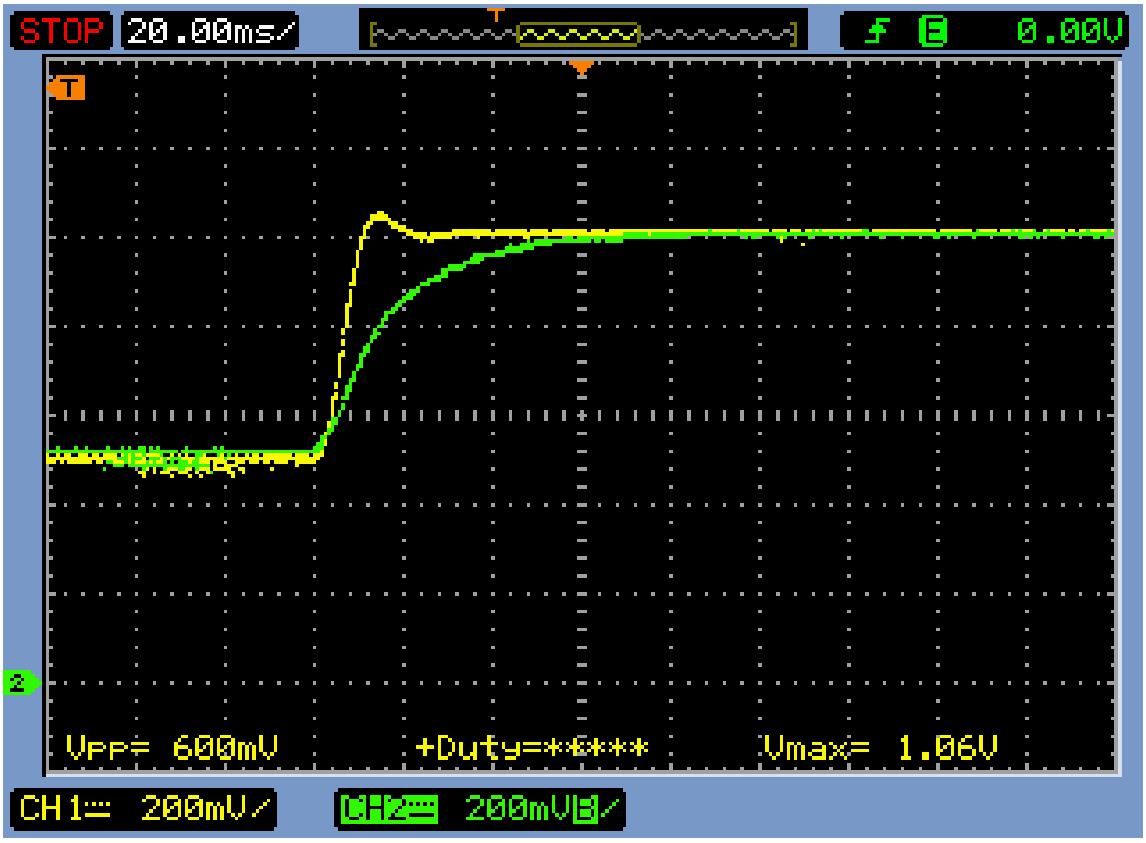


Figure 3.37: Step response showing settling time for a step-change in sine-wave input; Legend: Yellow – actual system output, green – response from the LTI model.

Response to step input: The fundamental $x_1(t)$

For the square-wave input the fundamental extracted signal along with the input is shown in Figure 3.39. It can be clearly seen that the fundamental settles within 1.5 cycles. This is as good as the best algorithms in this class [Karimi *et al.*(2003)]. It is also to be noted that the extracted fundamental is in synchronization with respect to the input square-wave and the steady-state error is less than 1.5%.

Response to step input: The harmonics in $x_I(t)$

The harmonic component extracted from the square-wave is shown in Figure 3.40.

Response to input amplitude modulation

The performance of the scheme is verified for tracking a slow-varying amplitude, as might happen in power system. This feature is also important for amplitude demodulation in other applications like in signal-communication systems. The input considered

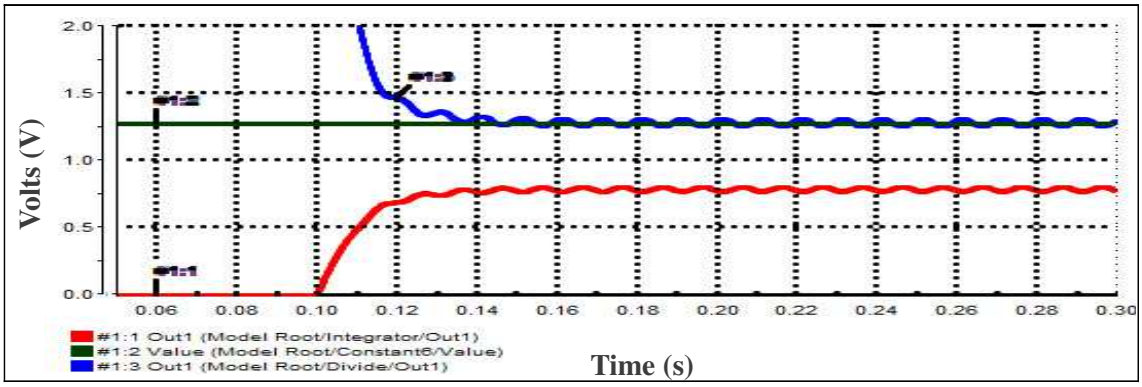


Figure 3.38: Step response showing settling time for a square-wave input, Legend: red $\leftrightarrow$ u; black $\leftrightarrow \frac{4}{\pi}$; blue $\leftrightarrow$c

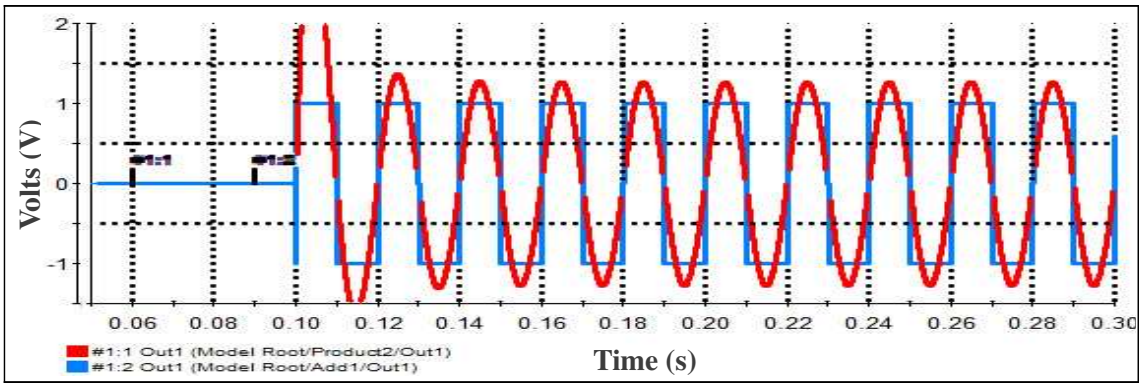


Figure 3.39: Output for a square-wave input, Legend: blue – input; red – output

is:

$$x_I(t) \quad = \quad [1 + \Delta c(t)]\sin(100\pi t) = [1 + 0.2\sin(4\pi t)]\sin(100\pi t). \tag{3.53}$$

The modulating signal $\Delta c(t)$ (=$0.2\sin(4\pi t)$ having a relative depth of modulation of 0.2 units, and a frequency of modulation of 2 Hz) is modulating the 50 Hz signal with an amplitude of 1.0 unit. Figure 3.41 displays an area zoomed to around one cycle of the modulating signal in order to clearly show the negligible phase-lag between the output and the input modulating signal. It should be noted that the phase-angle must be measured between the input and the average of the output, where the ripples due to 50 ± 2 Hz should vanish. This shows the good tracking ability of the algorithm and is on a par with the competing algorithms in this category.

Noise rejection

Experiments are conducted to asses the noise rejection capabilities of the ALL. The Figure 3.42 shows the input, which is a sine wave of 100π rad/s with band-limited white noise, and the corresponding output. For an input with signal-to-noise-and-distortion

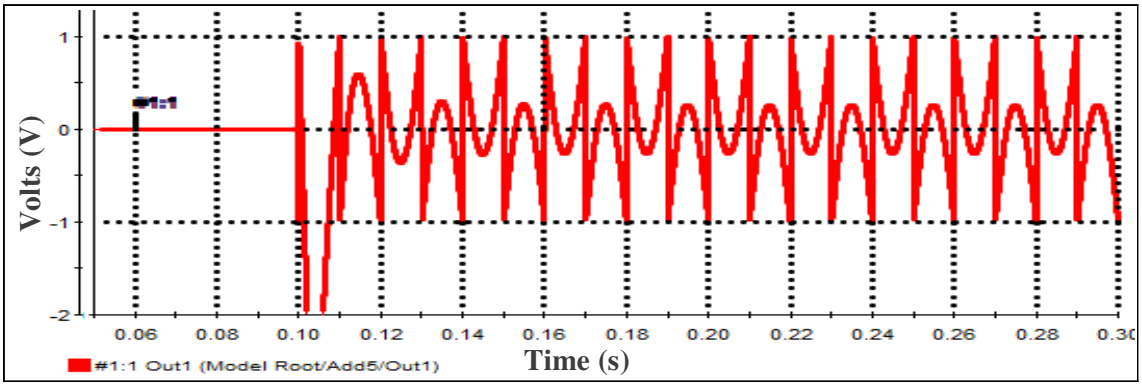


Figure 3.40: Harmonics extracted from the square-wave input

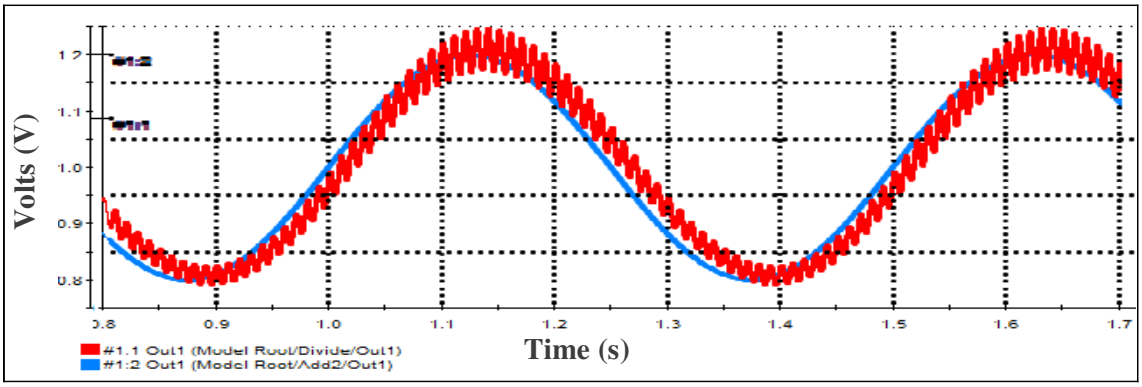


Figure 3.41: Output amplitude to an input whose amplitude is modulated Legend: blue – input; red – output

ratio (SNDR) of 6 dB, the SNDR of the output was observed to be 36.3 dB. It can be clearly seen that the noise is severely snubbed in the output. It works very well under noisy environments.

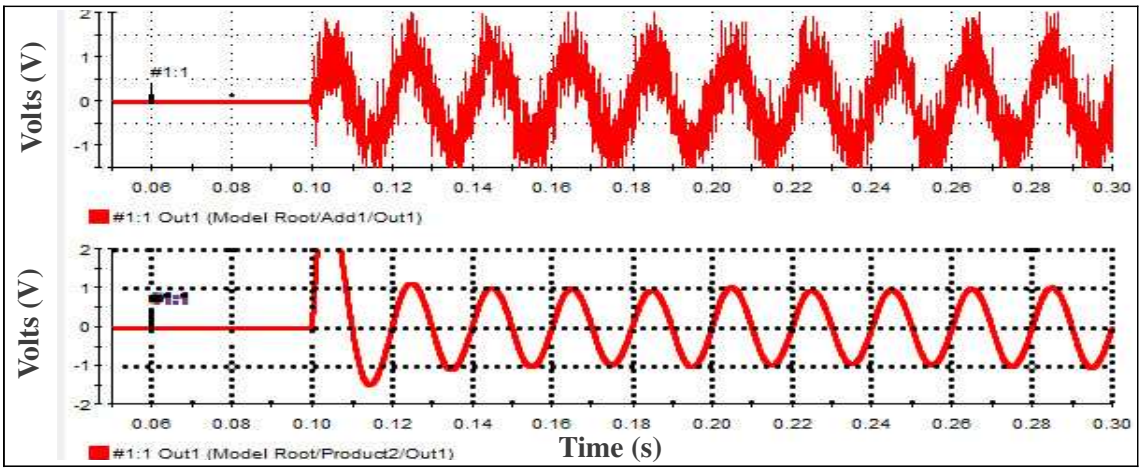


Figure 3.42: Performance under noisy conditions Legend: top – noisy input; bottom – filtered output

3.4.5 Observations from Real-time implementation

It is proposed to validate the real-time implementation of the proposed extraction techniques for extracting the harmonics and/or the fundamental from a distorted periodic signal. The algorithms are implemented on a real-time emulation platform – dSPACE Modular System based on DS1006, and the results of the tests are presented.

It is found that the results of teal-time hardware implementation responses compare very favorably with the results of its off-line simulation. Hence the possibility of its application to Active Power Filtering of harmonics in power systems stands confirmed.

3.5 Conclusions

The principle of operation and design of the algorithms proposed for extraction of harmonics and/or fundamental from a distorted periodic signal are presented. The simulation results are discussed. The results from the real-time implementation of the algorithms are given at the end. The results are summerised as follows:

- Settling time is dependent on tuning and it has been possible to get a speed of as good as 1.5 cycles on 50 Hz, for both Algorithms.
- Accuracy: Can be seen in the spectra presented, in Figures 3.13 and 3.23, by comparing spectra of the Output with that for the corresponding Input.
- Frequency tracking: Tracks a variation as high as 5 Hz/s, which is much beyond the rate of system frequency variation, Figure 3.10.
- Noise immunity: SNDR as high as 25-36 dB in the output for an input with an SNDR of 6-7 dB for the chosen parameters, Figures 3.14 and 3.25.

It is found that both the algorithms gave satisfactory performance under the steady-state and transient conditions. Their tracking abilities and noise rejection properties are excellent. This confirms that the algorithms can be used in real systems for for extraction of harmonics and/or fundamental from a distorted periodic signal. In Chapter 5 these algorithms are incorporated in the Power-Shield and the their capabilities are tested.

Chapter 4

Investigation on alternative Switching schemes for Hysteresis Control

4.1 Introduction

The implementation of the Shunt Active Filters is by current control of voltage source inverters employing a suitable switching technique. Hysteresis or bang-bang control is a very effective method of current control in power electronics circuits. It is considered to have the advantages like – the model of the plant is not necessary for control; it is very easy to implement; and it is very stable [Bose (1990)]. However it suffers from – the need for specification of a good hysteresis band, the variation of the switching frequency over the cycle, and a steady-state error when implemented with a constant *sampling* frequency, which is the practice in digital implementation. Some of these problems get minimized with a feedback control by means of an additional control effort and some error may remain without correction and thus resulting in a poor control performance. The claim that the hysteresis control renders a model independent control with respect to the variations in system parameters also need not be correct. Some of these problems are brought out in this chapter and two techniques making use of voltage at the **far-end** (while the other end termed as the **VSI-end**) of the current injecting inductor are proposed. In this Chapter only the performance evaluation of the proposed switching techniques is attempted, with reference to a common reference circuit. A voltage source, a load as stiff as an ideal current source, and a sample VSI based current injector, form a common system, against which the algorithms are tested. The parameters used for

comparison are defined and the process employed and its implementation are discussed in this chapter. Some conclusions are drawn based on the simulation results.

4.2 Hysteresis control techniques

4.2.1 Review

The closed-loop current control is required in many applications. The hysteresis control technique has been used in many applications requiring a closed-loop current control with great success. Many variations are tried with varying results. A paper by Brod and Novotny [Brod and Novotny(1985)] has dealt in detail about various current control techniques like – ramp comparison control, predictive current control and the hysteresis control. A synchronous current controller is proposed by Rowen et al. [Rowen and Kerkman(1985)]. *Delta-modulation* technique is proposed by Hebetler et al. [Hebetler and Divan(1989)] which requires a switching frequency much higher than that of the fundamental to make the subharmonic insignificant. Some novel techniques based on space-phasor are proposed by Akira et al. [Nabae *et al.*(1986)] and Kwon et al. [Kwon *et al.*(1998)] which have a better performance but have more computations as it requires – an a priori computation of the voltage vector from the instantaneous value of the current and the current-injecting-inductor parameters (its resistance and inductance values) and the determination of the position of the **far-end** voltage vector. Some pre-programmed schemes [Enjeti *et al.*(1988)] with optimal switching frequency and pattern are suggested which are not suitable for power quality disturbance mitigation. A novel technique proposed by Malesani et al. [Malesani *et al.*(1991)] has the effect of minimising the interactions between the phases. A three-level hysteresis scheme is suggested by Chisrelli et al. [Chisrelli *et al.*(1993)] for single-phase UPS applications.

4.2.2 Performance evaluation

It is found that hysteresis control is simpler to implement and has better bandwidth. However the wide variation of the switching frequency for a wide variation of load has been a concern when implemented in analog form, including that of thinner pulses and the shoot-through faults. Also the method suffers from the problem of a conflicting requirements between the width of the current hysteresis band and the speed of response.

The claims that hysteresis control does not require the information about the model of the system is not completely true in practice, since a practical implementation requires a finite switching frequency. It should also be noted that the techniques referred above using information about the reference current and controlled current suffer from the problem of excessive current at the modulating frequency or the sub-harmonic frequencies. At these low frequencies the impedance offered by the injecting-inductor being very low, any small differential voltage across it can result in a large current. A hysteresis controller having no knowledge of the **far-end** voltage has to rely heavily on the ideal implementation, which is near possible only when the switching frequency is excessively high. In actual practice, where an overriding/ supervisory closed-loop control is used to determine the reference current itself, then it is possible to obtain a better tracking, with an additional control effort, as determined by the overriding control loop.

In all the schemes proposed so far the **far-end** voltage information is not considered. However if it is used, a direct and fast control with an improved tracking can be achieved. This is considered in this thesis and presented in this chapter.

4.3 Novel Multi Criteria Based Switching Principle

A switching technique which makes use of the three voltage levels [+1, 0, -1] from the VSI bridge, error in the injected quantity, polarity of the supply voltage, a periodic sampling, and the specified hysteresis band is developed. It has shown improvements over the basic hysteresis control, in terms of the reduction in the number of switchings per cycle and the distortion in the injected current. Consider the circuit shown in Figure 4.1 for the purpose of discussion. As shown, the current-injecting-inductor L_1

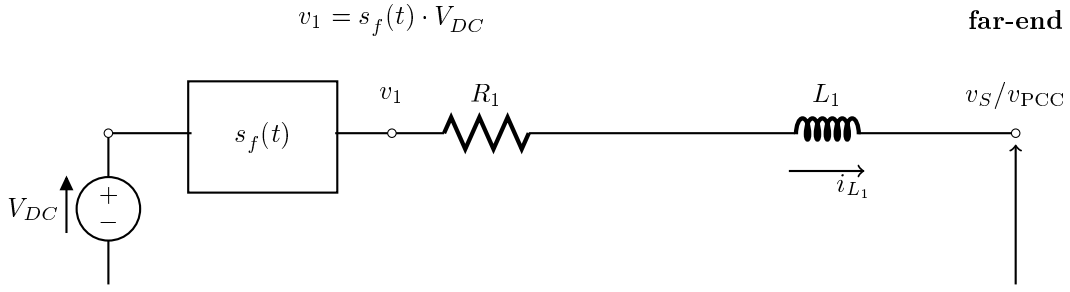


Figure 4.1: Circuit for demonstrating the effect of **far-end** voltage on the performance of the Basic hysteresis scheme

with its ESR R_1, is connected at the **far-end** to the PCC and at the other end, the VSI end to v_1 – the output of the inverter. $s_f(t)$ is the time dependent switching function decided by the switching Schemes, that determines v_1. The knowledge of v_S is used in the proposed switching Schemes.

Criteria used for novel hysteresis controller

A new basis for hysteresis control is presented which considers the **far-end** voltage information in addition to the sign and magnitude of the current tracking error. It can lead to many schemes depending upon the way and the extent to which that information is used. In the simplest form the *polarity* information of the voltage is used. In the present case it is considered to investigate the performance of the schemes with the incorporation of the following features:

- polarity information of the **far-end** voltage
- sign and magnitude of the error in the current
- three-level switching [1, -1, 0]
- periodic sampling with switching at integral multiples of sampling period (T_{sw}).
- switching decided by the rules specific to the schemes proposed here

A blend of novel hysteresis-switching synchronised with supply waveform

In this simulation study all the schemes considered are implemented at a maximum sampling-cum-switching frequency (f_{sw}) of 10 kHz. The basic hysteresis scheme also is considered for comparison, but with the constant switching frequency of 10 kHz. The schemes are implemented by triggering switching-decision block at f_{sw}. The actual switching period for the basic scheme will be at the switching period (T_{sw}), but for the novel schemes proposed here it will be at integer multiples of T_{sw}. This results in reduced number of switchings per fundamental period, without compromising on the quality of the tracking. The reduction in the number of switchings is expected to come from skipping the switching(s) at constant frequency when there is no need to do so. The switching is also line-locked with the supply. The synchronization with the line is expected to render periodicity (at fundamental) of the control sequence and hence

alleviate the problem of subharmonic oscillations. This is in line with the choice of synchronous algorithms for extraction of compensating quantities in this thesis.

4.4 The Process

The evaluation of any scheme requires a platform to conduct the experiments and a basis for comparison. Then a set of steps are required to collect or generate the data necessary for drawing conclusions. In the present case the steps followed are summarized below:

1. Define a set of performance parameters for comparison.

2. Choose a circuit with necessary circuit elements and sources to suit the purpose of the test and obtain the dynamic model of the circuit in state-space form: $\frac{d}{dt}\mathbf{x} = \mathscr{A}\mathbf{x} + \mathscr{B}\mathbf{u}$.

3. Conduct simulation experiments with the chosen cases on each of the schemes proposed here.

4. Analyse the data and draw conclusions.

4.4.1 Circuit considered

For the purpose of verifying the effectiveness or performance of the switching-schemes proposed, the circuit shown in Figure 4.2 is considered.

In the circuit the following quantities are referred as defined below:

$v_s(t)$	– Supply voltage	: $V_m \sin(\omega_1 t)$ volts
$i_O(t)$	– Current source	: a square-wave of amplitude I_O amperes and
		– period $T_1 = \frac{2\pi}{\omega_1}$ seconds
$v_1(t)$	– VSI output	: Controlled by the hysteresis controller
V_{DC}	– a constant	: The source voltage of the VSI.

The harmonic current in $i_O(t)$, is chosen as the reference current to be injected in L_1, say $i_C(t)$. $i_C(t)$ may be extracted by employing one of the algorithms proposed in Chapter 3. $i_C(t)$ is injected by controlling the voltage $v_1(t)$, of the VSI as controlled by the switching scheme employed.

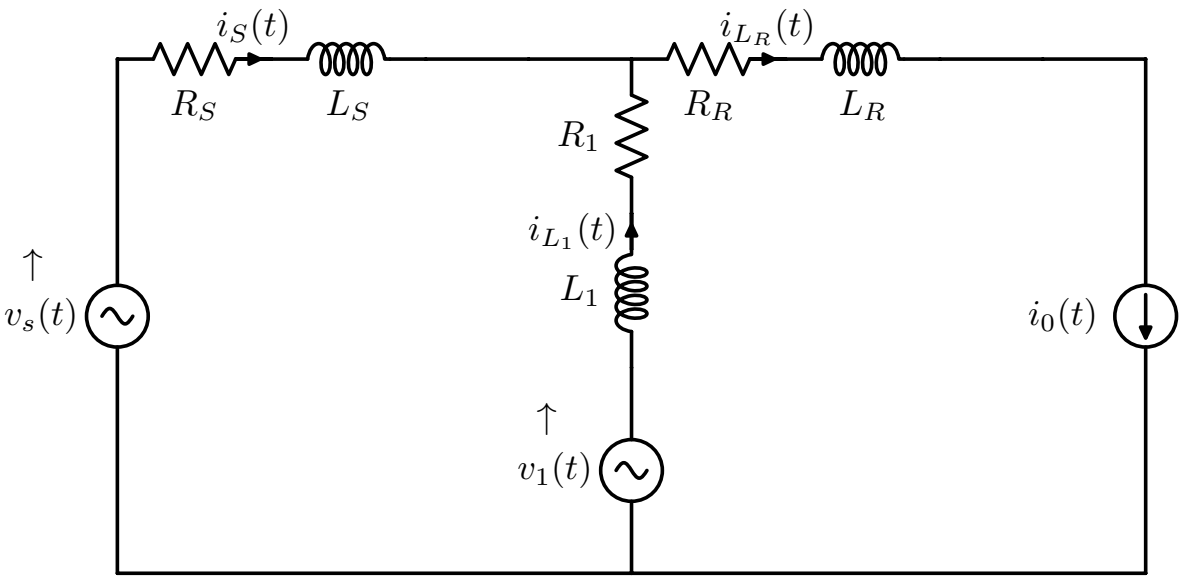


Figure 4.2: Circuit used for verifying the effectiveness of the proposed switching schemes

4.4.2 Basis for comparison

The effectiveness of the switching schemes is compared on the basis of – effectiveness of injection as measured by the difference between the spectral content of the reference current and that of the injected current, the RMS deviation, the number of switchings per cycle of the fundamental, and the computational complexity. In this context few parameters are identified as follows:

S_C	: Number of switchings per cycle of the fundamental, 50 Hz.
ϵ_k	: Tracking error (in ampere)s, $1 \leq k \leq K$ – sample count index, K – counts for one full cycle
μ_ϵ	: root mean square error (in amperes)
ϵ_{AR}	: Arithmetic Average error (in amperes)
ϵ_{AB}	: Absolute Average error (in amperes)
I_{L_1}	: Fundamental amplitude in the Injected current (in amperes)
I_{DC}	: Constant component in the Injected current (in amperes)
i_{REF}	: reference current to the hysteresis controller
i_{TRACK}	: Tracking current by the hysteresis controller

Some of the above identified parameters are defined mathematically as follows:

$$\epsilon_k = i_{REF_k} - i_{TRACK_k} \tag{4.1}$$

$$\mu_\epsilon = \sqrt{\frac{\sum_{k=1}^{K} \epsilon_k^2}{K}} \tag{4.2}$$

$$\epsilon_{AR} = \frac{\sum_{k=1}^{K} \epsilon_k}{K} \tag{4.3}$$

$$\epsilon_{AB} = \frac{\sum_{k=1}^{K} |\epsilon_k|}{K} \tag{4.4}$$

4.4.3 Simulation Setup

The simulation setup used is as shown in Figure 4.3.

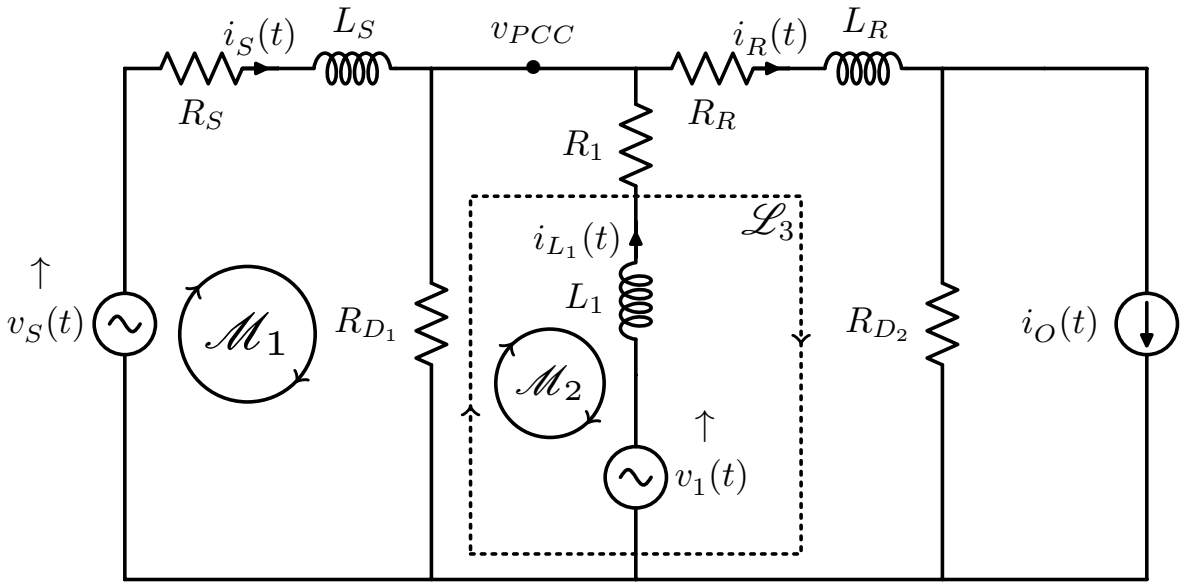


Figure 4.3: Circuit used for verifying the effectiveness of the proposed switching schemes

Here the $v_s(t)$ branch represents the source side, terminating at the point-of-common-coupling indicated by the voltage v_{PCC}. The hysteresis current control branch is containing the $v_1(t)$, and the right-most branch indicates the current source $i_O(t)$. The resistances R_{D_1} and R_{D_2} are dummy with a very large value and are included to remove degeneracy due to L-I (inductor, current-source) cut-sets: $\{L_S,\ L_1,\ L_R\}$ and $\{L_R,\ i_O(t)\}$. These are necessary for setting up the simulation to avoid impulses, which causes convergence problems during simulation.

4.4.4 Dynamic model of the circuit

The loop equations for the loops: $\{\mathscr{M}_1, \mathscr{M}_2, \mathscr{L}_3\}$ for the system shown in Figure 4.3 are,

$$\begin{aligned}
\text{Mesh} - \mathscr{M}_1 : \quad & v_s - R_s i_{L_S} - v_{L_S} - R_{D_1}(i_{L_S} + i_{L_1} - i_{L_R}) && = 0 \\
\text{Mesh} - \mathscr{M}_2 : \quad & R_{D_1}(i_{L_S} + i_{L_1} - i_{L_R}) + R_1 i_{L_1} + v_{L_1} - v_1 && = 0 \\
\text{Loop} - \mathscr{L}_3 : \quad & R_{D_1}(i_{L_S} + i_{L_1} - i_{L_R}) - R_R i_{L_R} - v_{L_R} - R_{D_2}(i_{L_R} - i_O) && = 0 \\
& . && \qquad (4.5)
\end{aligned}$$

These mesh equations are solved for the inductor voltages $[v_{L_S} \;\; v_{L_1} \;\; v_{L_R}] \stackrel{\Delta}{=} \mathbf{v_L}$ and expressed in a matrix form to give,

$$\left[\mathbf{v_L}\right] = \begin{bmatrix} -(R_S + R_{D_1}) & -R_{D_1} & R_{D_1} \\ -R_{D_1} & -(R_1 + R_{D_1}) & R_{D_1} \\ R_{D_1} & R_{D_1} & -(R_C + R_{D_1} + R_{D_2}) \end{bmatrix} \begin{bmatrix} i_{L_S} \\ i_{L_1} \\ i_{L_R} \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & R_{D_2} & 0 \end{bmatrix} \begin{bmatrix} v_S \\ i_O \\ v_1 \end{bmatrix} \qquad (4.6)$$

The voltage-current relations for the inductors are,

$$\begin{bmatrix} v_{L_S} \\ v_{L_1} \\ v_{L_R} \end{bmatrix} = \begin{bmatrix} L_S & 0 & 0 \\ 0 & L_1 & 0 \\ 0 & 0 & L_R \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L_S} \\ i_{L_1} \\ i_{L_R} \end{bmatrix}.$$

These are expressed in differential equations form as:

$$\frac{d}{dt} \begin{bmatrix} i_{L_S} \\ i_{L_1} \\ i_{L_R} \end{bmatrix} = \begin{bmatrix} \Gamma_S & 0 & 0 \\ 0 & \Gamma_1 & 0 \\ 0 & 0 & \Gamma_R \end{bmatrix} \begin{bmatrix} v_{L_S} \\ v_{L_1} \\ v_{L_R} \end{bmatrix} \qquad (4.7)$$

where Γ_k are the levitances expressed in this context as L_k^{-1}. Substituting for $\mathbf{v_L}$ from (4.6) in (4.7) and after simplification we get,

$$\frac{d}{dt} \begin{bmatrix} i_{L_S} \\ i_{L_1} \\ i_{L_R} \end{bmatrix} = \begin{bmatrix} -\Gamma_S(R_S + R_{D_1}) & -\Gamma_S R_{D_1} & \Gamma_S R_{D_1} \\ -\Gamma_1 R_{D_1} & -\Gamma_1(R_1 + R_{D_1}) & \Gamma_1 R_{D_1} \\ \Gamma_R R_{D_1} & \Gamma_R R_{D_1} & -\Gamma_R(R_C + R_{D_1} + R_{D_2}) \end{bmatrix} \begin{bmatrix} i_{L_S} \\ i_{L_1} \\ i_{L_R} \end{bmatrix} + \begin{bmatrix} \Gamma_S & 0 & 0 \\ 0 & 0 & \Gamma_1 \\ 0 & \Gamma_R R_{D_2} & 0 \end{bmatrix} \begin{bmatrix} v_S \\ i_O \\ v_1 \end{bmatrix} \qquad (4.8)$$

The system represented by (4.8) is the state-space form representation of the circuit considered and shown in Figure 4.3.

4.4.5 The schematic representation of the simulation setup

The structure and the components of the simulation setup are as shown in Figure 4.4. The sampled hysteresis is implemented by making the hysteresis block to be executed as a triggered block, triggered by a pulse generator set to sampling frequency.

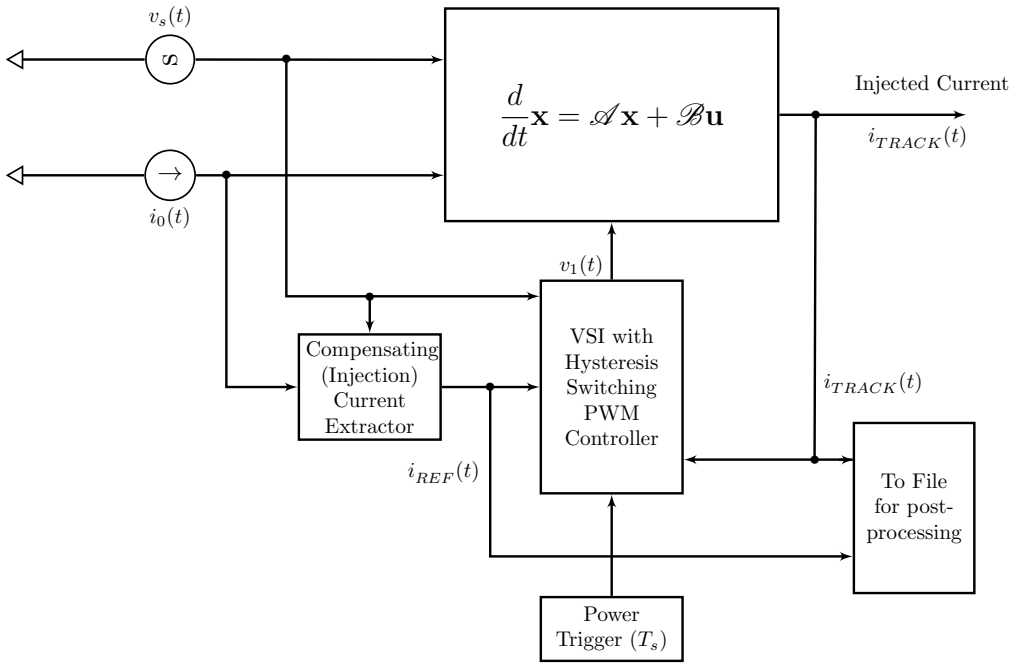


Figure 4.4: Setup schematic for coding the system represented by (4.8)

4.4.6 The Simulink schematic of the system

This set of equations (4.8) are coded in MATLAB®/ Simulink®, which is shown in Figure 4.5. The reference current to be injected in the L_1 branch using the hysteresis control is chosen as the harmonic component in the $i_O(t)$. It is obtained by employing one of the techniques proposed in Chapter 3. The hysteresis controller makes use of a subset of the information like – the reference current, the actual injected current, and the source or the voltage at the point-of-common-coupling – depending upon the switching technique employed, as discussed in the following. The voltage generated by the hysteresis controller $v_1(t)$, is input to the model as shown.

Simulation profile

The values of circuit elements and those of the parameters of the sources are edited in a **.m** file and run prior to starting of the simulation. A variable time-step-size t_s, (10^{-6}s $\leq t_s \leq 10^{-12}$ s) with *ode15s* method of simulation is used. The result of simulation is stored in the *each-case-id.dat* and is used for post processing.

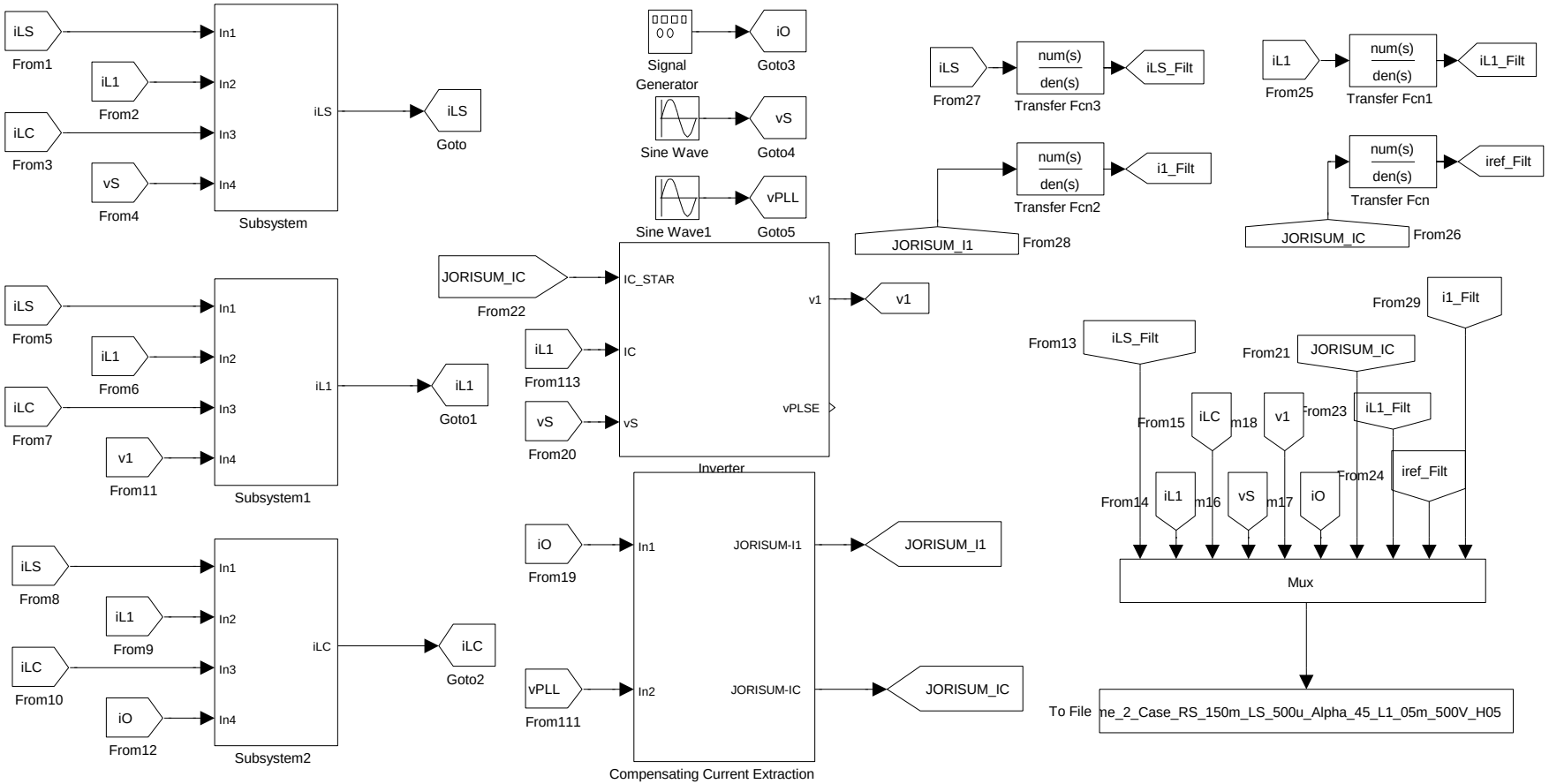


Figure 4.5: Simulink Setup for coding the system of equations (4.8)

4.5 Switching rules or Schemes and their implementation

In this section the switching schemes considered for comparison are explained and their implementations in Simulink® are shown. Here, v_S is used in place of v_{PCC}, as the difference between them is negligible. However, in practice v_{PCC} is expected to be used, which is sensed and used for several other purposes in the implementation.

4.5.1 The switching rule for the Basic Hysteresis

The basic hysteresis is generally based on an *a priori* defined hysteresis band Δi – shown as HLP in Simulink® setup. The reference current error $\Delta i^* \triangleq i_{TRACK} - i_{REF}$ (shown as DELTA_I in Simulink® setup) is compared with Δi, to determine the output voltage vector, either V or -V, a two level switching, where V is the value of the VSI source voltage V_{DC}. At any instant of sampling, the scheme is as detailed in Table 4.1.

Table 4.1: Switching scheme for Basic Hysteresis

if	$\Delta i^* \geq \Delta i$	then	$v_1 = -V$
else-if	$\Delta i^* \leq$-Δi	then	$v_1 = V$
else-if	-$\Delta i \leq \Delta i^* \leq \Delta i$	then	Do not change v_1, like,
	if $v_1 = V$	then	$v_1 = \quad V$
	else-if $v_1 = -V$	then	$v_1 = -V$

This is coded using the hysteresis block provided in the Simulink® library.

4.5.2 The switching rule for the Novel Hysteresis: Proposal Scheme-1

In this method of switching, in addition to the currents the voltage at the PCC is also used. Also the third level of a **zero**-level available in the VSI is used. Hence the switching strategy may be summarized as shown the Table 4.2. This is coded as shown in Figure 4.6 using the blocks provided in Simulink® library.

Table 4.2: Switching scheme for Novel Hysteresis Scheme-1

if	$\Delta i^* \geq \Delta i$	and	$v_S < 0$	then	$v_1 = -V$
else-if	$\Delta i^* \leq$ -Δi	and	$v_S > 0$	then	$v_1 = \quad V$
else	if none of the above conditions are met			then	$v_1 = \quad 0$

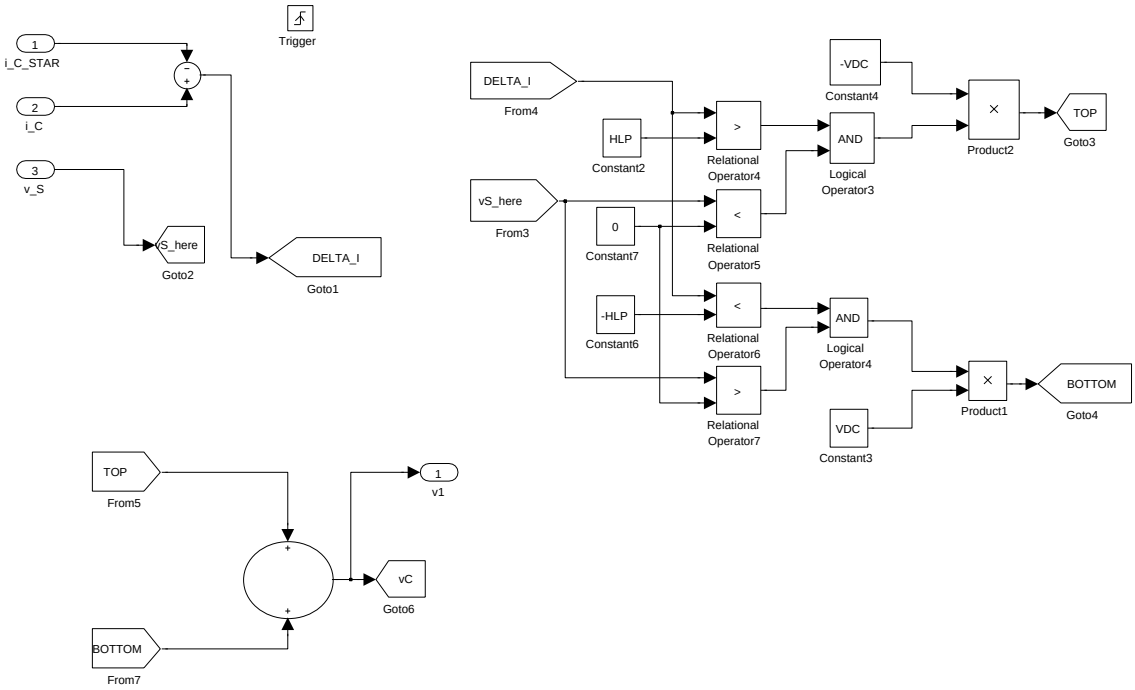


Figure 4.6: Simulink Setup for coding the decisions in Table (4.2)

4.5.3 The switching rule for the Novel Hysteresis: Proposal Scheme-2

A small extra addition in computation as shown in Table 4.3 leads to another scheme. A careful observation will reveal that it is not necessary to compute the **zero** vector. This scheme is implemented in Simulink® as shown in Figure 4.7.

It may be noted that the addition of the source voltage in decision making is not a burden, because, this information is anyway necessary in most of the cases as a reference for switching, like PLL. Compared to the improvement in the quality of the tracking, the extra burden of computation is bearable.

It may be noted from Tables 4.2 and 4.3, that, in Scheme-1 if Δi^* is within the hysteresis band, it will always switch to $v_1 = 0$ from its earlier states of $\{-V$ or $+V\}$. However in

Table 4.3: Switching scheme for Novel Hysteresis Scheme-2

if	$\Delta i^* \geq \Delta i$	and	$v_S < 0$	then	$v_1 = -V$
else-if	$\Delta i^* \leq$-Δi	and	$v_S > 0$	then	$v_1 = \quad V$
else-if	-$\Delta i \leq \Delta i^* \leq \Delta i$	then	Do not change v_1, like,		
	if $v_1 = V$	then			$v_1 = \quad V$
	else-if $v_1 = -V$	then			$v_1 = -V$
else	if none of the above conditions are met			then	$v_1 = \quad 0$

Scheme-2, it may not switch; it depends on the other conditions specified as tabulated therein; thus reducing the number of switchings. This difference will be observed in the results presented in Section 4.6.

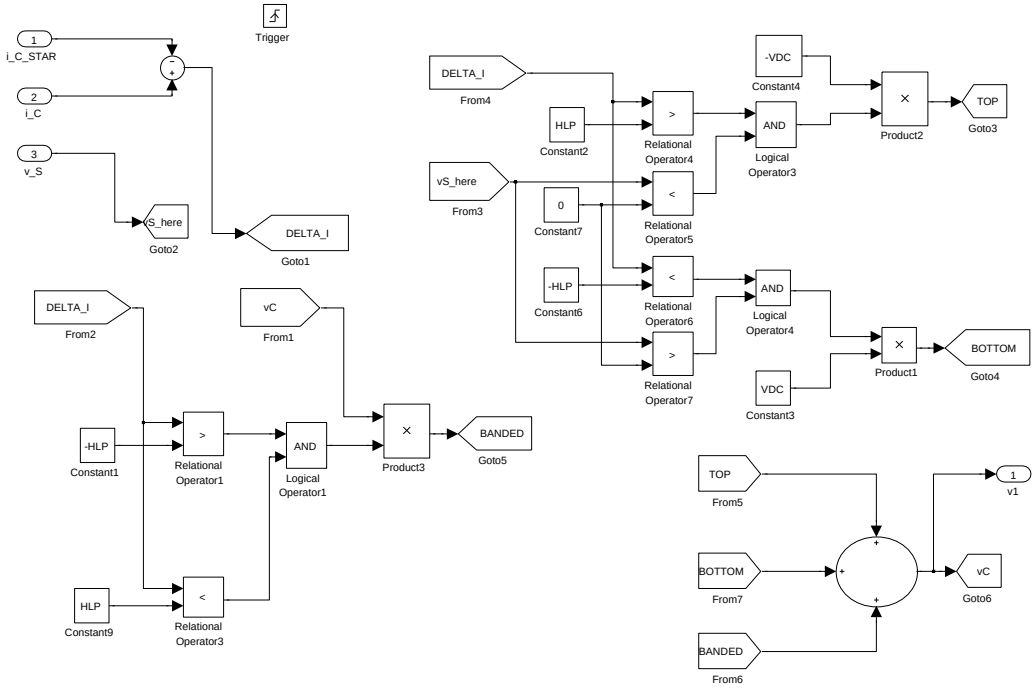


Figure 4.7: Simulink Setup for coding the scheme detailed in Table 4.3

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4.6 Simulation Results from Switching schemes

In this section the proposed switching schemes are evaluated. A common circuit as detailed below is used for comparison. In Section 4.6.1, the system description is given. The problem of fundamental frequency component error – either induced by the inherent fundamental switching period or due to the modulation by the voltage at the **far-end** of the injecting inductor is explained in Section 4.6.2. In Sections 4.6.3

to 4.6.11, the results obtained employing the three Schemes, for three set of system-parameters are given. The number of switchings and the performance parameters as defined in Section 4.4.2 are determined for comparison and are tabulated and the summarized.

4.6.1 Data used for the Simulation experiment

The novel switching schemes are tested for various cases and the results are presented in this Section. The system against which they are tested consists of, a voltage source, an ideal current source, and a VSI based current injector – which is switched by these Schemes. The set of parameters of the system and that of the schemes used for simulation are given in Table 4.4. The different cases are formed by changing R_S, L_S, Δi, L_1, and α, while maintaining the other variables and element values constant.

Table 4.4: Data used for the Simulation

Supply voltage $v_S(t)$	230 V, 50 Hz
$i_O(t)$	10 A, Square-wave, 20 ms period
α – delay angle	0° or -45° w.r.t $v_S(t)$, defined on the fundamental in $i_O(t)$
Frequency of sampling/switching	10 kHz
VSI source voltage V_{DC}	500 V
Inductance of Injecting Inductor, L_1	10 mH or 15 mH
Resistance of the Injecting Inductor, R_1	0.1 Ω
Hysteresis band Δi	±5% or ±10% (of $i_O(t)$)
Source side impedance	R_S = 150 mΩ, L_S = 500 μH or R_S = 250 mΩ, L_S = 2 mH
Commutating Inductor	R_R = 100 mΩ, L_R = 100 μH
Dummy Resistors	R_{D_1} and R_{D_2} are set to 1 MΩ each

4.6.2 An example to show the effect of far-end voltage on the periodically sampled hysteresis control implementation without far-end voltage information

The current injected is dependent on the differential voltage available across the injecting inductor. Thus it will be different for the two cases – one with zero **far-end** voltage and the other with non-zero **far-end** voltage. When the **far-end** voltage is varying,

determining the switching instants without considering it, will result in an excessive current at the modulating frequency of the differential voltage. This is demonstrated by comparing the current injected by the injecting-inductor for the two cases. Consider the circuit shown in Figure 4.1 and is repeated in Figure 4.8 for convenience.

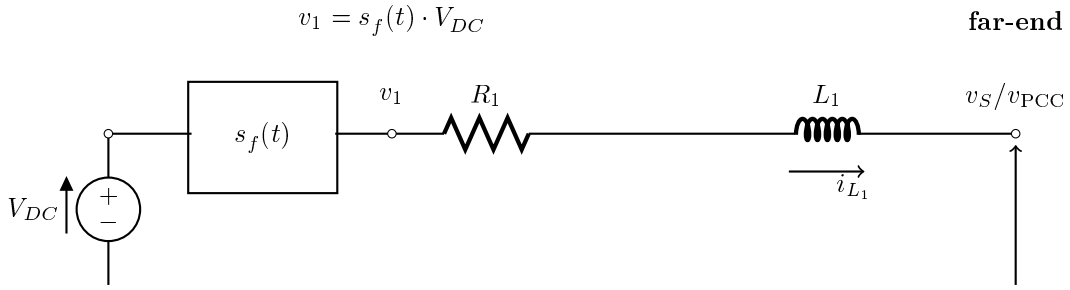

Figure 4.8: Circuit for demonstrating the effect of **far-end** voltage on the performance of the Basic hysteresis scheme

Let $v_S(t)$ is the **far-end** voltage and $v_1(t)$ is the controlled voltage source (output of the VSI, $v_1 = s_f(t) \cdot V_{DC}$, $s_f(t)$ – the switching function) and $\{R_1,\ L_1\}$ forms the injecting inductor. This circuit can be obtained to very close approximation from the circuit shown in Figure 4.3 by setting $i_O = 0$. Since R_{D_1} and R_{D_2} are very large it reduces to circuit shown in Figure 4.1, with the injecting-inductor $\{R_1,\ L_1\}$ here replaced by the series combination of $\{R_S,\ L_S\}$ and $\{R_1,\ L_1\}$ from there. Following set of values are chosen common to both cases – with zero and with non-zero **far-end** voltage.

R_S	L_S	L_1	Δi
150 mΩ	500 μH	10 mH	05

The results of simulation and analysis are presented in Figures 4.9 and 4.10 for the case with $v_S(t)$ set to zero or passivated.

It can be observed from Figure 4.10 that the fundamental component in the injected current is around 0.5 A, which is attributed to the fundamental frequency in the reference (modulating) signal. However it must be noted that the fundamental component in the reference current is zero.

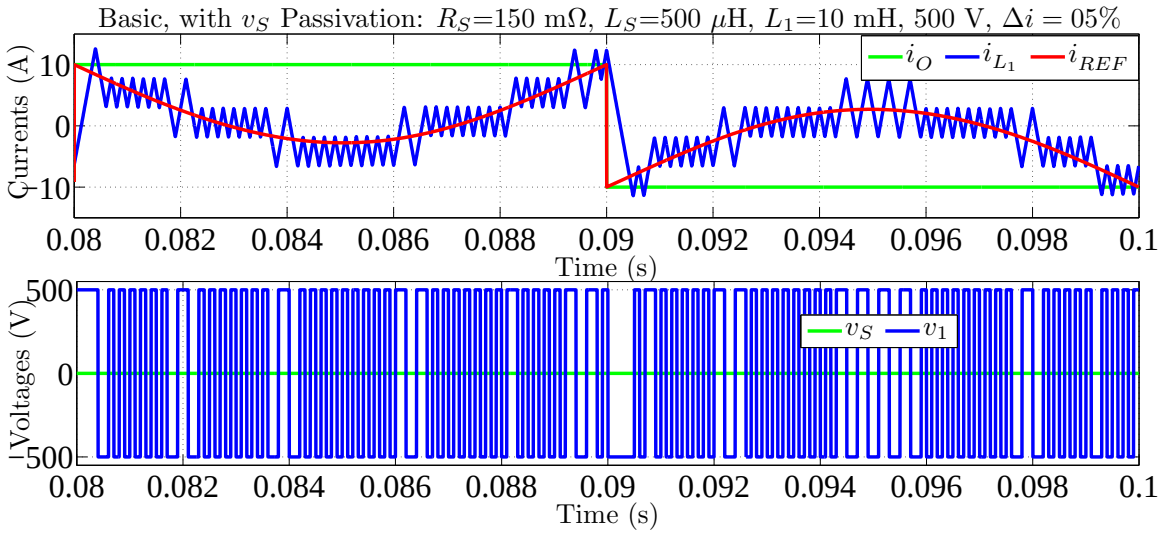

Figure 4.9: Time domain performance of the hysteresis switching technique – Basic Scheme, with **far-end** voltage source passivated, $v_S(t) = 0$

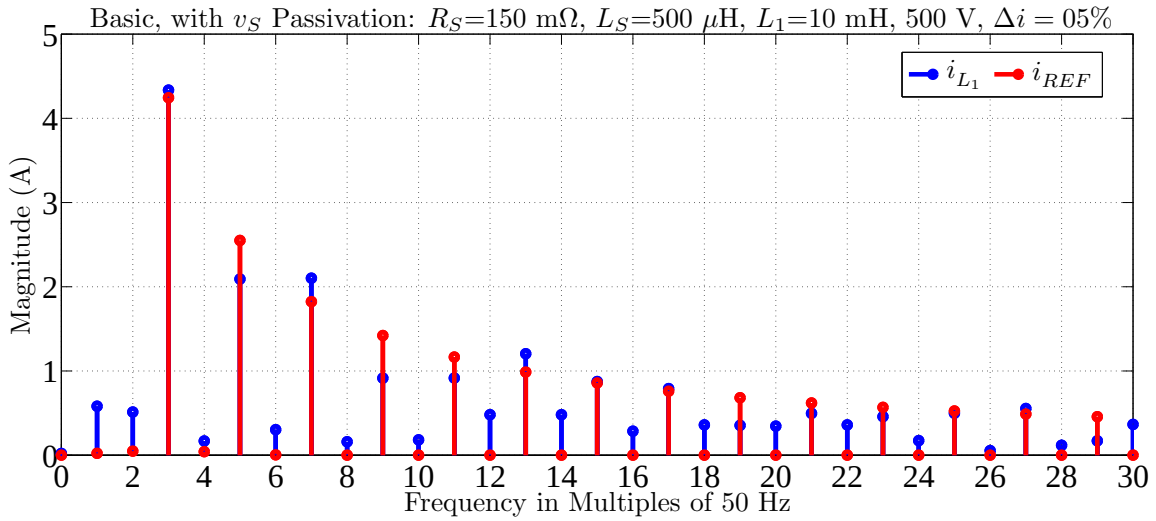

Figure 4.10: Frequency domain performance of the hysteresis switching technique – Basic Scheme, with **far-end** voltage passivated, $v_S(t) = 0$

In Figures 4.11 and 4.12 the results for the case with **far-end** voltage set to $v_S(t) = 230\sqrt{2}\sin(100\pi t)$ V, is given.

It may be observed that the fundamental component in the injected current is excessively large at 4.25 A and also there is a larger deviation in tracking for the other components as well. This is the usual trend in hysteresis control implemented without using the **far-end** voltage information. It can also be observed that the injected current may not posses half-wave symmetry and can contain even harmonics with considerable amount.

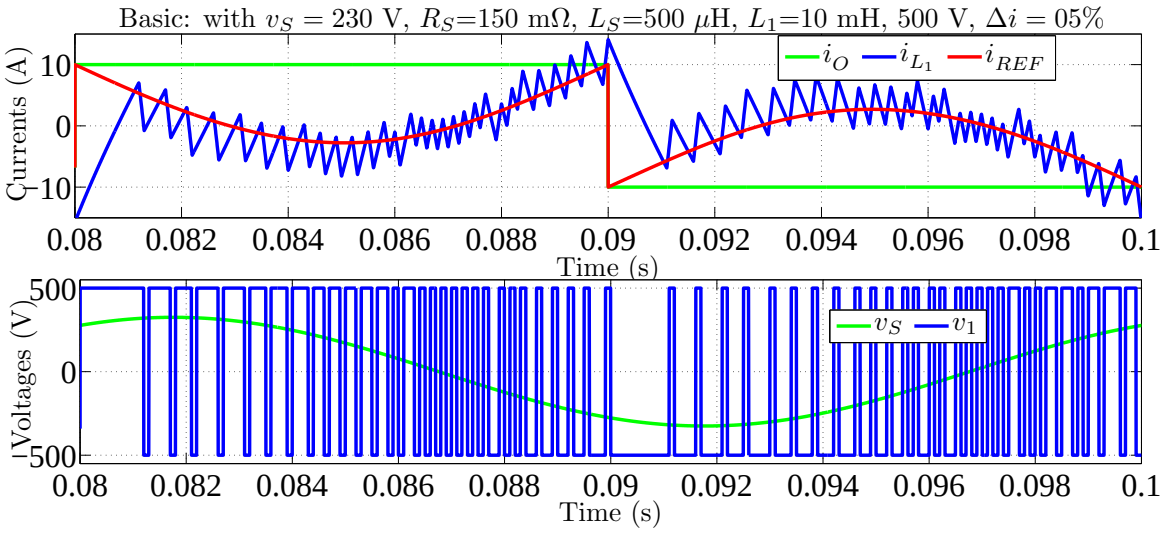

Figure 4.11: Time domain performance of the hysteresis switching technique – Basic Scheme, with **far-end** voltage – $v_S(t) = 230$ V

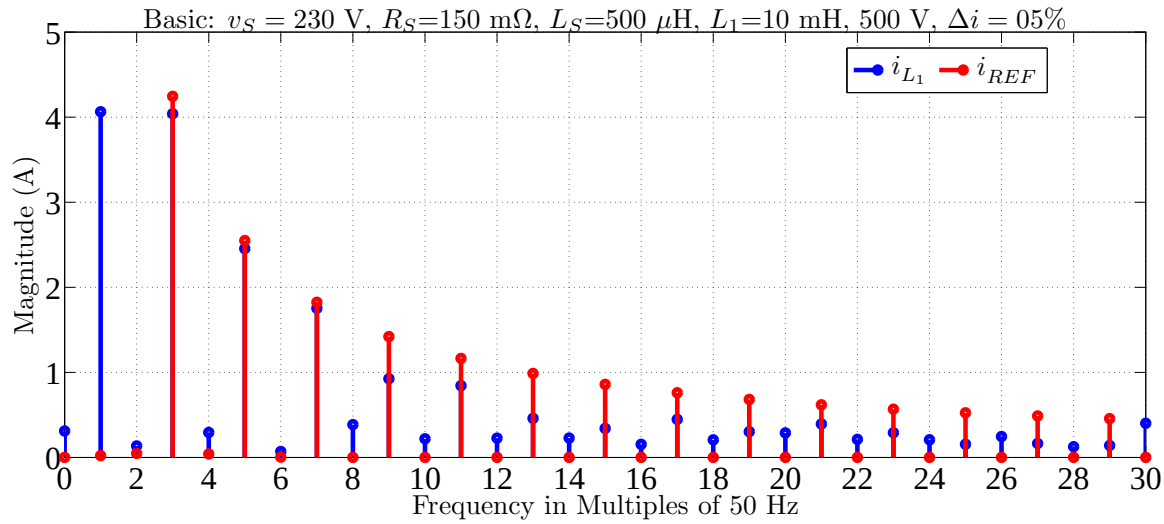

Figure 4.12: Frequency domain performance of the hysteresis switching technique – Basic Scheme, with **far-end** voltage – $v_S(t) = 230$ V

In the following results from simulation experiments for various cases on all the three schemes considered are presented.

4.6.3 Case-1: Basic Hysteresis control

Parameters considered:

R_S	L_S	α	L_1	Δi
150 mΩ	500 μH	0°	15 mH	10%

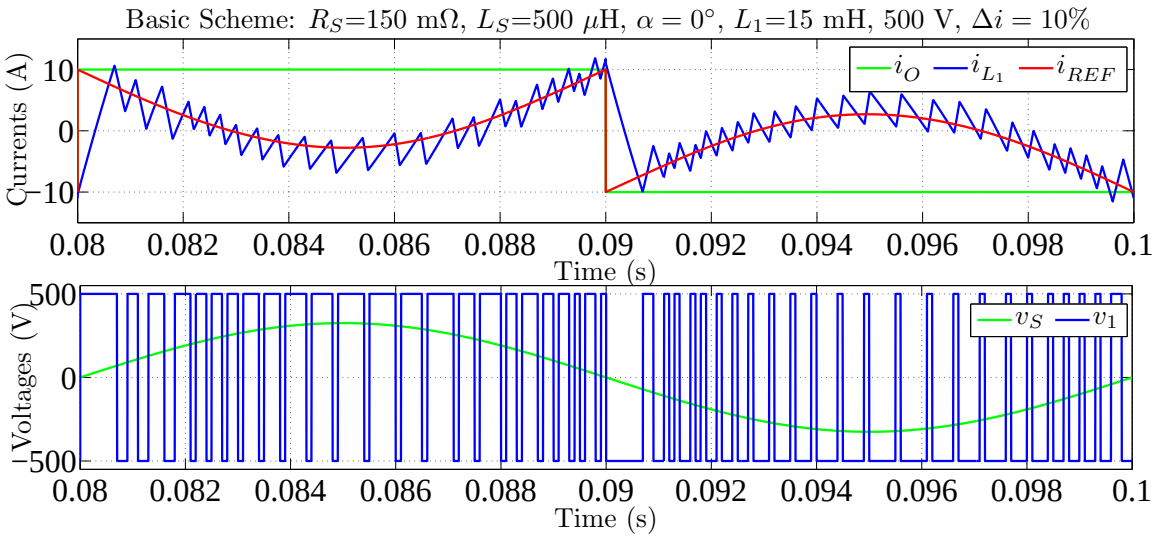

Figure 4.13: Time domain performance of the hysteresis switching technique –Case-1, Basic scheme

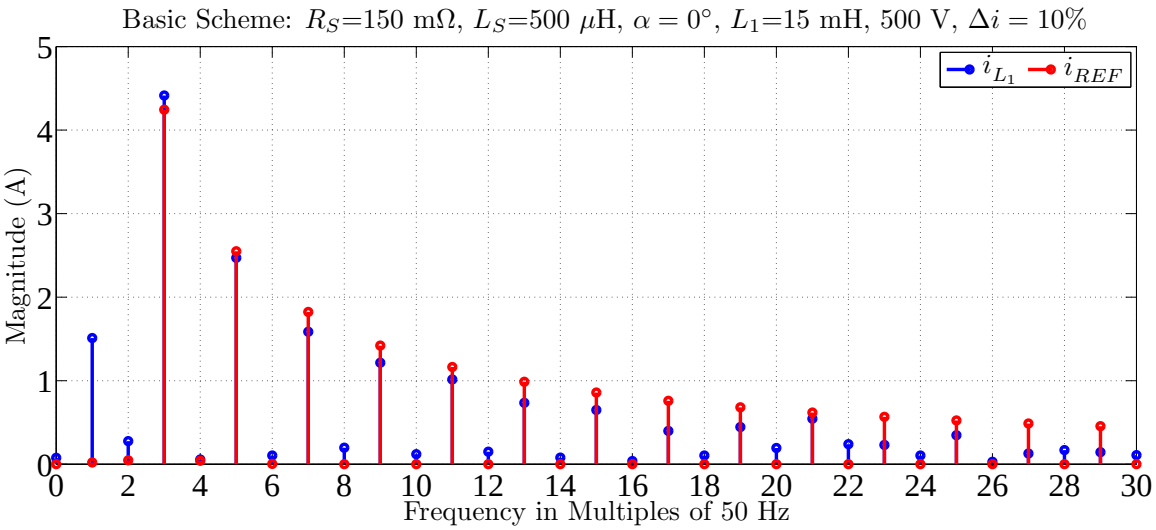

Figure 4.14: Frequency domain performance of the hysteresis switching technique – Case-1, Basic scheme

4.6.4 Case-1: Hysteresis control: Scheme-1

Parameters considered:

R_S	L_S	α	L_1	Δi
150 mΩ	500 μH	0°	15 mH	10%

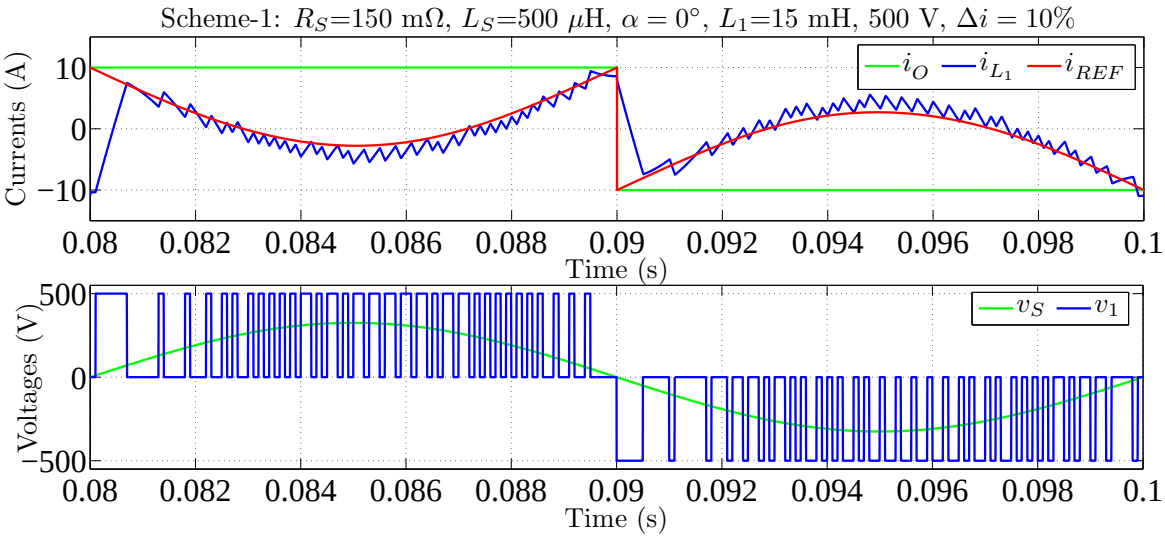

Figure 4.15: Time domain performance of the hysteresis switching technique –Case-1, Scheme-1

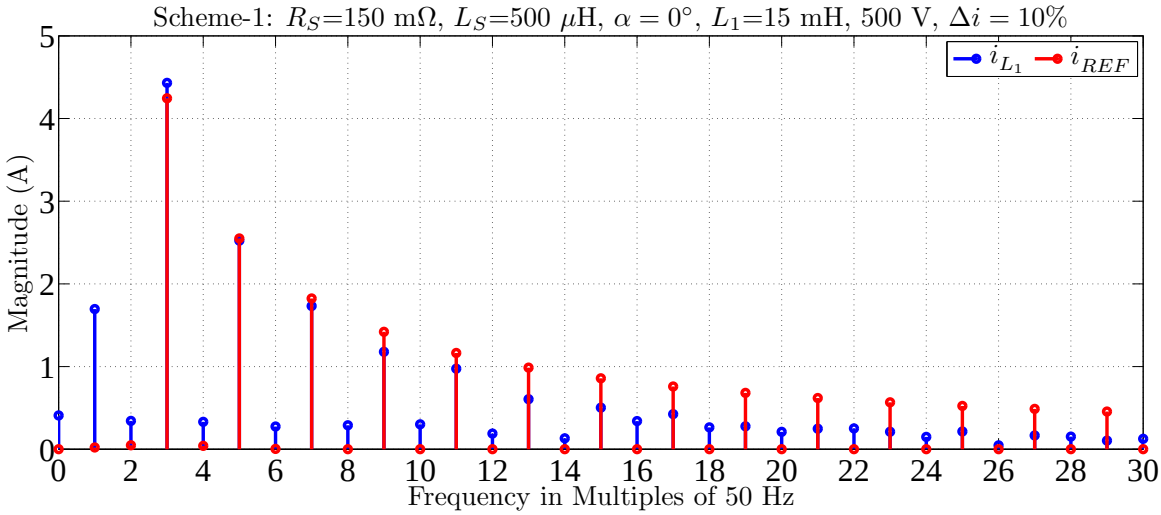

Figure 4.16: Frequency domain performance of the hysteresis switching technique – Case-1, Scheme-1

4.6.5 Case-1: Hysteresis control: Scheme-2

Parameters considered:

R_S	L_S	α	L_1	Δi
150 mΩ	500 μH	0°	15 mH	10%

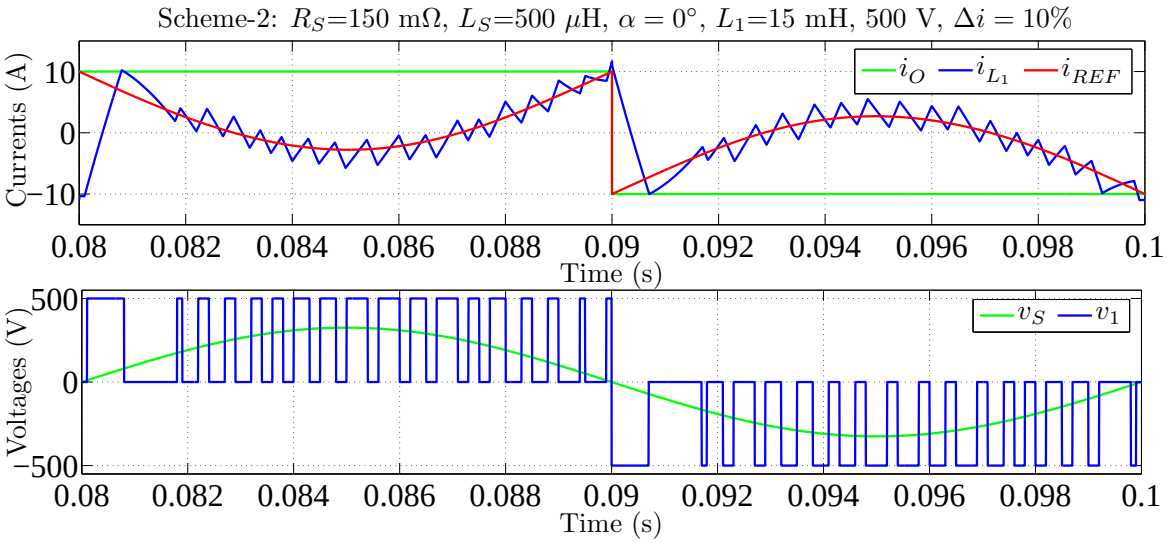

Figure 4.17: Time domain performance of the hysteresis switching technique –Case-1, Scheme-2

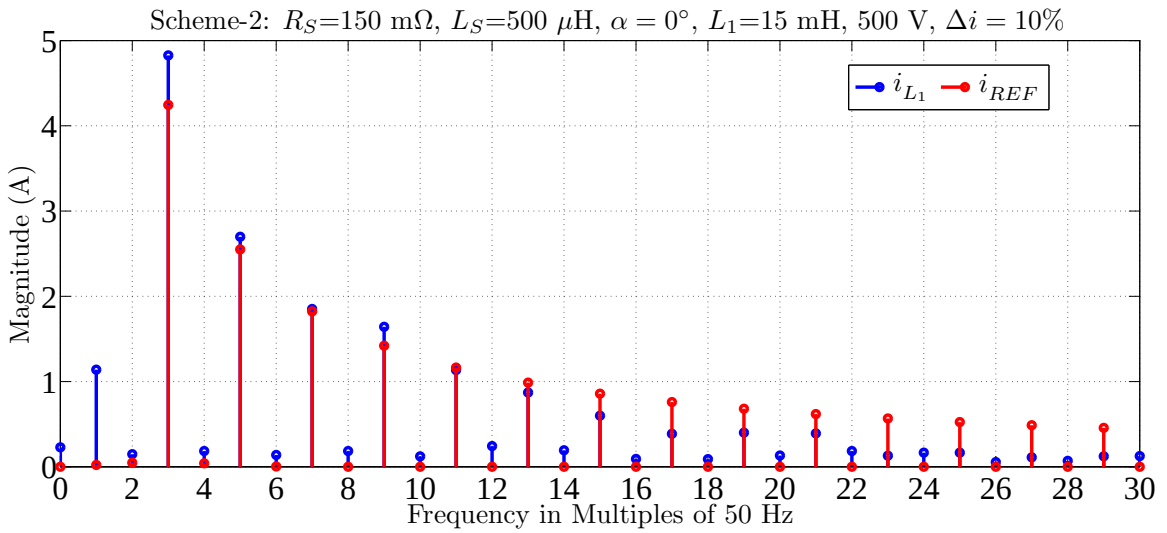

Figure 4.18: Frequency domain performance of the hysteresis switching technique – Case-1, Scheme-2

4.6.6 Case-2: Basic Hysteresis control

Parameters considered:

R_S	L_S	α	L_1	Δi
150 mΩ	500 μH	45°	10 mH	05%

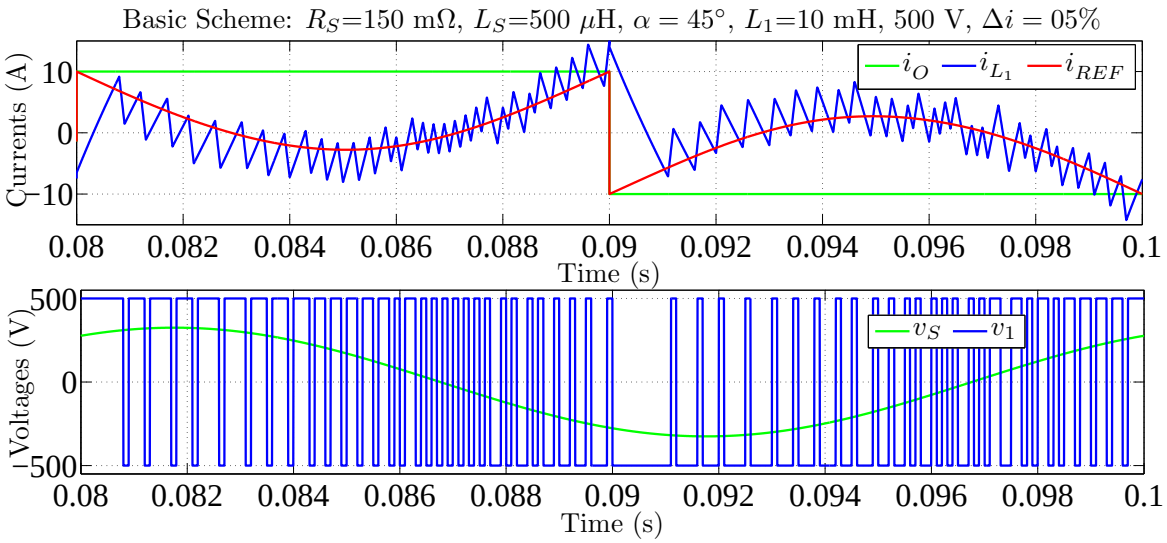

Figure 4.19: Time domain performance of the hysteresis switching technique –Case-2, Basic scheme

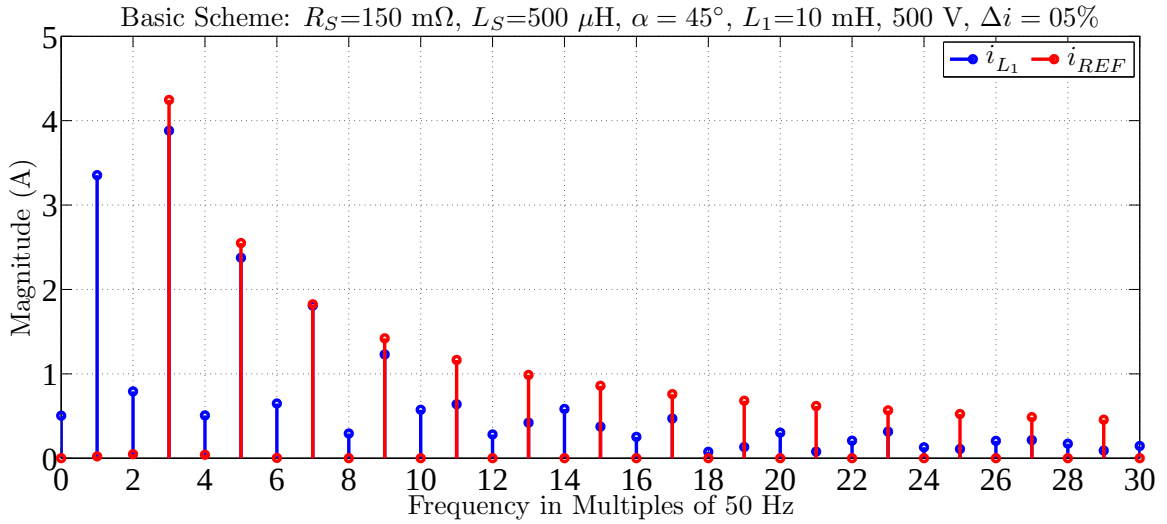

Figure 4.20: Frequency domain performance of the hysteresis switching technique – Case-2, Basic scheme

4.6.7 Case-2: Hysteresis control: Scheme-1

Parameters considered:

R_S	L_S	α	L_1	Δi
150 mΩ	500 μH	45°	10 mH	05%

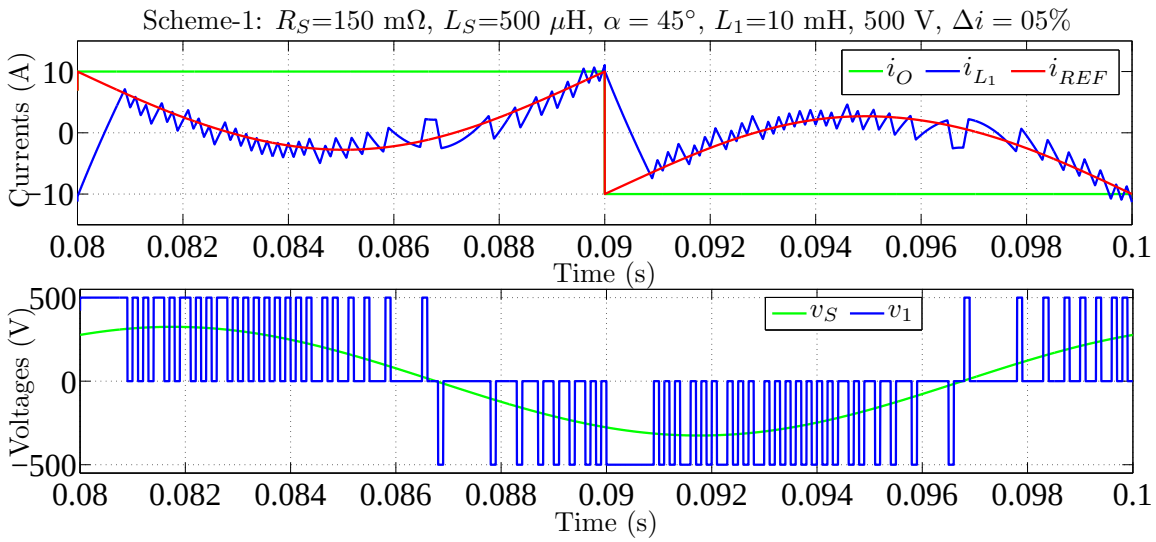

Figure 4.21: Time domain performance of the hysteresis switching technique –Case-2, Scheme-1

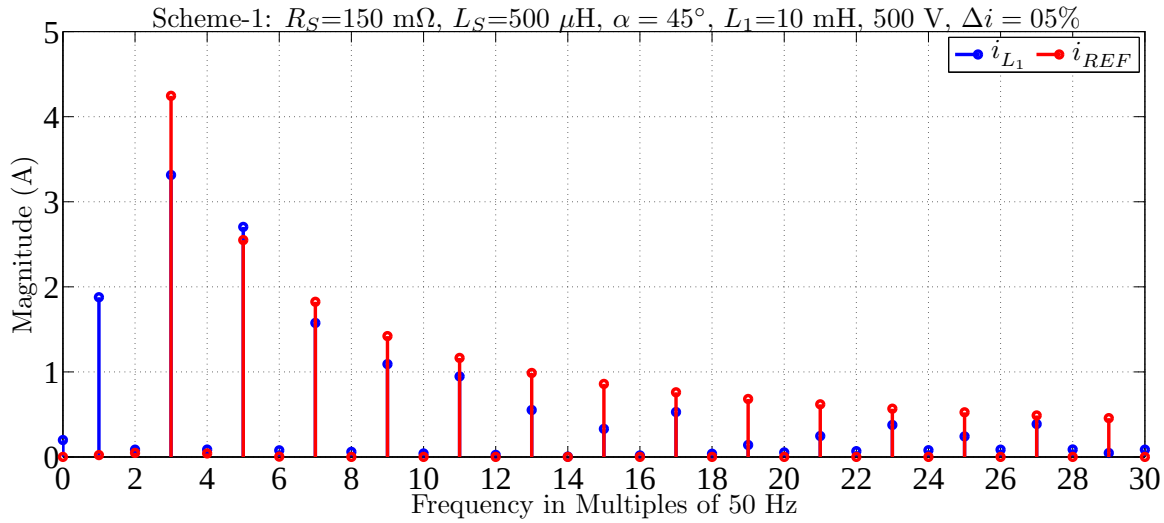

Figure 4.22: Frequency domain performance of the hysteresis switching technique – Case-2, Scheme-1

4.6.8 Case-2: Hysteresis control: Scheme-2

Parameters considered:

R_S	L_S	α	L_1	Δi
150 mΩ	500 μH	45°	10 mH	05%

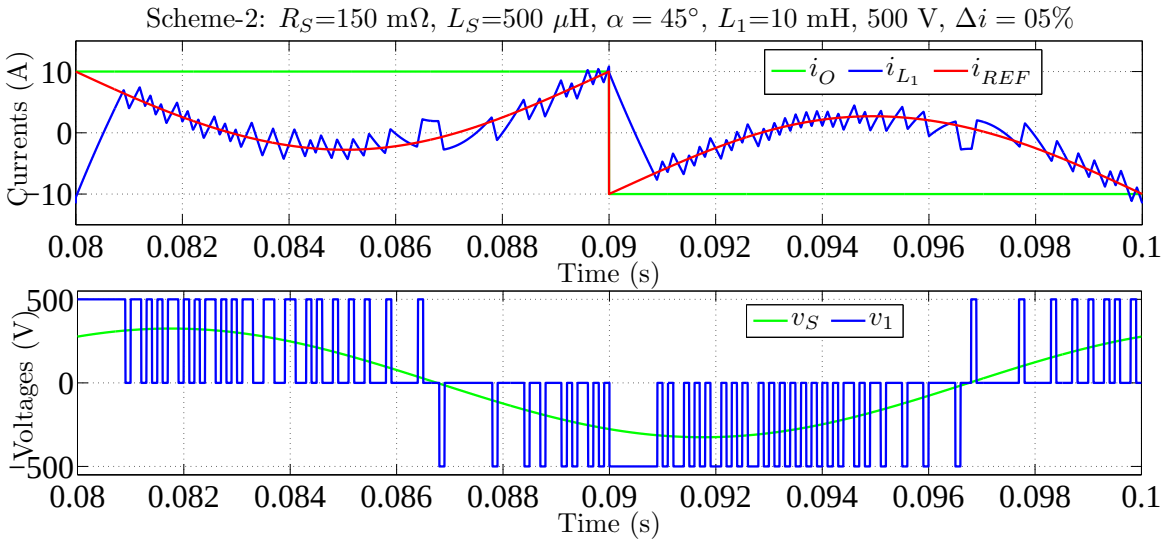

Figure 4.23: Time domain performance of the hysteresis switching technique –Case-2, Scheme-2

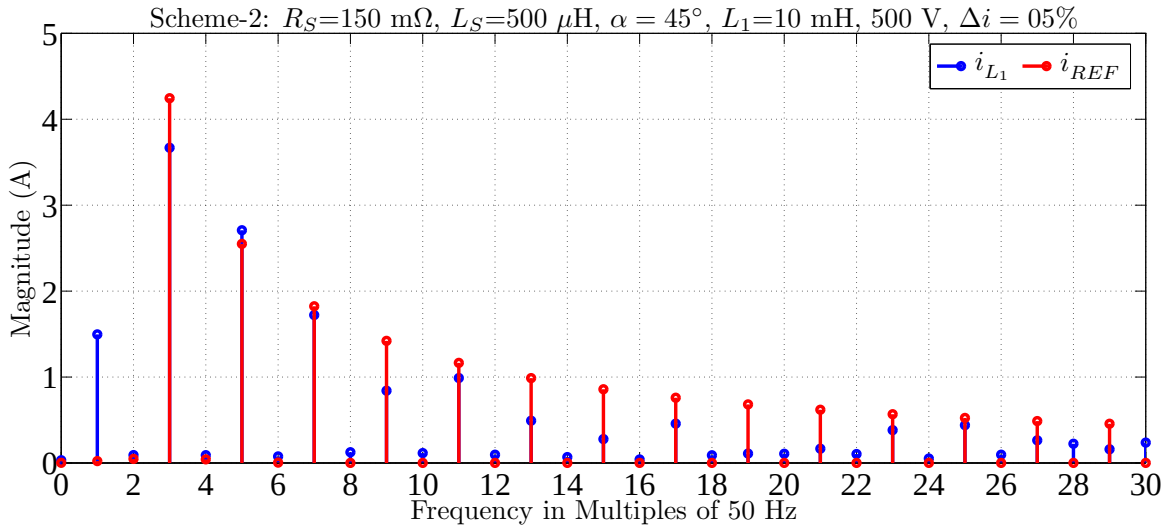

Figure 4.24: Frequency domain performance of the hysteresis switching technique – Case-2, Scheme-2

4.6.9 Case-3: Basic Hysteresis control

Parameters considered:

R_S	L_S	α	L_1	Δi
250 mΩ	2 mH	45°	15 mH	10%

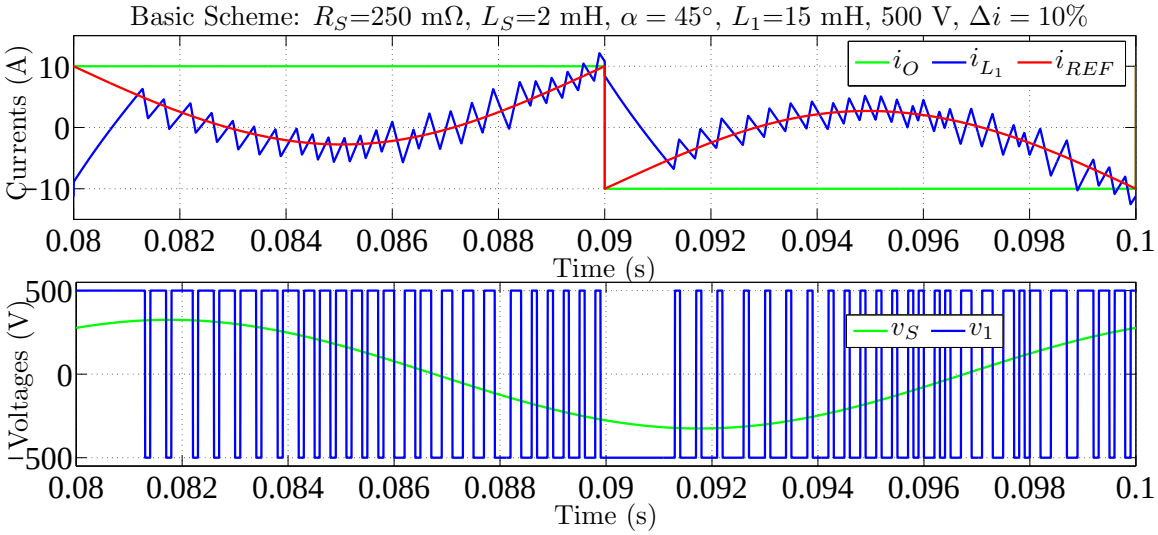

Figure 4.25: Time domain performance of the hysteresis switching technique –Case-3, Basic scheme

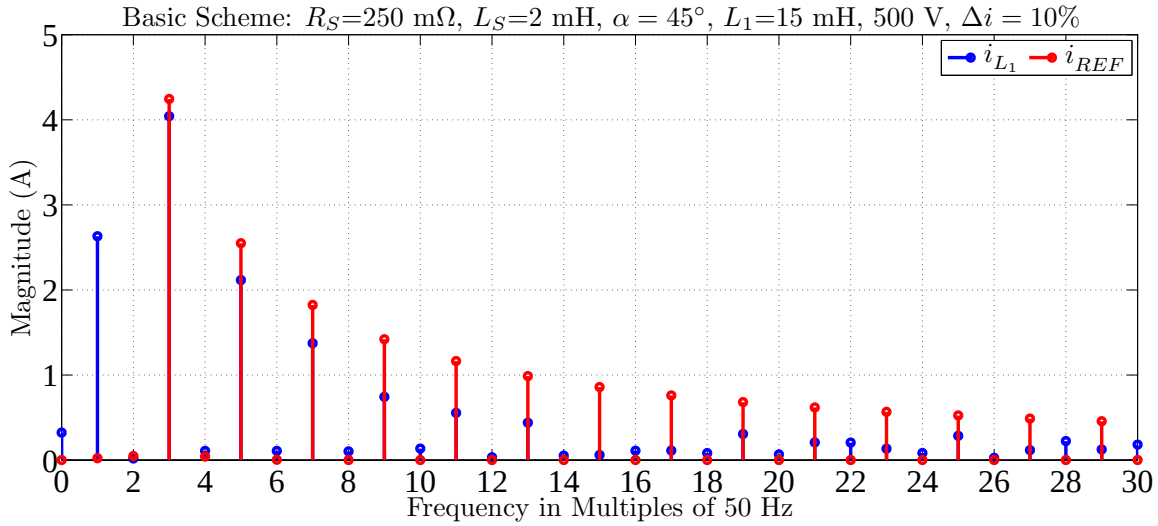

Figure 4.26: Frequency domain performance of the hysteresis switching technique – Case-3, Basic scheme

4.6.10 Case-3: Hysteresis control: Scheme-1

Parameters considered:

R_S	L_S	α	L_1	Δi
250 mΩ	2 mH	45°	15 mH	10%

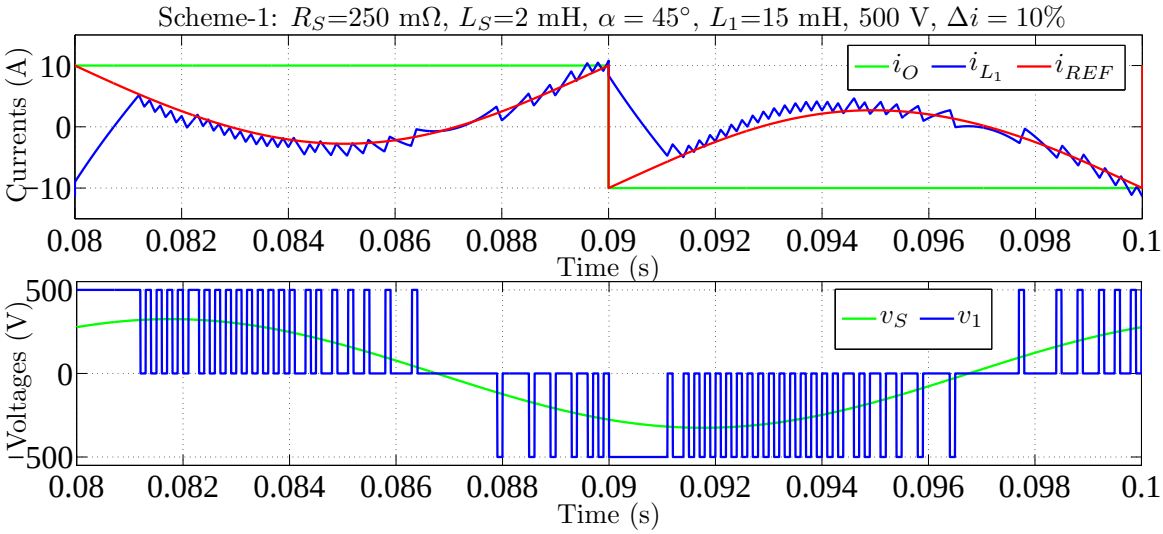

Figure 4.27: Time domain performance of the hysteresis switching technique –Case-3, Scheme-1

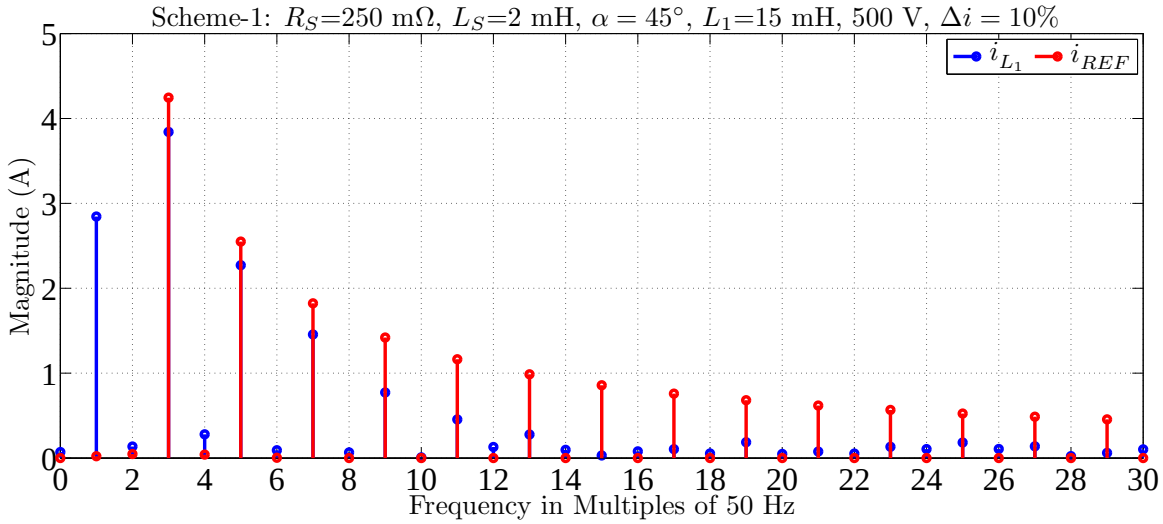

Figure 4.28: Frequency domain performance of the hysteresis switching technique – Case-3, Scheme-1

4.6.11 Case-3: Hysteresis control: Scheme-2

Parameters considered:

R_S	L_S	α	L_1	Δi
250 mΩ	2 mH	45°	15 mH	10%

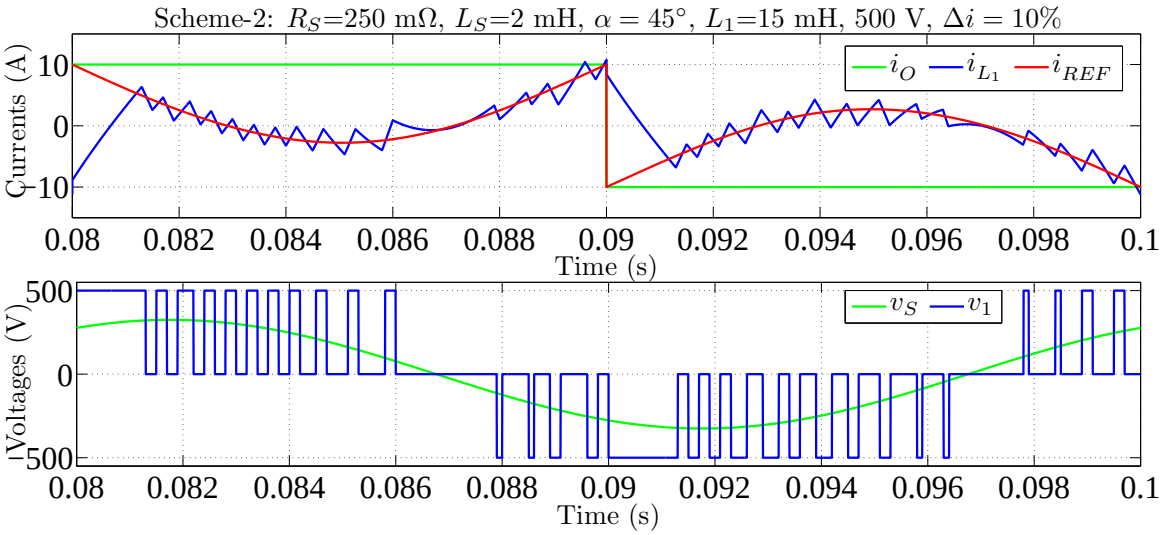

Figure 4.29: Time domain performance of the hysteresis switching technique –Case-3, Scheme-2

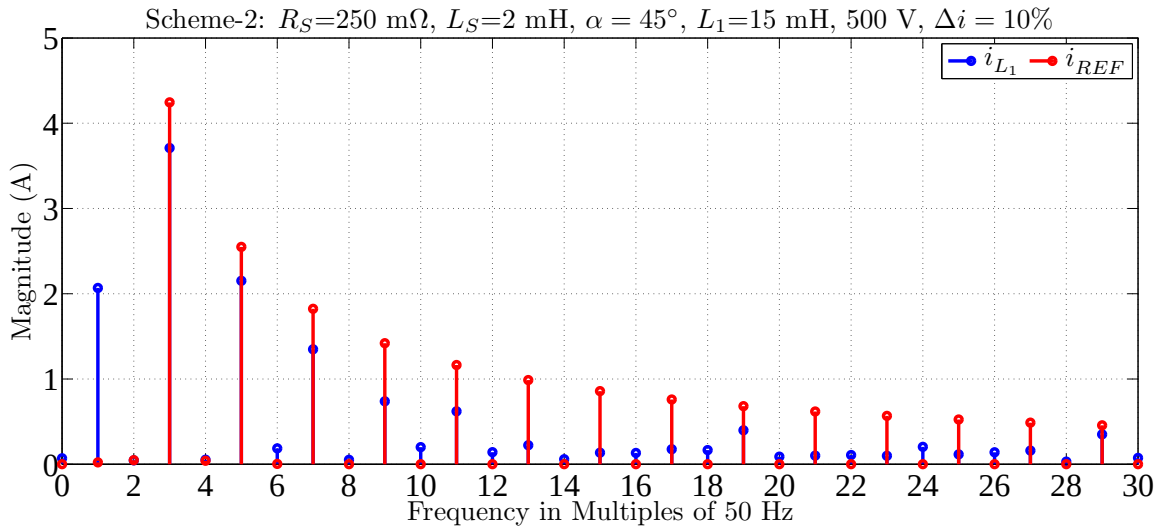

Figure 4.30: Frequency domain performance of the hysteresis switching technique – Case-3, Scheme-2

4.6.12 Summary of the Results

The performance parameters defined are determined for all the cases and the schemes considered. They are tabulated in Table 4.5.

Table 4.5: Summary of the results for the Novel Switching Principle

Case	Scheme	μ_ϵ	ϵ_{AR}	ϵ_{AB}	I_{DC}	I_{L_1}	S_C
Case-1	Basic	3.2214	-0.0379	1.7966	0.0385	1.5101	96
	Scheme-1	3.0759	-0.2035	1.5117	0.2041	1.6959	132
	Scheme-2	3.3957	-0.1135	1.7123	0.1141	1.1389	72
Case-2	Basic	4.1026	-0.2525	2.5244	0.2519	3.3545	126
	Scheme-1	3.5101	-0.0986	1.6960	0.0991	1.8769	124
	Scheme-2	3.4922	-0.0152	1.6497	0.0157	1.4960	112
Case-3	Basic	3.8095	-0.1608	2.0585	0.1613	2.6306	100
	Scheme-1	3.6982	-0.0353	1.7407	0.0359	2.8449	112
	Scheme-2	3.7076	-0.0343	1.7911	0.0349	2.0681	62

Following observations can made from this Table.

- that most important parameters like: ϵ_{AR}, I_{L_1}, and S_C are least for Scheme-2
- the measures: ϵ_{AB} and μ_ϵ are in the comparable ranges
- performance parameters for a given scheme vary very much for different cases, showing that the system parameters have a strong influence on the performance of the schemes
- in all cases the constant component is negative for all schemes considered

Considering the fact that the number of switchings per cycle and the fundamental in injected current are small it proves that Scheme-2 has good desirable characteristics.

4.7 Conclusions

A **far-end** voltage information incorporated multi-criteria based hysteresis control concept is introduced. The significance of the influence of the **far-end** voltage on the injected current as modulated by that voltage is illustrated in the beginning. This concept can lead to many techniques. In this thesis two schemes with different switching rules are implemented and compared with the basic hysteresis control. The performance parameters for comparison are defined. The following observations are presented:

- The illustration showed that the **far-end** voltage has significant modulation influence on the injected current.
- The **far-end** voltage being the utility supply voltage, the large fundamental current circulated affects the performance of the Active Power Filter.
- It is found that the Scheme-2 as referred has very good performance parameters like: minimum number of switchings per fundamental cycle, smallest fundamental amplitude as well as the constant component in the injected current.
- The switching count is important considering the switching stress on the devices and also the EMI problems because of the traverse of the pole voltage.
- Since the fundamental component in the injected current is smaller, tracking will be better and faster, because it depends relatively lesser on the supervisory controller.

Chapter 5

Power-Shield – Modeling and Simulation

5.1 Introduction

Current-source type of nonlinear loads need a detailed study to arrive at an appropriate topology that will impede it infiltrating with current harmonics into the upstream side from the PCC and that will minimise the distortion of voltage at the PCC. A general structure with a series element (passive and/or active) and a shunt element (shunt passive filter and/or a shunt active filter) are included for study. A detailed study is carried out to discover the appropriate topology (termed as Power-Shield henceforth) and to find justifications thereof. Thus in Section 5.2, the basis for the choice of the simulation strategy, and the objectives of simulation are explained. In the light of some of the difficulties observed in the standard packages for simulation, the complete power circuit system is modeled in state-space and implemented in MATLAB®/Simulink®. The development of the model is explained in Section 5.3. The design of different components of the Power-Shield is briefly discussed in Section 5.4. The simulation setup is explained in Section 5.6. The simulation studies are conducted for various cases and the results are presented in Sections 5.7 through 5.9. Conclusions are drawn based on the simulation results justifying the choice of the topology for Power-Shield – one of the main focus of the study for the current-source type of nonlinear loads. They are presented in Section 5.11.

5.2 Simulation: Platform, Strategy, and objectives

5.2.1 Basis for the choice of the Platform

A survey of some of the commercially available packages for simulation of a switched electric circuit is carried out. It was found that most of the packages did not give consistent results to some of the test circuits, for which simple analytical solutions can be obtained. The functionality of various components used in the packages is not reliable. For example, a two-winding transformer has to function as a transformer, whether excited by a voltage source or a current source, on any one or both of the windings. The transformer models in the standard packages are based on turns ratio and in some packages are suited for sinusoidal steady-state operation only. On the other hand the detailed switching device models used in most of the packages result in simulation difficulties; such a detailed model is not a necessity in the search for a topology. It is also to be noted that the model parameters to be chosen in the packages being empirical and are difficult to determine through experiments in the laboratory. Since the reliability of the simulation result is of paramount importance for the current study, the mathematical modeling from the first principles is used, in spite of being tedious and laborious. The model equations are coded in MATLAB®/Simulink®.

5.2.2 Simulation Strategy adopted

A model based on state-space approach [Balabanian and Bickart(1969)], [Mendalek and Al-Haddad(2003), Bina and Bhat(2008)] is obtained and is implemented in MATLAB®/Simulink®. A state-variable-dependent switching-function is developed to turn-ON or turn-OFF the rectifier devices, in either continuous current mode of operation or discontinuous mode of operation. The model simulated is very general with 16 state-variables. Most of the resistances can be made to act as artifices and hence several combinations of the filtering and compensation can be simulated and performance evaluated. It is also very reliable, general, and flexible. When we take up mathematical modeling approach to switched-circuit simulation all the flexibility needed to change the topology must be incorporated in the very beginning. A single system of equations is developed to represent all possible combinations of the topology. Few features of the model are listed below:

- State-space based model is developed.
- Freedom preserving model is adopted (number of state variables is fixed).
- Dependent-Switching function based approach is used for the SCR based fully-controlled rectifier feeding the load, which can operate either in continuous cur-

rent conduction mode (CCM) or discontinuous current mode (DCM), whereas the shunt current injector or the series voltage injector are of VSI type – which are independently switched.

- Appropriate artifices (in the form of parallel or series resistors) are included in the circuit to control the inclusion or the exclusion of any of the components to alter the topology. Some artifices in the form of large resistances are used to serve the purpose of eliminating the all-inductor-current-source cut-sets, which is required for convergence in simulation.

5.2.3 Objective of the simulation setup

The main objective of the simulation is to obtain a topology for the Power-Shield. However it is achieved through a systematic study by meeting several sub-objectives. They are, to:

- test the compensating signal extraction algorithms for their effectiveness
- test effectiveness of the multifunction capability of the possibilities of the technology available.
- conduct a study on the type of compensation (topology) suitable for Current-Source type of nonlinear loads (by changing the settings of the artifices different combinations can be obtained and a comparison can be made).
- check if a series impedance and/ or source may be a better alternative than the shunt compensation, given the source has very low impedance.
- Or a right-shunt is better or a left-shunt, when series compensation is used.
- study the effect of the commutating inductance of the rectifier on the filtering requirement and the load, and for optimally designing it.
- study the effect of signal used for PLL on the operation, control, and performance of the chosen topology.
- To compare the results from simulation with the experimental results

5.3 Development of the model of the Power-Shield

The circuit considered in this study is shown in Figure 5.1.

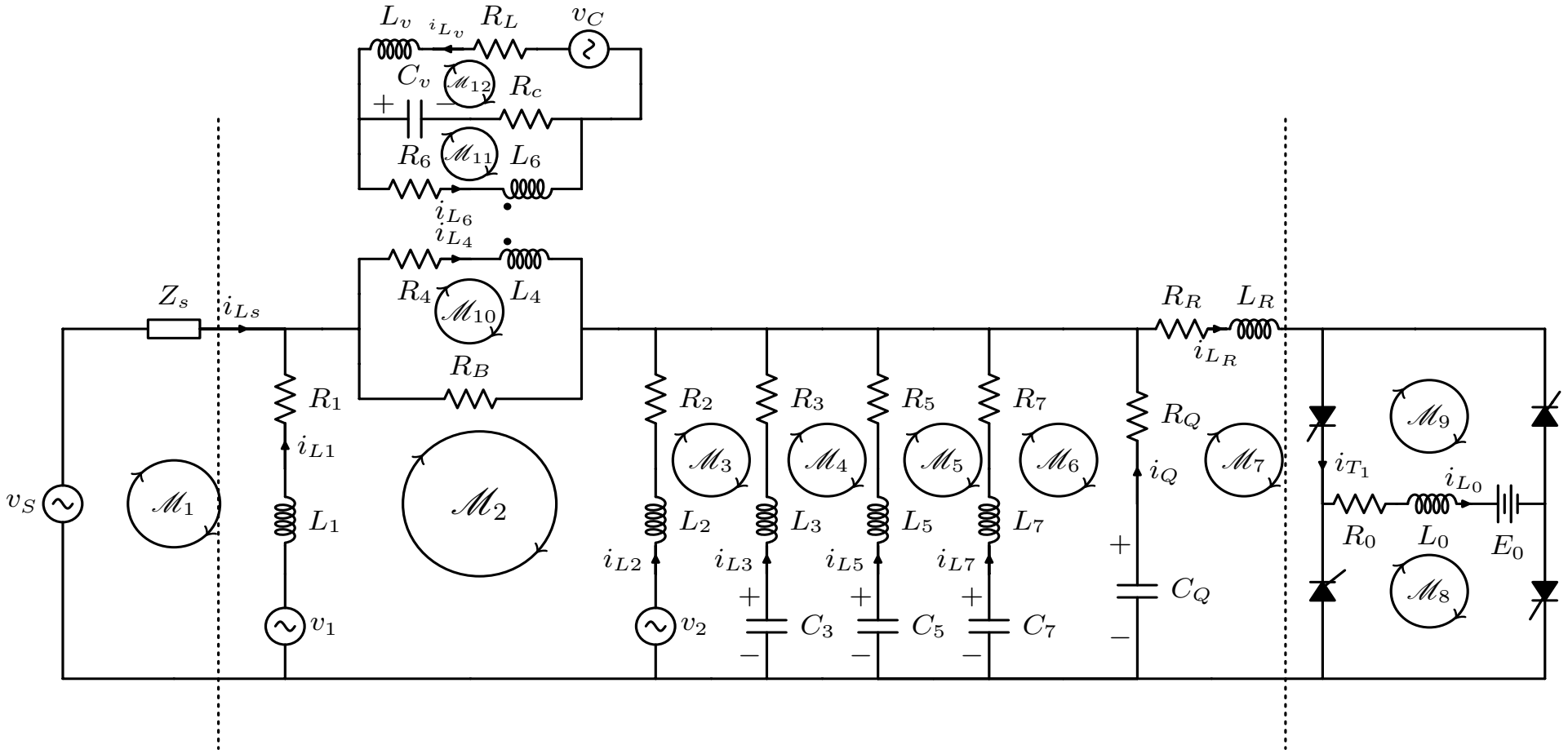

Figure 5.1: The Topology Considered for Implementation with marking of loops and nodes, to facilitate writing of system equations

5.3.1 Modeling of the multifunction topology

State-vector for inductors' currents,

$$\mathbf{i_L} = \begin{bmatrix} i_{L_4} & i_{L_6} & i_{L_S} & i_{L_1} & i_{L_v} & i_{L_2} & i_{L_3} & i_{L_5} & i_{L_7} & i_{L_R} & i_{L_O} \end{bmatrix}^T. \tag{5.1}$$

State-vector for capacitors' voltages

$$\mathbf{v_C} = \begin{bmatrix} v_{C_v} & v_{C_3} & v_{C_5} & v_{C_7} & v_{C_Q} \end{bmatrix}^T. \tag{5.2}$$

And the complete state-vector is $\mathbf{x} = [\mathbf{i_L^T v_C^T}]^\mathbf{T}$.

The Voltage Current Relations (VCR) for the inductors:

$$v_{L_4} = L_4 \frac{d}{dt} i_{L_4} + M \frac{d}{dt} i_{L_6} \tag{5.3}$$

$$v_{L_6} = L_6 \frac{d}{dt} i_{L_6} + M \frac{d}{dt} i_{L_4} \tag{5.4}$$

$$v_{L_k} = L_k \frac{d}{dt} i_{L_k} \quad \forall \text{ other } k - \text{stands for an } \boldsymbol{alpha-numeric} \text{ index} \tag{5.5}$$

where M $= \kappa\sqrt{L_4 L_6}$, with κ – the coupling coefficient of the series transformer, which is close to unity for transformers. It can be expressed in matrix form in short as follows:

$$\mathbf{v_L} = \begin{bmatrix} \mathbf{L} \end{bmatrix} \frac{d}{dt} \mathbf{i_L}. \tag{5.6}$$

Here the inductance matrix for the coupled coils L_C is,

$$L_C = \begin{bmatrix} L_4 & M \\ M & L_6 \end{bmatrix} \tag{5.7}$$

where suffix 'C' stands for coupled coils and the corresponding levitance matrix is,

$$\Gamma_C = \begin{bmatrix} \dfrac{L_6}{L_4 L_6 - M^2} & \dfrac{-M}{L_4 L_6 - M^2} \\ \dfrac{-M}{L_6 L_4 - M^2} & \dfrac{L_4}{L_4 L_6 - M^2} \end{bmatrix} = \begin{bmatrix} \Gamma_4 & \Gamma_{46} \\ \Gamma_{64} & \Gamma_6 \end{bmatrix}. \tag{5.8}$$

The VCR for the capacitors:

$$i_{C_k} = C_k \frac{d}{dt} v_{C_k} \tag{5.9}$$

It can be expressed as,

$$\mathbf{i_C} = \Big[\mathbf{C}\Big] \frac{d}{dt} \mathbf{v_C}. \tag{5.10}$$

The VCR equations for Resistances (R) in series with the inductors:

$$v_{R_k} \;=\; R_k \, i_{R_k}. \tag{5.11}$$

The VCR equations for Conductances (G) in shunt with the capacitors:

$$i_{G_k} \;=\; G_k \, v_{G_k}. \tag{5.12}$$

In short form, for a system of Rs and Gs,

$$\mathbf{v_R} = \Big[\mathbf{R}\Big] \, \mathbf{i_R} \tag{5.13}$$

and

$$\mathbf{i_G} = \Big[\mathbf{G}\Big] \, \mathbf{v_G}. \tag{5.14}$$

Then element VCR equations for the energy storage elements,

$$\begin{bmatrix} \mathbf{v_L} \\ \mathbf{i_C} \end{bmatrix} = \begin{bmatrix} \mathbf{L} & \mathbf{0} \\ \mathbf{0} & \mathbf{C} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C}. \end{bmatrix}. \tag{5.15}$$

And hence,

$$\frac{d}{dt} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} = \begin{matrix} 11 \\ 5 \end{matrix} \overset{\begin{matrix} 11 & \quad 5 \end{matrix}}{\begin{bmatrix} \mathbf{\Gamma} & \mathbf{0} \\ \mathbf{0} & \mathbf{C^{-1}} \end{bmatrix}} \begin{bmatrix} \mathbf{v_L} \\ \mathbf{i_C} \end{bmatrix} \tag{5.16}$$

where $\mathbf{\Gamma} = \mathbf{L}^{-1}$ is the system levitance matrix, which is block diagonal and $\mathbf{C^{-1}}$ is the system elastance matrix, which is diagonal with elements ${C^{-1}}_{kk} = \dfrac{1}{C_k}$. The detailed representation of system (5.16) is given in (5.17),

$$\frac{d}{dt}\begin{bmatrix} i_{L_4} \\ i_{L_6} \\ i_{L_S} \\ i_{L_1} \\ i_{L_v} \\ i_{L_2} \\ i_{L_3} \\ i_{L_5} \\ i_{L_7} \\ i_{L_R} \\ i_{L_O} \\ v_{C_v} \\ v_{C_3} \\ v_{C_5} \\ v_{C_7} \\ v_{C_Q} \end{bmatrix} = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \\ 15 \\ 16 \end{array} \begin{array}{c} \begin{array}{cccccccccccccccc} i_{L_4} & i_{L_6} & i_{L_S} & i_{L_1} & i_{L_v} & i_{L_2} & i_{L_3} & i_{L_5} & i_{L_7} & i_{L_R} & i_{L_O} & v_{C_v} & v_{C_3} & v_{C_5} & v_{C_7} & v_{C_Q} \end{array} \\ \begin{bmatrix} \Gamma_4 & \Gamma_{46} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \Gamma_{64} & \Gamma_6 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \Gamma_S & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \Gamma_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \Gamma_v & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \Gamma_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \Gamma_3 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \Gamma_5 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \Gamma_7 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \Gamma_R & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \Gamma_O & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_v^{-1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_3^{-1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_5^{-1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_7^{-1} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_Q^{-1} \end{bmatrix} \end{array} \begin{bmatrix} i_{L_4} \\ i_{L_6} \\ i_{L_S} \\ i_{L_1} \\ i_{L_v} \\ i_{L_2} \\ i_{L_3} \\ i_{L_5} \\ i_{L_7} \\ i_{L_R} \\ i_{L_O} \\ v_{C_v} \\ v_{C_3} \\ v_{C_5} \\ v_{C_7} \\ v_{C_Q} \end{bmatrix}. \tag{5.17}$$

Let the vector of input quantities be, $\mathbf{u} \triangleq [v_s, v_1, v_2, v_C, E_O]^T$. The $\mathbf{v_L}$ and $\mathbf{i_C}$ are expressed in terms of the state-variables by applying the Kirchhoff's Voltage- and Current relations (i.e., by mesh equations (KVR – Kirchhoff's Voltage Relation) and node equations (KCR – Kirchhoff's Current Relation)) to the circuit. The variable and parameters are as indicated in the circuit diagram in Figure 5.1. R_P and R_N represent the resistance of the positive and negative group of Thyristors, the values of which are dependent on the state of the Thyristors, being ON (when it is set to $R_{ON} = 0.1\ \Omega$) or OFF (when it is set to $R_{OFF} = 1\ \mathrm{M}\Omega$). Below given are the mesh equations for the meshes $\mathscr{M}_1 - \mathscr{M}_{12}$:

$$
\begin{aligned}
\text{Mesh- } \mathscr{M}_1 : \quad & v_s - R_s i_{L_S} - v_{L_S} + R_s i_{L_1} + v_{L_1} - v_1 && = 0 \\
\text{Mesh- } \mathscr{M}_2 : \quad & v_1 - v_{L_1} - R_1 i_{L_1} - R_B(i_{L_S} + i_{L_1} - i_{L_4}) + R_2 i_{L_2} + v_{L_2} - v_2 && = 0 \\
\text{Mesh- } \mathscr{M}_3 : \quad & v_2 - v_{L_2} - R_2 i_{L_2} + R_3 i_{L_3} + v_{L_3} - v_{C_3} && = 0 \\
\text{Mesh- } \mathscr{M}_4 : \quad & v_{C_3} - v_{L_3} - R_3 i_{L_3} + R_5 i_{L_5} + v_{L_5} - v_{C_5} && = 0 \\
\text{Mesh- } \mathscr{M}_5 : \quad & v_{C_5} - v_{L_5} - R_5 i_{L_5} + R_7 i_{L_7} + v_{L_7} - v_{C_7} && = 0 \\
\text{Mesh- } \mathscr{M}_6 : \quad & v_{C_7} - v_{L_7} - R_7 i_{L_7} + R_Q(i_{L_R} - i_{L_S} - i_{L_1} - i_{L_2} - i_{L_3} - i_{L_5} - i_{L_7}) - v_{C_Q} && = 0 \\
\text{Mesh- } \mathscr{M}_7 : \quad & v_{C_Q} - R_Q(i_{L_R} - i_{L_S} - i_{L_1} - i_{L_2} - i_{L_3} - i_{L_5} - i_{L_7}) - R_R i_{L_R} - v_{L_R} \\
& \qquad - R_P i_{T_1} - R_N(i_{T_1} - i_{L_O}) && = 0 \\
\text{Mesh- } \mathscr{M}_8 : \quad & R_N(i_{T_1} - i_{L_O}) - R_O i_{L_O} - v_{L_O} - E_O - R_P(i_{L_O} + i_{L_R} - i_{T_1}) && = 0 \\
\text{Mesh- } \mathscr{M}_9 : \quad & R_P i_{T_1} - R_N(i_{L_R} - i_{T_1}) + E_O + v_{L_O} + R_O i_{L_O} && = 0 \\
\text{Mesh-}\mathscr{M}_{10} : \quad & -R_4 i_{L_4} - v_{L_4} + R_B(i_{L_S} + i_{L_1} - i_{L_4}) && = 0 \\
\text{Mesh-}\mathscr{M}_{11} : \quad & -v_{C_v} - R_C(i_{L_v} - i_{L_6}) + v_{L_6} + R_6 i_{L_6} && = 0 \\
\text{Mesh-}\mathscr{M}_{12} : \quad & v_{L_v} + R_L i_{L_v} - v_C + R_C(i_{L_v} - i_{L_6}) + v_{C_v} && = 0.
\end{aligned}
$$

These mesh equations are solved and expressed in matrix form to give,

$$
\left[\mathbf{v_L}\right] = \begin{bmatrix} \widehat{\mathbf{A}}_{\mathbf{11}} & \widehat{\mathbf{A}}_{\mathbf{12}} \end{bmatrix} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} + \left[\widehat{\mathbf{B}}_{\mathbf{1}}\right] \mathbf{u} \tag{5.18}
$$

where,

$$\left[\widehat{\mathbf{A}}_{\mathbf{11}}\right] = \begin{array}{c} \\ v_{L_4} \\ v_{L_6} \\ v_{L_S} \\ v_{L_1} \\ v_{L_V} \\ v_{L_2} \\ v_{L_3} \\ v_{L_5} \\ v_{L_7} \\ v_{L_R} \\ v_{L_O} \end{array} \begin{array}{c} \begin{array}{ccccccccccc} i_{L_4} & i_{L_6} & i_{L_S} & i_{L_1} & i_{L_v} & i_{L_2} & i_{L_3} & i_{L_5} & i_{L_7} & i_{L_R} & i_{L_O} \end{array} \\ \left[\begin{array}{ccccccccccc} -R_{4B} & 0 & R_B & R_B & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -R_{C6} & 0 & 0 & R_C & 0 & 0 & 0 & 0 & 0 & 0 \\ R_B & 0 & -R_{QBS} & -R_{QB} & 0 & -R_Q & -R_Q & -R_Q & -R_Q & R_Q & 0 \\ R_B & 0 & -R_{QB} & -R_{1QB} & 0 & -R_Q & -R_Q & -R_Q & -R_Q & R_Q & 0 \\ 0 & R_C & 0 & 0 & -R_{LC} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -R_Q & -R_Q & 0 & -R_{2Q} & -R_Q & -R_Q & -R_Q & R_Q & 0 \\ 0 & 0 & -R_Q & -R_Q & 0 & -R_Q & -R_{3Q} & -R_Q & -R_Q & R_Q & 0 \\ 0 & 0 & -R_Q & -R_Q & 0 & -R_Q & -R_Q & -R_{5Q} & -R_Q & R_Q & 0 \\ 0 & 0 & -R_Q & -R_Q & 0 & -R_Q & -R_Q & -R_Q & -R_{7Q} & R_Q & 0 \\ 0 & 0 & R_Q & R_Q & 0 & R_Q & R_Q & R_Q & R_Q & -(R_{RQ}+\frac{R}{2}) & R_N-\frac{R}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_N-\frac{R}{2} & -(R_O+\frac{R}{2}) \end{array}\right] \end{array}. \tag{5.19}$$

Here R= 10^6 Ω, R_N – is the time-dependent resistance of the negative group of SCRs, and the multiple subscripts for R has the meaning: $R_{4B} = R_4 + R_B$, $R_{1QB} = R_1 + R_Q + R_B$, etc.

$$\left[\widehat{\mathbf{A}}_{\mathbf{12}}\right]^T = \begin{array}{c} \\ v_{C_v} \\ v_{C_3} \\ v_{C_5} \\ v_{C_7} \\ v_{C_Q} \end{array} \begin{array}{c} \begin{array}{ccccccccccc} i_{L_4} & i_{L_6} & i_{L_S} & i_{L_1} & i_{L_v} & i_{L_2} & i_{L_3} & i_{L_5} & i_{L_7} & i_{L_R} & i_{L_O} \end{array} \\ \begin{bmatrix} 0 & -1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & 0 \end{bmatrix} \end{array} \tag{5.20}$$

and

$$\left[\widehat{\mathbf{B}}_{\mathbf{1}}\right]^T = \begin{array}{c} \\ v_S \\ v_1 \\ v_2 \\ v_C \\ E_O \end{array} \begin{array}{c} \begin{array}{ccccccccccc} i_{L_4} & i_{L_6} & i_{L_S} & i_{L_1} & i_{L_v} & i_{L_2} & i_{L_3} & i_{L_5} & i_{L_7} & i_{L_R} & i_{L_O} \end{array} \\ \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix} \end{array}. \tag{5.21}$$

Similarly KCR gives:

$$\begin{bmatrix} i_{C_v} \\ i_{C_3} \\ i_{C_5} \\ i_{C_7} \\ i_{C_q} \end{bmatrix} = \begin{array}{c} \begin{array}{ccccccccccc} i_{L_4} & i_{L_6} & i_{L_S} & i_{L_1} & i_{L_v} & i_{L_2} & i_{L_3} & i_{L_5} & i_{L_7} & i_{L_R} & i_{L_O} \end{array} \\ \begin{bmatrix} 0 & -1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & 0 \end{bmatrix} \end{array} \begin{bmatrix} \mathbf{i_L} \end{bmatrix}. \tag{5.22}$$

It can be expressed in compact form as,

$$\left[\mathbf{i_C}\right] = \left[\widehat{\mathbf{A}}_{\mathbf{21}}\right] \left[\mathbf{i_L}\right]. \tag{5.23}$$

This can be expressed in the standard form as,

$$\left[\mathbf{i_C}\right] = \begin{bmatrix} \widehat{\mathbf{A}}_{\mathbf{21}} & \widehat{\mathbf{A}}_{\mathbf{22}} \end{bmatrix} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} + \left[\widehat{\mathbf{B}}_{\mathbf{2}}\right] \mathbf{u} \tag{5.24}$$

with $\widehat{\mathbf{A}}_{\mathbf{22}} = \mathbf{0}$ and $\widehat{\mathbf{B}}_{\mathbf{2}} = \mathbf{0}$. Combining (5.18) and (5.24) we have,

$$\begin{bmatrix} \mathbf{v_L} \\ \mathbf{i_C} \end{bmatrix} = \begin{bmatrix} \widehat{\mathbf{A}}_{\mathbf{11}} & \widehat{\mathbf{A}}_{\mathbf{12}} \\ \widehat{\mathbf{A}}_{\mathbf{21}} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} + \begin{bmatrix} \widehat{\mathbf{B}}_{\mathbf{1}} \\ \mathbf{0} \end{bmatrix} \mathbf{u} \tag{5.25}$$

where $\widehat{\mathbf{A}}_{\mathbf{11}}$, $\widehat{\mathbf{A}}_{\mathbf{12}}$, $\widehat{\mathbf{A}}_{\mathbf{21}}$ and $\mathbf{0}$ are vectors of size 11×11, 11×5, 5×11, and 5×5 respectively. Then, substituting (5.25) in (5.16) we can write,

$$\frac{d}{dt} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} = \begin{matrix} 11 \\ 5 \end{matrix} \overset{\begin{matrix} 11 & 5 \end{matrix}}{\begin{bmatrix} \mathbf{\Gamma} & \mathbf{0} \\ \mathbf{0} & \mathbf{C^{-1}} \end{bmatrix}} \begin{bmatrix} \widehat{\mathbf{A}}_{\mathbf{11}} & \widehat{\mathbf{A}}_{\mathbf{12}} \\ \widehat{\mathbf{A}}_{\mathbf{21}} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} + \begin{bmatrix} \mathbf{\Gamma} & \mathbf{0} \\ \mathbf{0} & \mathbf{C^{-1}} \end{bmatrix} \begin{bmatrix} \widehat{\mathbf{B}}_{\mathbf{1}} \\ \mathbf{0} \end{bmatrix} \mathbf{u} \tag{5.26}$$

which after multiplication gives,

$$\frac{d}{dt} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} = \begin{bmatrix} \mathbf{\Gamma}\widehat{\mathbf{A}}_{\mathbf{11}} & \mathbf{\Gamma}\widehat{\mathbf{A}}_{\mathbf{12}} \\ \mathbf{C^{-1}}\widehat{\mathbf{A}}_{\mathbf{21}} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} + \begin{bmatrix} \mathbf{\Gamma}\widehat{\mathbf{B}}_{\mathbf{1}} \\ \mathbf{0} \end{bmatrix} \mathbf{u} \tag{5.27}$$

which can be simplified to,

$$\frac{d}{dt} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} = \begin{bmatrix} \mathbf{A_{11}} & \mathbf{A_{12}} \\ \mathbf{A_{21}} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{i_L} \\ \mathbf{v_C} \end{bmatrix} + \begin{bmatrix} \mathbf{B_1} \\ \mathbf{0} \end{bmatrix} \mathbf{u}. \tag{5.28}$$

Expressing (5.28) in standard state-space form gives,

$$\frac{d}{dt}\mathbf{x(t)} = \mathscr{A}(\mathbf{t})\mathbf{x(t)} + \mathscr{B}\mathbf{u(t)}. \tag{5.29}$$

The system represented by (5.29) is used for the simulation. Each row of (5.29) represents a first order differential equation corresponding to one state-variable, and is implemented as one block with other state variables, the sources, and the time dependent resistors (determining the operation of the converters and those of the choice of the different combinations of PPF, PAF, and SAFs) as inputs.

5.4 Design of Power-Shield

5.4.1 Specification of the system:

Input	Voltage and frequency	Nominal values: 230 V, 50 Hz, single-phase, sinusoidal
Rectifier	Output current (I_O)	Constant at 10 A (highly inductive load)
Load	Voltage (E_O) Power rating	Variable depending on the output power P_O 1 kW $\leq P_O \leq$ 5 kW

5.4.2 General observations on the features of the Topology

It must be noted that a combination of SPF, PPF, and PAF is a must to insulate the load and/or the source from the harmonics of a current-source type of non-linear loads. It is also confirmed through several simulation studies. The most important features are listed below:

- Only PPF, if adopted, may be susceptible to resonance with the source or to sinking the illegitimate currents upstream the load, and may result in distortion of the voltage input to the rectifier if the SCR of the source is low.

- Series impedance (inductive reactance in some form) is very much necessary to shape the source current, to make both the PPF and PAF effective in restricting the harmonics to be drawn from the source.

- However an increase in source inductance, commutating inductance, or the inclusion of the series injection transformer without the PPF, though has some effect on reducing the harmonic content of the source current, it comes at the cost of increased commutation overlap, line notching, and hence the associated problems of – limitation on the range of control and the load dependent model for the load-end rectifier, the later leading to suboptimal controller design or the need for an adaptive controller.

- If a PPF is included along with a SPF then the source current will be shaped very well; the reactive power demand from the source will reduce; and there will be no distortion (line notching) of the voltage at the PCC. The PAF has to

supply only very little fundamental reactive current and the harmonic currents (especially at higher harmonic frequencies). This permits the PAF to be operated at much higher switching frequencies and enables for further reduction in the source current distortion.

- The choice of the injector parameters of the PAF has a deterministic role in the quality of the voltage v_{PCC} at the PCC. The reflection of the injector-inverter voltage v_1/v_2 at PCC must be minimised. The design of the injector parameters is discussed in Section 5.4.4.

- It is also true that a right-shunt (inserted immediately to the left of the CSNL and to the right of a mandatory series passive compensator) arrangement is not suitable.

The main objective of the simulation study is to determine the best possible/ necessary combination of the different components (SPF, SAF, PPF, and PAF), in order to meet the requirements of the Power-Shield for Current-Source type of Nonlinear Loads. It must be noted that a UPQC – a combination of PAF-SAP will not be able to compensate for the CSNL. These devices cannot compensate sharp transitions in the current as is the case in CSNL. Its series compensator being a voltage source is a generalized short circuit; hence UPQC does not have the capability of affecting the line current. Series and Parallel passive compensation is mandatory and that too in the relative position as found and concluded for Power-Shield.

5.4.3 Design of the Passive Filter

The passive filters have their advantages and hence are considered here to reduce the rating of the PAF. The tuned passive filters TF_h, for the dominant frequencies are designed so that the VA rating of the PAF is reduced. Number of steps in the Capacitive reactive power compensator in PPF are selected based on the range of the load variation. For a fixed and ripple-free load current the harmonic contents will remain the same independent of the load power and hence the tuned filters are designed to supply the tuned harmonic current and a portion of the fundamental capacitive reactive power. Detailed information regarding the passive filters for compensation is available

in the literature [Das(2004), El-Saadany *et al.*(2000), Czarnecki and Ginn-III(2005), Volkov(2002)].

Passive Filter – Tuned

The tuned passive filters TF_h are designed such that a certain amount of fundamental reactive current is supplied by the tuned filter. In the current study it is decided to allow this amount to be 1 A (RMS). This makes way for deciding the values of the inductance and the capacitance for the tuned filter. The detailed derivation is provided in Appendix E.2. Thus the capacitance C_h for the h^{th} harmonic tuned filter is:

$$C_h = \frac{h^2 - 1}{h^2} \frac{I_{1h}}{\omega_1 V_1} \tag{5.30}$$

where, I_{1h} – permissible fundamental current; V_1 – fundamental voltage, ω_1 – fundamental frequency in rad/s.
Then the inductance required is obtained from:

$$L_h = \frac{1}{h^2 \omega_1^2 C_h}. \tag{5.31}$$

The capacitor values for the tuned filter are obtained from (5.30) and is found that $C_h \cong 12.5\ \mu\text{F}\ \forall h$. Then the required inductance L_h is obtained from (5.31) for different tuned filters. The quality factor determines the value of the resistance for the tuned filter and hence the size of the conductor diameter for the inductor. The results tabulated in Table 5.1 is obtained by assuming suitable plausible values of the quality factors.

Table 5.1: Tuned filter parameters

Order	C_h	L_h	Q-factor	R_h	f_h
h	μ F	mH		Ω	Hz
3	12.5	90.50	15	5.68	149.64
5	12.5	32.85	25	2.06	248.37
7	12.5	16.92	40	1.00	346.08

Passive Filter – Capacitive Compensator, C_Q

The fundamental reactive current at any firing angle α for a single-phase rectifier drawing a square-wave current from the supply is given by:

$$I_{1Q}(\alpha) = \frac{4I_O}{\pi\sqrt{2}} \sin\alpha. \tag{5.32}$$

The fundamental reactive current $I_{1C_Q}(\alpha)$ to be supplied by the shunt capacitor C_Q is:

$$I_{1C_Q}(\alpha) = I_{1Q}(\alpha) - \sum_{h=3,5,7} I_{1h}. \tag{5.33}$$

Also,

$$I_{1C_Q}(\alpha) = \omega_1 C_Q(\alpha) V_1. \tag{5.34}$$

Then the value of Capacitance $C_Q(\alpha)$ as a function of α (where α determines the load) for reactive power compensation is,

$$C_Q(\alpha) = \frac{I_{1_Q}(\alpha) - \sum_{h=3,5,7} I_{1h}}{\omega_1 V_1}. \tag{5.35}$$

The values are calculated for few cases and are tabulated below:

α (degree)	20°	30°	45°	60°	72°
Capacitance (μF)	1.1	20	46.57	66.38	76.98
Realization (μF)	1	12.5x2	50	50+12.5	50+12.5+12.5

5.4.4 Compensating Current Injector

The design of the PAF involves, the selection of the values for the injecting inductor, the hysteresis band, the inverter DC link voltage V_{DC}, and the switching frequency f_{sw}. With reference to the Figure 5.2 and considering that $\frac{L_k}{R_k} \gg T_{sw}$, qualifying to a linear approximation over the switching period, the associated VCR may be captured in the following expression:

$$V_{DC}\mathbf{s_{f_k}(t)} - v_{PR}(t) = L_k \frac{d}{dt} i_{L_k}; \qquad \text{k= 1, 2} \tag{5.36}$$

where, $\mathbf{s_{f_k}(t)}$ is the switching function evaluated by the hysteresis controller taking values from the set {-1, 0, 1} – depending on the type of switching technique adopted

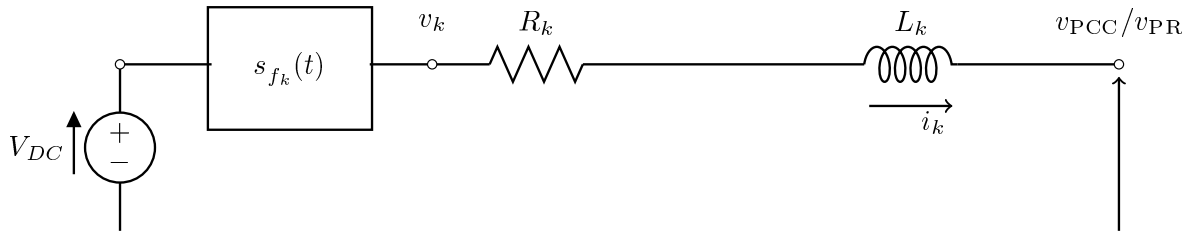

Figure 5.2: Equivalent Circuit for Compensation Current Injection

and v_{PR} is the voltage at the PCC on the right side of the series compensator. Here $v_k = V_{DC}\mathbf{s_{f_k}(t)}$. The requirements of the injector are as follows:

1. it should be capable of following the compensating current within the hysteresis band specified.

2. it should not distort the v_{PCC} (v_{PR}).

The constraint (1), requires that L_k be as small as possible, V_{DC} be as large as possible and f_{sw} be large, with as small a value as possible for Δi – the hysteresis band. The constraint (2), is governed by the inter-relation between the source impedance, effective impedance offered by the SPF and the PPF, and L_k. If L_k is small compared to L_S, then v_{kh} at any ω_h, will appear at PCC and distort v_{PCC}. And if L_k is large, then the ability of the PAF to sink or source the harmonics in the residual current, $i_{RESI}(= i_{L_R} - i_{L_3} - i_{L_5} - i_{L_7} - i_{C_Q})$ will diminish.

Consideration of the limit on Δi

The guideline adopted in this work is as that specified in IEEE standard on harmonics, IEEE 519:1992. Accordingly Total Demand Distortion (TDD) is specified for variable loads [IEEE Std 519-1992(1992)]. In this case of the current-source type of nonlinear loads the harmonic content does not vary with load, hence it is decided that the RMS value of the harmonic current is to be limited, which will limit the total demand distortion (TDD) under all load conditions. Thus if we approximate the ripple in i_{L_k} to a triangular waveform of height Δi, then with a constraint on the RMS value of the error the following relation will approximately hold good,

$$\frac{\Delta i}{\sqrt{3}} \leq 0.05 I_O \tag{5.37}$$

$$\Delta i \leq 0.05\sqrt{3} I_O. \tag{5.38}$$

Also from (5.36)

$$L_k \frac{\Delta i}{\Delta t} = \Delta V. \tag{5.39}$$

And using this in (5.38) we get,

$$\frac{\Delta V \Delta t}{L_k} \leq 0.05\sqrt{3} I_O \qquad \text{which leads to} \tag{5.40}$$

$$\frac{\Delta V}{4 f_{sw} L_k} \leq 0.05\sqrt{3} I_O. \tag{5.41}$$

Then the product,

$$f_{sw} L_k \geq \frac{\Delta V}{0.2\sqrt{3} I_O} \tag{5.42}$$

has to be satisfied. After several simulation studies, a DC link voltage of 500 V is found suitable. Hence ΔV_{max}= ±500 V and ΔV_{min}= ±175 V for a 230 V mains. This is used to find a range of values for the $(f_{sw} \cdot L_k)$ product. This led to the use of a maximum switching frequency of f_{sw} = 15 kHz, and an L_k = 15 mH. The results of the simulation studies for some typical cases are presented in the following Sections 5.7 through 5.9.

5.4.5 Series Compensator

The series compensator is composed of a VSI inverter ($v_C(t)$), a low pass filter (L_v, R_L, C_v, and R_C), and a coupling transformer (L_4, R_4, L_6, R_6 and κ). It has a bypass switch represented by R_B. The κ of the transformer is varied to study the effect of the leakage reactance of the transformer.

5.5 Determination of parameters for the system

5.5.1 DC Machine Parameters Test

The load under consideration is a separately excited DC motor. The armature inductance (L_A) of the motor is necessary in the simulation. This is determined as follows (D.1). The armature resistance (R_A) is measured by Voltmeter-Ammeter method by passing currents over a wide range of values and by moving the armature in order to eliminate the effect of variation of the brush contact. A known constant step voltage is

applied to the armature of the motor (which is kept locked in position) and the armature current waveform ($i_A(t)$) is recorded using a storage oscilloscope [Tektronix(2012)], which is exponentially rising to a steady-state current determined by the applied voltage and the armature resistance. Several experiments are conducted with the field windings kept open as well as shorted. Knowing the applied voltage, the average resistance of the armature, and the slope of the initial portion of the $i_A(t)$, L_A is determined. The mean values of all the experiments are tabulated below:

$$R_A = 1.44\ \Omega \qquad\qquad L_A = 32.4\ \text{mH}$$

5.5.2 Determination of Utility parameters

The Power-Shield is interfaced with the utility and hence the utility parameters are necessary of conducting the simulation studies. Some practical estimate can be obtained from [Ramamurthy(2009)]. There is some information reported in the literature in this regard [D.Basic and P.K.Muttik(2000), Simone Buso and Mattavelli(1998), Bhattacharya *et al.*(1996)]. A Thevenin's equivalent ($Z_S = R_S + j\omega_S L_S$) is considered in all the cases. However for ascertaining the values at the PCC in the laboratory where the experiments are intended to be conducted the values of the Thevenin's equivalent are determined by Voltmeter-Ammeter method. The procedure adopted is as follows (D.3). The open circuit voltage is determined at the PCC. A known resistive load (lamp load) is connected at the PCC and the voltage with this load is determined. This experiment is repeated at several instances of the day and on different days of the weeks. The average values from the experiment are tabulated below:

$$R_S = 330\ \text{m}\Omega \qquad\qquad L_S = 711\ \mu\text{H}$$

5.6 Simulation setup

The model obtained is coded in MATLAB®/Simulink® ([MathWorks®(2006)])in different blocks as represented in the Figure 5.3. A detailed Simulink schematic is appended in A.5. The detailed simulations are carried out and the results with conclusions are presented in the following Sections. A brief description of the block diagram of the setup is given below:

- Parameters: This block represents all the parameters of the components of the Power-Shield – like those of source impedance, passive filters, active compensators

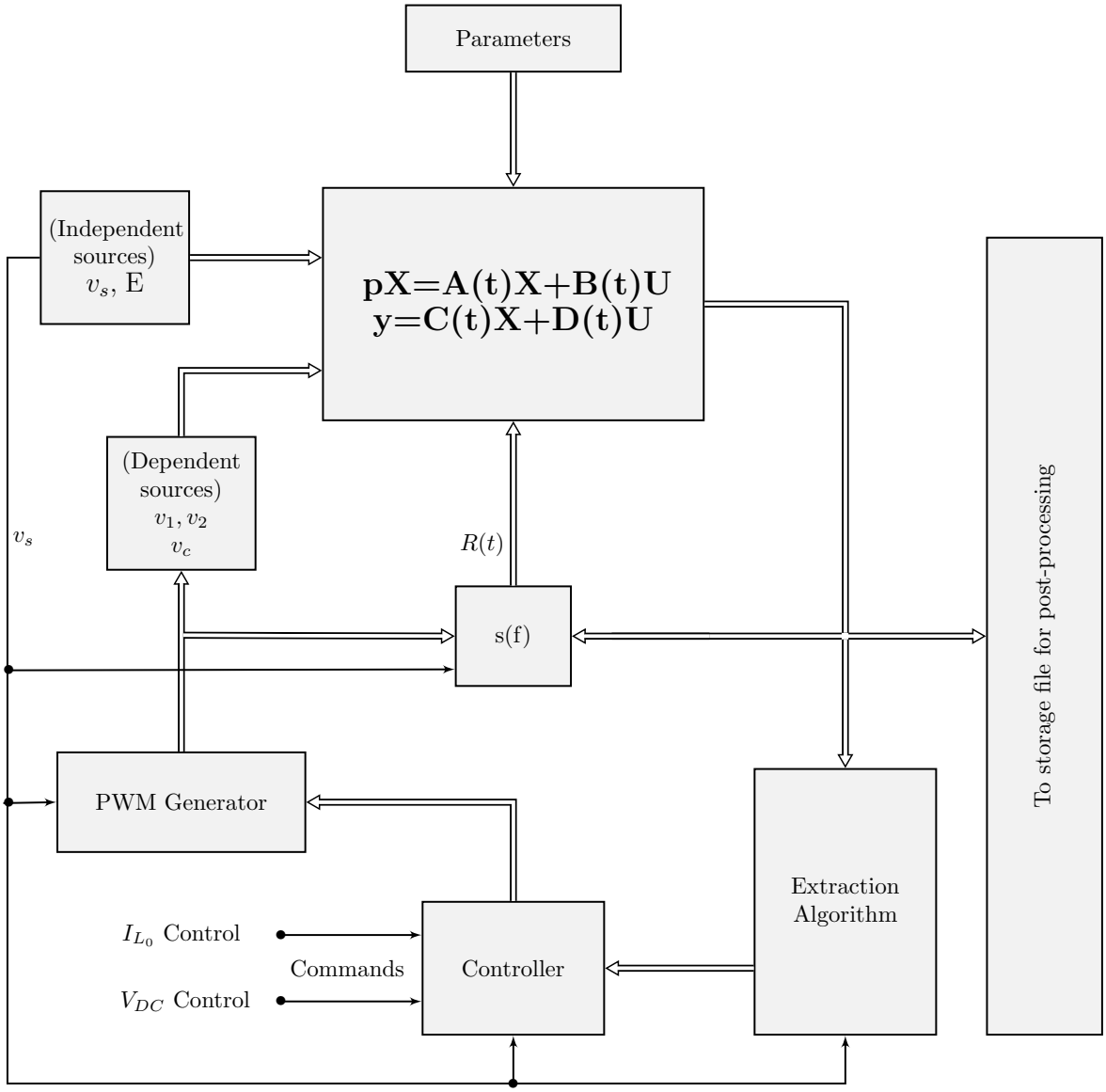

Figure 5.3: Simulation setup for Power-Shield

(shunt and series), and load from the power circuit side, and PLL, control system, PWM technique, and extraction algorithm from the control system side.

- Independent sources: It represents the only two independent sources – $v_S(t)$ and E_O.

- Dependent sources: The sources which are dependent on the control requirement are shown in this block. They are derived depending on the load conditions and on the type of control and switching technique used.

- System: This block represents the mathematical representation of the power circuit.

- Extraction Algorithm: It takes input from the System and determines compensating component of the current to be injected by controlling either $v_1(t)$ (left-shunt) or $v_2(t)$ (right-shunt) to improve the quality of the input current waveform, or the voltage to be injected by controlling v_C to execute the necessary function intended by the series compensator. It contains,
  - a PLL and
  - the extraction algorithms presented in this thesis. One of the algorithms, namely that proposed in Section 3.3 for extraction, is used in the implementation of the PAF and its performance is observed to be satisfactory.
- PWM block: It represents the implementation of the switching techniques used.
- Controller: This block represents mainly the control system associated with the active series and shunt compensators. This block determines the dependent sources $v_1(t)$ or $v_2(t)$, and $v_C(t)$ necessary for improving the quality of POWER. The PWM block will generate these voltages. The rectifier output current I_{L_O} – that determines the load current i_{L_R} on the utility system and reference for indirect control of bus voltage of the VSI for the PAF are the reference inputs for the controller as shown in Figure 5.3.
- $\mathbf{s}_f\mathbf{(t)}$ block: The load considered is a single-phase SCR controlled bridge-rectifier, with R-L-E load. The SCRs are represented by four time-dependent resistors ($R_k(t)$). They take on a high value (10 MΩ) when any is OFF, and a very low value (mΩ) when any is ON. They are triggered (switched-ON) by the firing angle controller. The switching ON of any SCR is an independent input as far as the converter is concerned, but the switching OFF which depends on the device current and hence requires a separate logic. This block is concerned with the generation of those four time dependent resistors representing the bridge rectifier.

5.7 Simulation Results with only Passive Filters

The set of cases considered here is to find out the effectiveness of the Passive filters. The effects of L_R, L_S, and X_{l_T} are to be studied. Two load conditions are considered and the simulation trials are conducted with and without PPF. The common model

parameters are as specified in Appendix A.2 and those of the tuned filters are as given in Appendix A.1.2, corresponding to the values used in the experimental setup. The results are presented in the following. A base current of I_{NOM} = 10 A, is used for calculation of TDD.

5.7.1 Effect of Commutating Inductance L_R

The following cases are considered for this study.

Case-1: L_R= 150 μH, L_S= 711 μH, E_O = 110 V, PPF – ON, C_Q = 50 μF

The relevant waveforms are presented in Figure 5.4. The fast transitions of the rectifier input current i_{LR} is evident in the plots.

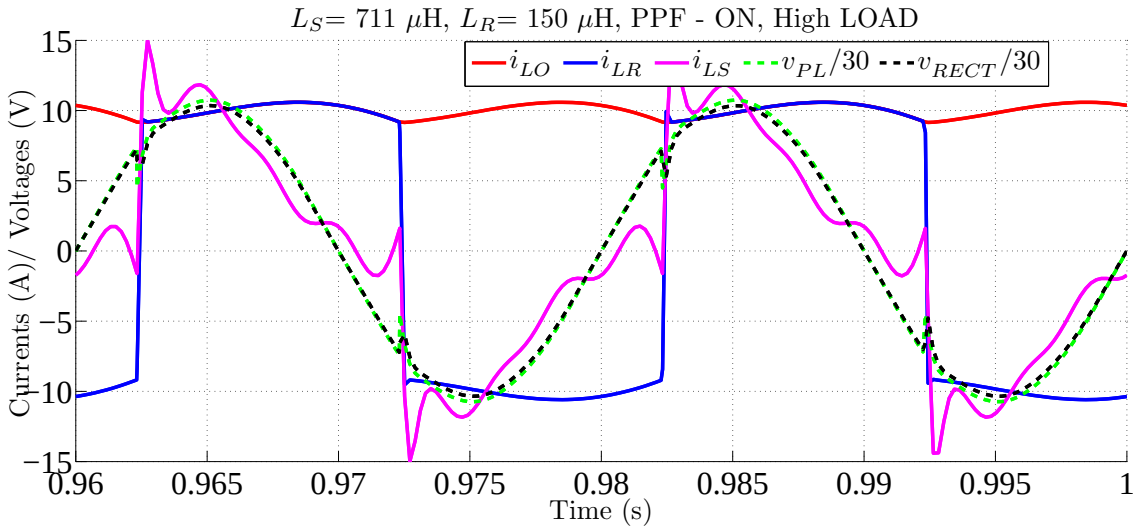

Figure 5.4: Relevant waveforms for showing the effect of Commutating Inductance for Case-1

Case-2: L_R = 15 mH, L_S = 711 μH, E_O = 110 V, PPF – ON, C_Q = 50 μF

In this study a large value of the commutating inductance, L_R= 15 mH is added and the PPF is kept in the ON condition. The pertinent waveforms for drawing conclusions are shown in Figure 5.5. As is expected the i_{LR} transitions very slowly. There is a large commutation overlap angle, which results in the loss of average voltage.

Comparison

The harmonic spectra for the two cases considered are as shown in Figure 5.6 and

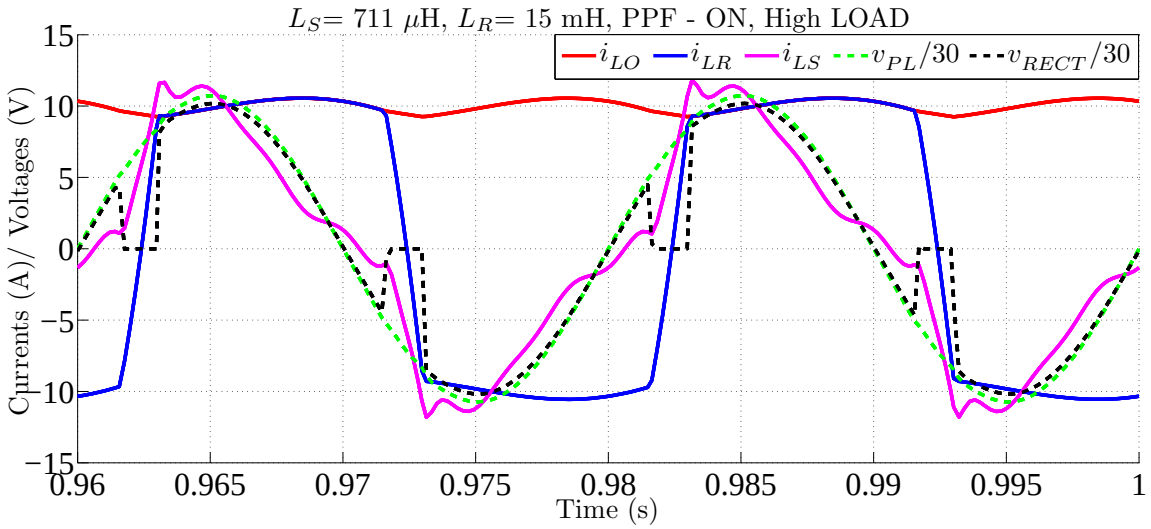

Figure 5.5: Relevant waveforms for showing the effect of Commutating Inductance for Case-2

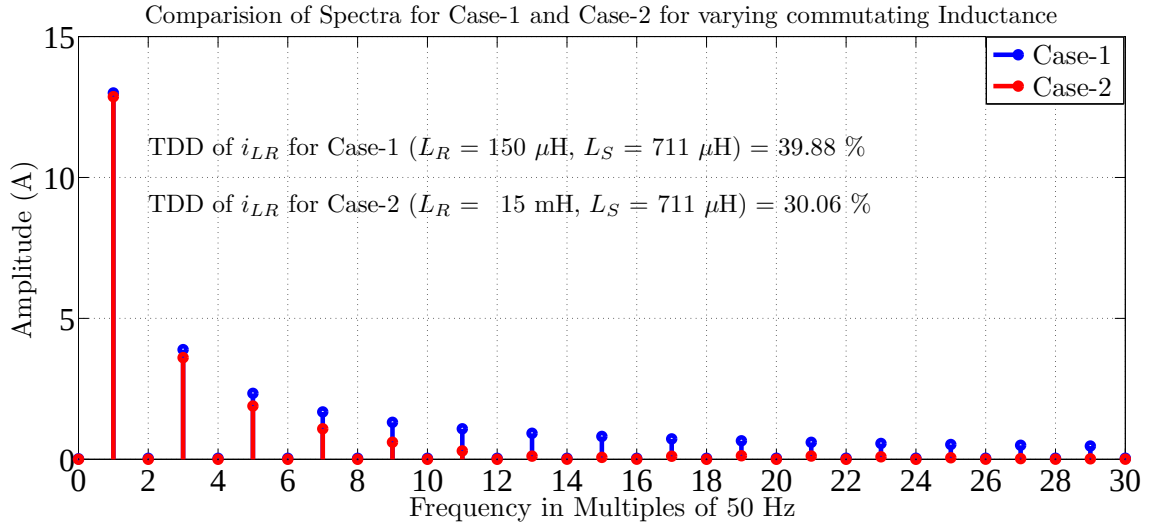

Figure 5.6: Harmonic Spectra of i_{LR} showing the effect of Commutating Inductance

Figure 5.7. It can be seen that the TDD in i_{LR} reduces from 39.88% to 30.06% and that in i_{LS} reduces from 26.08% to 17.57% for an increase in the L_R from 150 μH to 15 mH. It can also be observed that the higher harmonics are considerably reduced in each case. This implies that there is less stress on the PAF. This improvement in the TDD comes with a decrease in the firing angle and hence the fundamental power factor angle – an advantage considering the power factor, though line-notching and related problems remain as a concern.

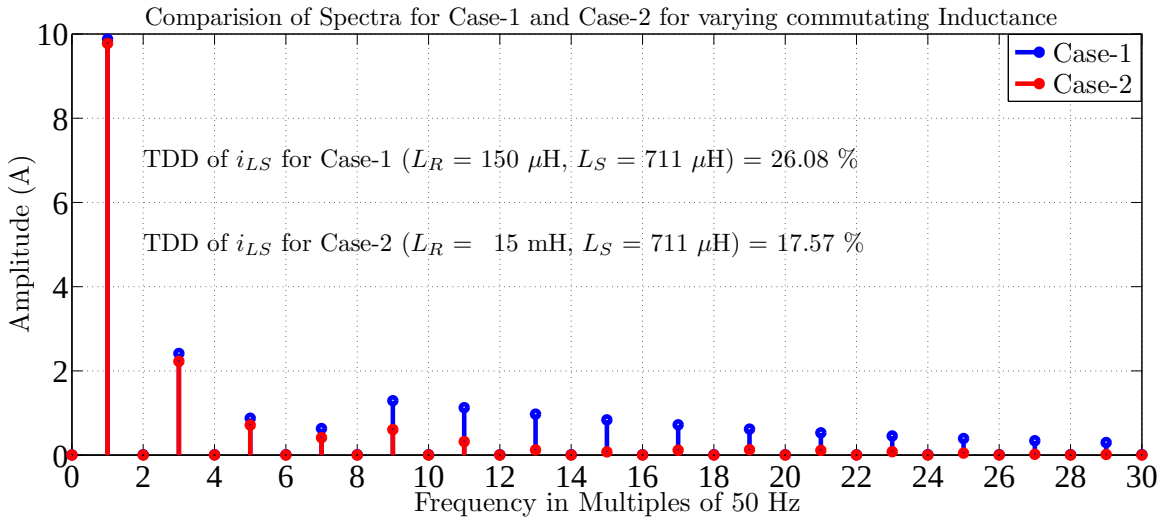

Figure 5.7: Harmonic Spectra of i_{LS} showing the effect of Commutating Inductance

5.7.2 Effect of Source Inductance L_S

The following cases are considered for this study.

Case-1: L_R= 150 μH, L_S= 711 μH, E_O= 110 V, PPF – ON, C_Q = 50 μF

The pertinent waveforms for this case are presented in Figure 5.4. The spectra of the i_{LS} and i_{LR} are shown in Figure 5.8. It can be seen from the spectrum of i_{LS} that

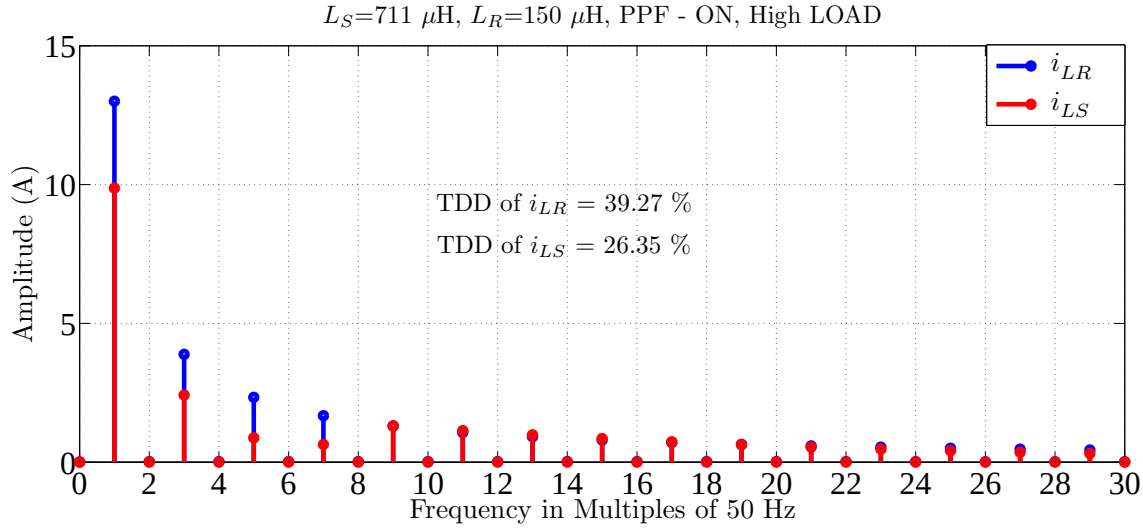

Figure 5.8: Harmonic Spectrum of i_{LS} showing the effect of Source Inductance

there is a decrease only in 3^{rd}, 5^{th}, and 7^{th} order harmonics (because of the presence of the corresponding tuned filters) and none of the other higher order harmonics are snubbed in the source current. The higher inductive reactance offered by the tuned

filters to higher order harmonics prevents such currents flowing into the parallel tuned filter branches. Hence there is little improvement in the TDD of i_{LS}.

Case-2: L_R = 150 μH, L_S = 5 mH, E_O = 110 V, PPF – ON, C_Q = 50 μF

The L_S is now increased to 5 mH and the results are presented in Figure 5.9. The

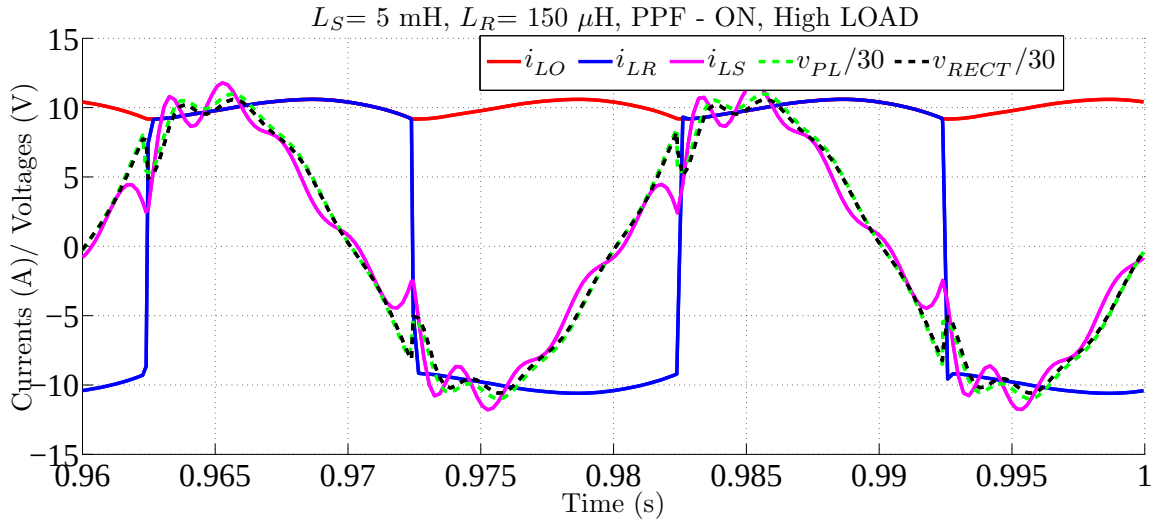

Figure 5.9: Relevant waveforms for showing the effect of Source Inductance

spectrum of the i_{LS} and i_{LR} is shown in Figure 5.10. It can be seen from the spectrum

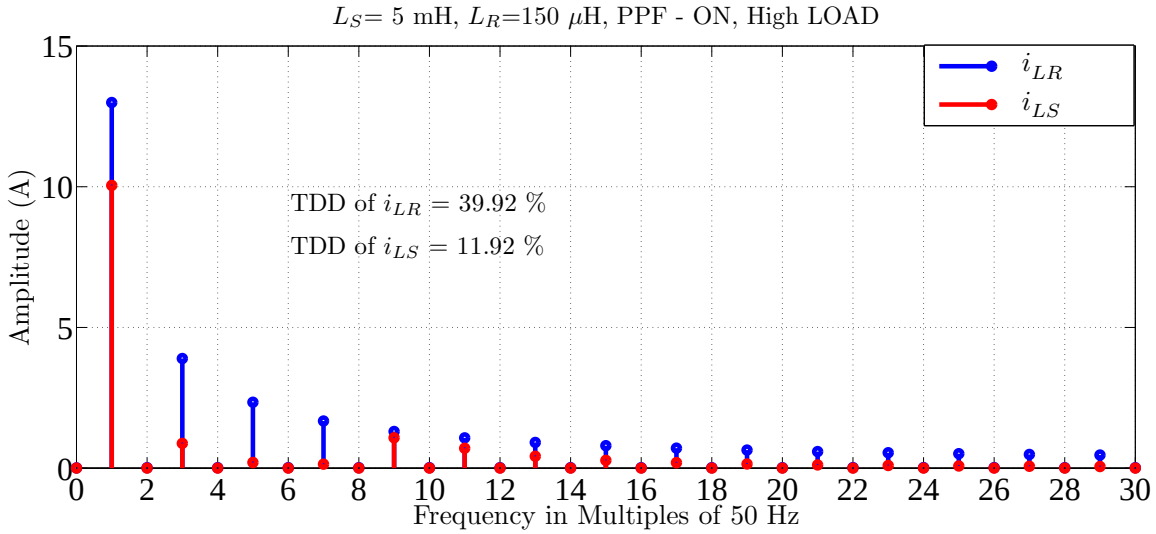

Figure 5.10: Harmonic Spectrum for showing the effect of Source Inductance

of i_{LS} that mainly the 3^{rd}, 9^{th}, 11^{th} and 13^{th} harmonics remain in the source current and most of the other – tuned as well as untuned harmonics are attenuated in the source current. The higher inductive reactance offered by L_S to higher order harmonics in

comparison with the tuned filters prevents such currents flowing into the source. Hence there is a good improvement in the TDD of i_{LS}.

Case-3: L_R = 150 μH, L_S = 711 μH, E_O = 12 V, PPF – ON, C_Q = 75 μF

The results for this case are presented in Figure 5.11. The spectrum of the i_{LS} and i_{LR}

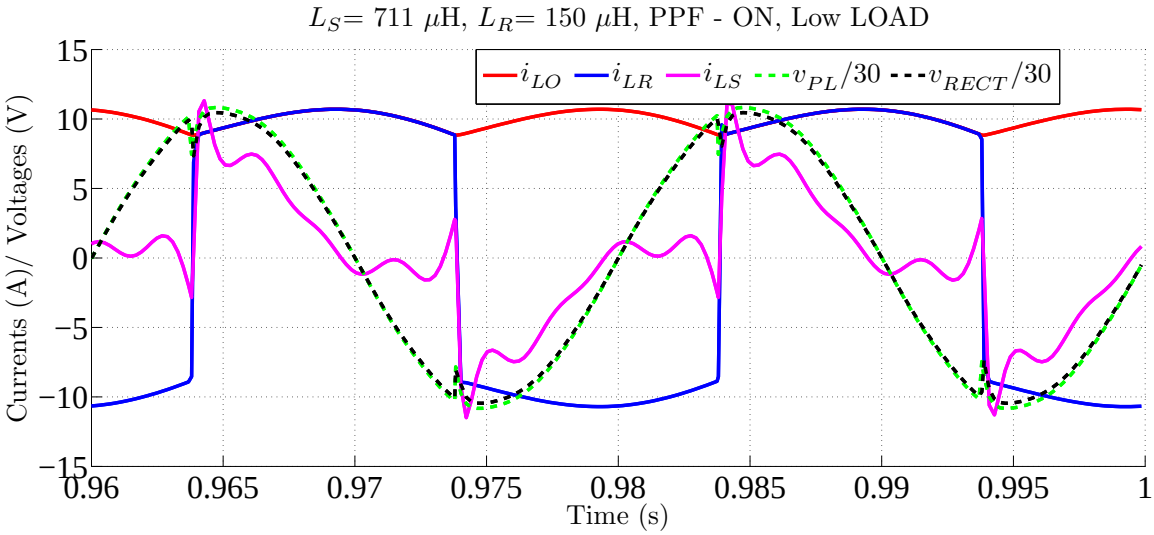

Figure 5.11: Relevant waveforms for showing the effect of Source Inductance

is shown in Figure 5.12. It can be seen from the spectrum of i_{LS} that it is similar to that

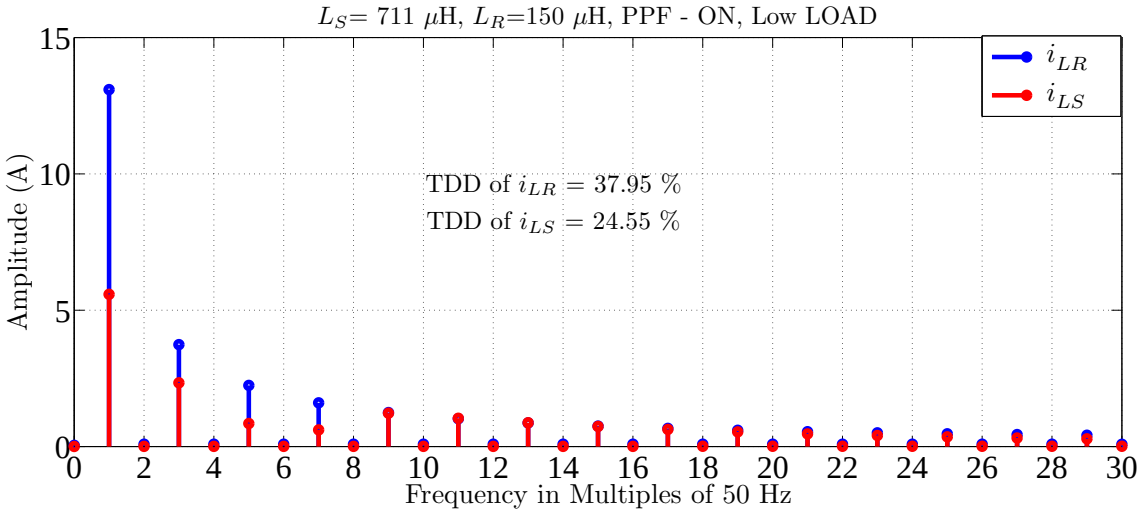

Figure 5.12: Harmonic Spectrum for showing the effect of Source Inductance

presented in Figure 5.8, except for the drastic decrease in the fundamental component which results from the contribution of the reactive power compensator. There is no change in the harmonics. There is not much change in the TDD since it is defined with reference to the normal rated current (I_{NOM} = 10 A).

Case-4: L_R = 150 μH, L_S = 5 mH, E_O = 12 V, PPF – ON, C_Q = 75 μF

The L_S is now increased to 5 mH and the results are presented in Figure 5.13. The drastic decrease in the amplitude of the i_{LS} is due to the absorption of the large reactive component of the current by the reactive power compensator C_Q. It can also be observed that the source current is almost in time phase with the supply voltage, and hence the load on the PAF is considerably reduced. The spectrum of the i_{LS} and

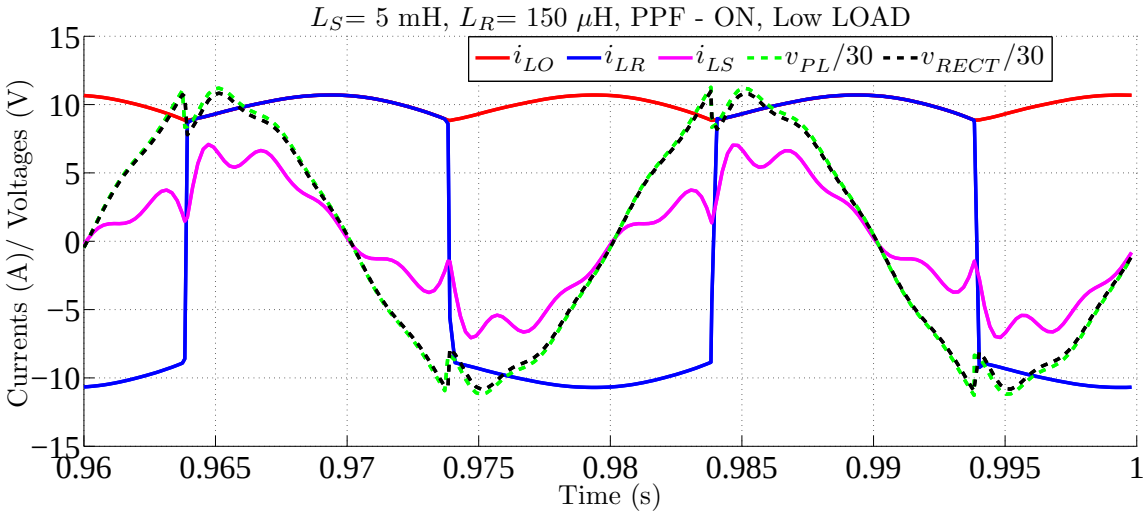

Figure 5.13: Relevant waveforms for showing the effect of Source Inductance

i_{LR} is shown in Figure 5.14. It can be seen from the spectrum of i_{LS} that mainly the

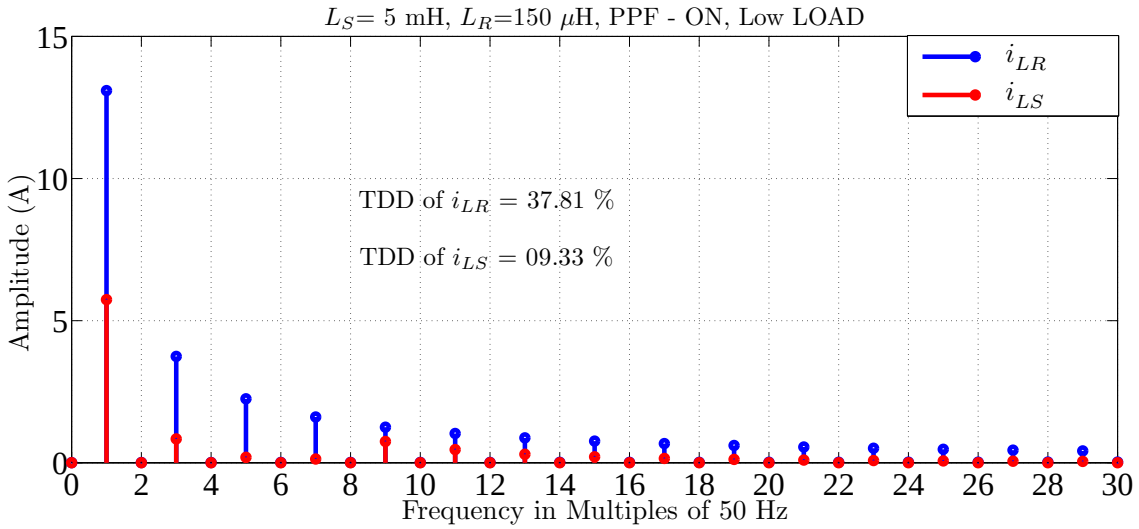

Figure 5.14: Harmonic Spectrum for showing the effect of Source Inductance

3^{rd}, 9^{th}, and 11^{th} harmonics remain in the source current and most of the other – tuned as well as untuned harmonics are attenuated in the source current. Hence there is a

good improvement in the TDD of i_{LS} as compared with that of the case with a source inductance of L_S= 711 μH.

5.8 Effect of Series transformer

The effect of the series compensation is emulated by adjusting the leakage reactance (X_{l_T}) of the series transformer, which in turn is varied by changing the mutual-coupling-coefficient, (κ). The studies are conducted with $L_4 = 1$ H $= L_6$, and considering mutual coupling coefficients of $\kappa = 0.99$ (corresponding to $X_{l_T} = 20$ mH) and 0.998 ($X_{l_T} = 4$ mH). Two loading conditions P_1 ($I_O = 10$A, $R_O = 3.75\ \Omega$, and $E_O = 110$ V); and P_2 ($I_O = 10$A, R_O= 3.75 Ω, and $E_O = 12$ V) are considered. Also the PPF is either ON or OFF in each case. The source and commutating inductance values are fixed at L_R = 150 μH and L_S = 711 μH.

5.8.1 Effect of series leakage reactance (X_{l_T}) with Load = P_1

Case-1: κ = 0.99, E_O = 110 V, PPF – ON, C_Q = 50 μF

The waveforms of the i_{LS} and i_{LR} for the case are shown in Figure 5.15. It is clear from the waveforms that with large leakage reactance the source current i_{LS} is smooth and is almost in phase with v_{PCC} and v_{RECT} The spectrum of the i_{LS} and i_{LR} is shown in

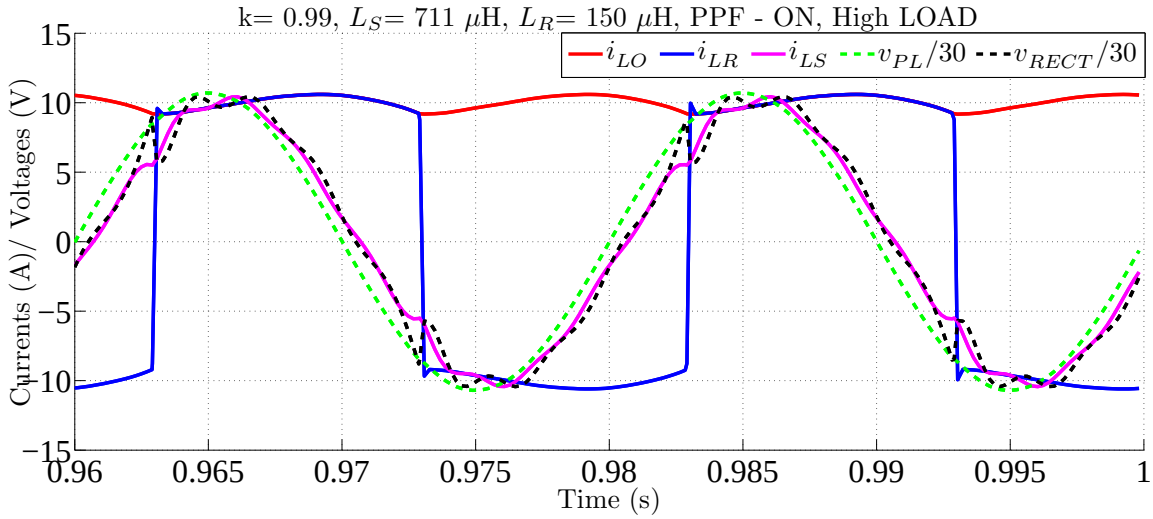

Figure 5.15: Relevant waveforms for showing the effect of Transformer leakage reactance (X_{l_T})

Figure 5.16. The Figure 5.15 reveals that there is very little distortion in the voltages

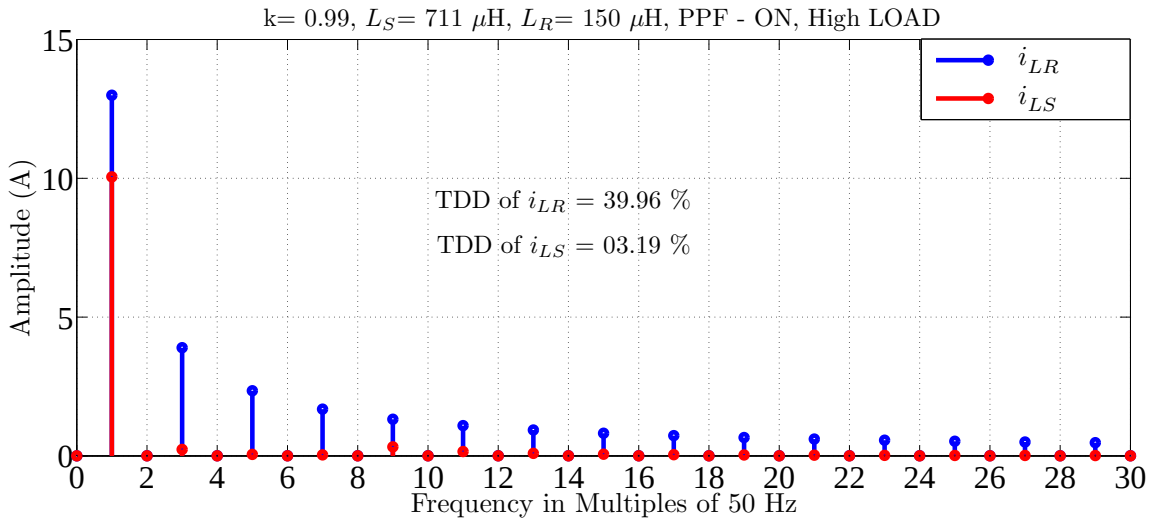

Figure 5.16: Harmonic Spectrum for showing the effect of X_{l_T}

at the PCC, and the source current is almost in-phase with the source voltage. The spectra in Figure 5.16, show a remarkable improvement in the TDD of the i_{LS} visa-a-vis in that of i_{LR}.

Case-2: κ = 0.99, E_O = 110 V, PPF – OFF, C_Q = 50 μF

The relevant waveforms are shown in Figure 5.17. The spectrum of the i_{LS} and i_{LR} is

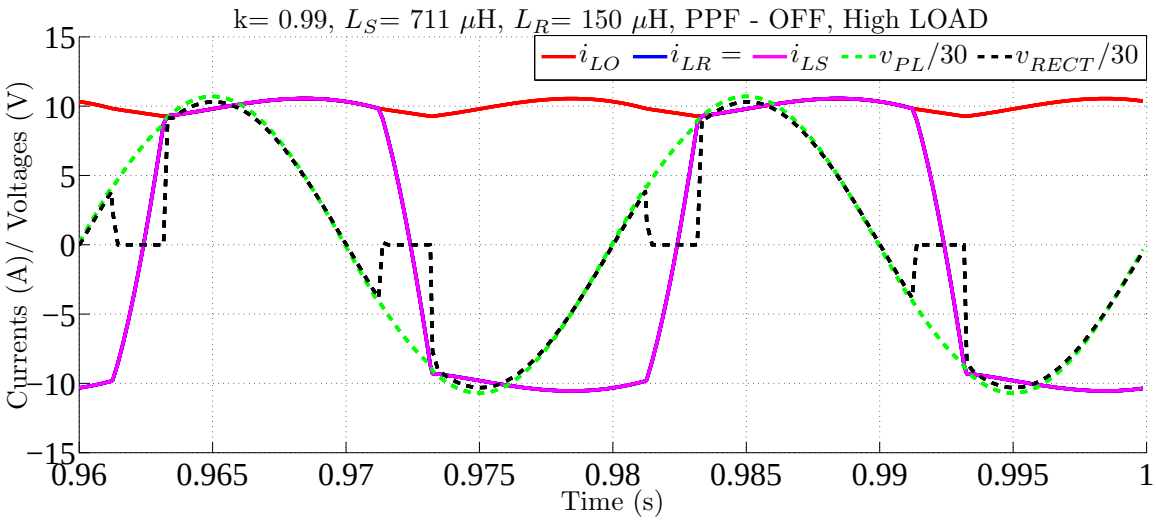

Figure 5.17: Relevant waveforms for showing the effect of Transformer leakage reactance (X_{l_T})

shown in Figure 5.18. In this case since the PPF is OFF, it amounts to the case with an increased value for L_R. It shows wide notches in the v_{RECT} but the v_{PCC} is smooth

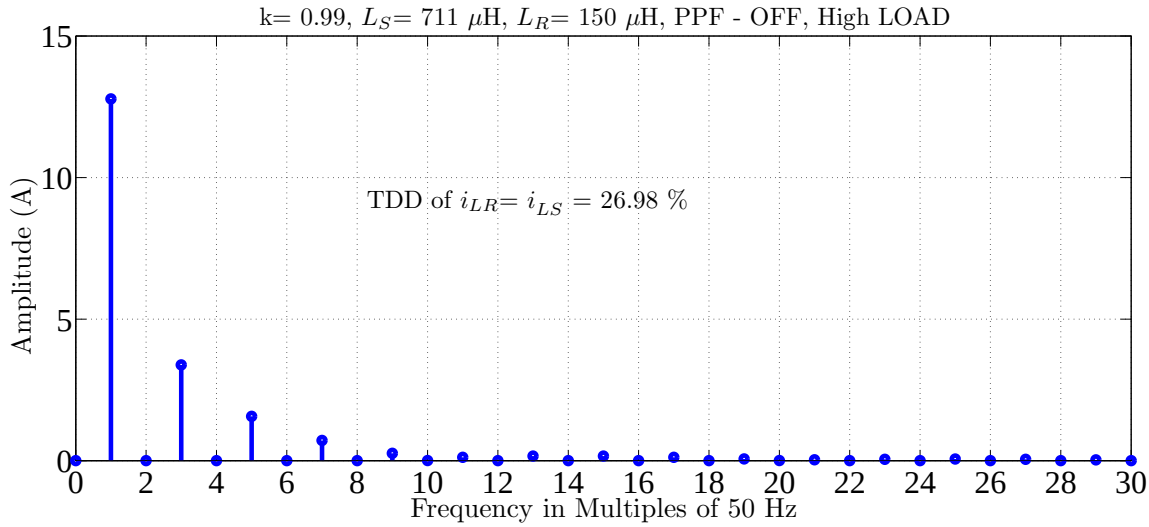

Figure 5.18: Harmonic Spectrum for showing the effect of X_{l_T}

enough. The slow transitions in the $i_{LS} = i_{LR}$ is obvious and results in a better TDD (=26.98%) as compared to around 40% of a square-wave.

Case-3: κ = 0.998, E_O = 110 V, PPF – ON, C_Q = 50 μF

The relevant waveforms are shown in Figure 5.19. The spectrum of the i_{LS} and i_{LR}

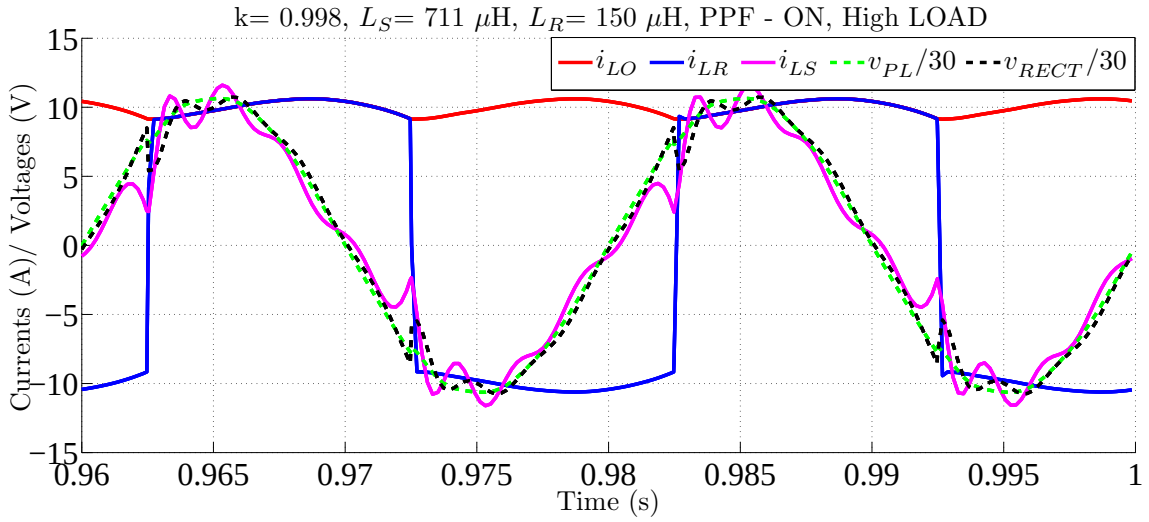

Figure 5.19: Relevant waveforms for showing the effect of Transformer leakage reactance (X_{l_T})

is shown in Figure 5.20. The effect of increased coupling coefficient and hence that of a decrease in X_{l_T} is evident in this case as compared to Case-1. The voltages at the common bus are more distorted and the TDD in i_{LS} increased from 03.19% for Case-1 to 12.05%.

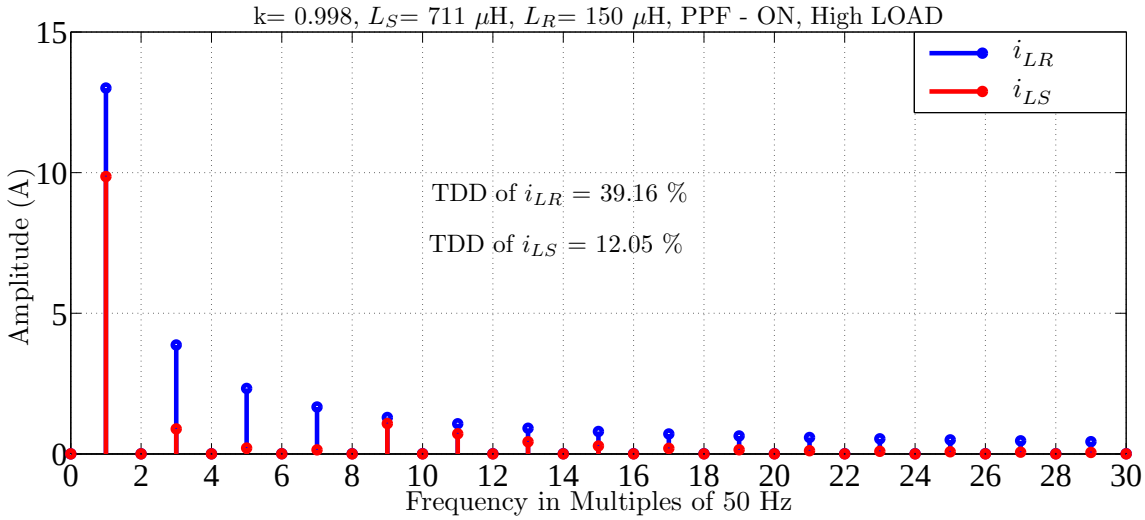

Figure 5.20: Harmonic Spectrum for showing the effect of X_{l_T}

Case-4: κ = 0.998, E_O = 110 V, PPF – OFF, C_Q = 50 μF

The relevant waveforms are shown in Figure 5.21. The decrease in X_{l_T} with the in-

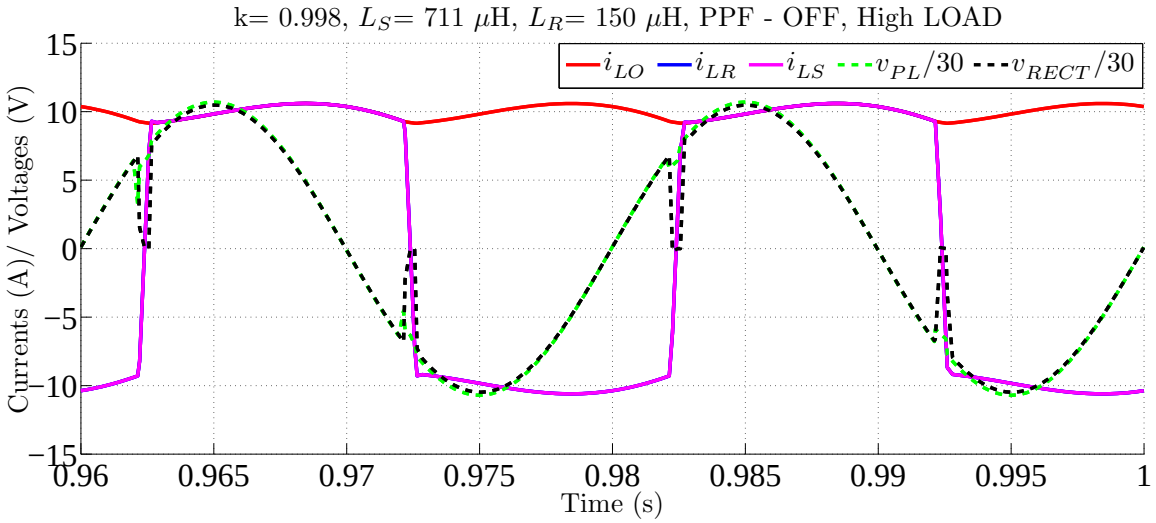

Figure 5.21: Relevant waveforms for showing the effect of Transformer leakage reactance (X_{l_T})

crease of κ, results in reduction of the notch-width as compared to Case-2, however the TDD increases from 26.98% to 36.78%. The spectrum of the i_{LS} and i_{LR} is shown in Figure 5.22.

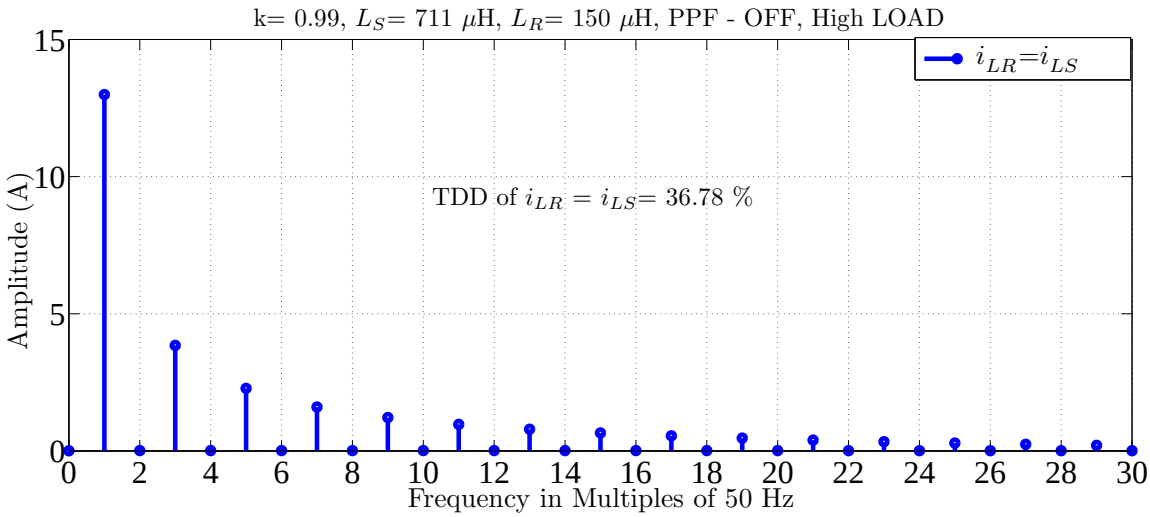

Figure 5.22: Harmonic Spectrum for showing the effect of X_{l_T}

5.8.2 Effect of series leakage reactance (X_{l_T}) with Load = P_2

Case-1: κ = 0.99, E_O = 12 V, PPF – ON, C_Q = 75 μF

The relevant waveforms are shown in Figure 5.23. The spectrum of the i_{LS} and i_{LR}

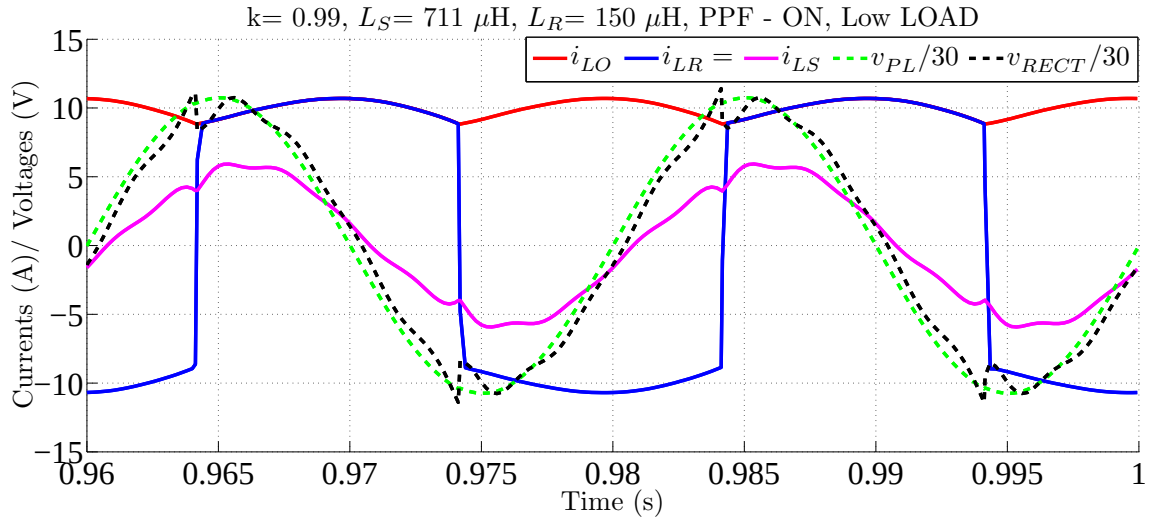

Figure 5.23: Relevant waveforms for showing the effect of Transformer leakage reactance (X_{l_T})

is shown in Figure 5.24. It is comparable to that shown in Figure 5.16 except for the decrease in the amplitude of the fundamental.

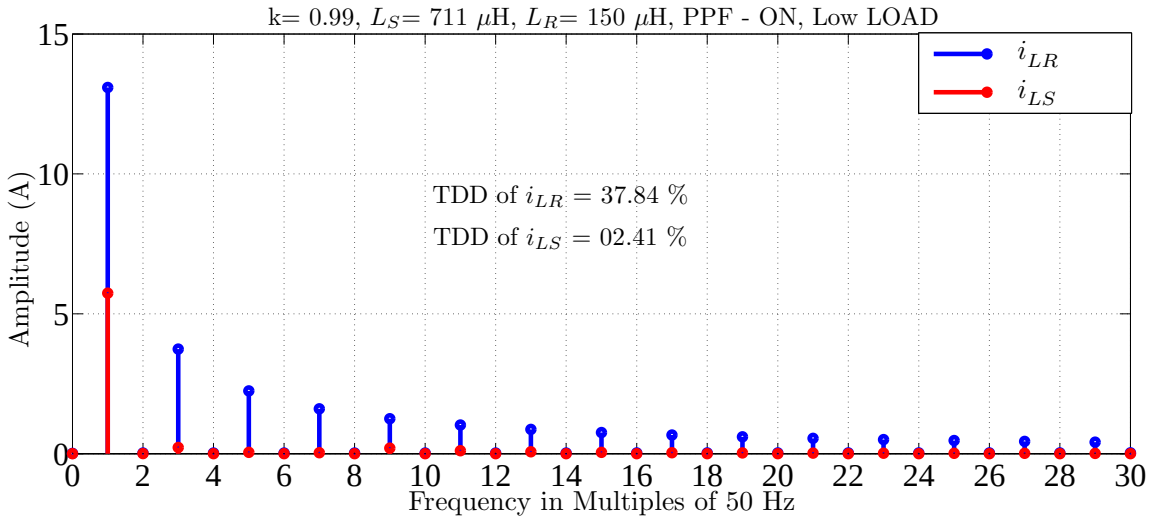

Figure 5.24: Harmonic Spectrum for showing the effect of X_{l_T}

Case-2: κ = 0.99, E_O = 12 V, PPF – OFF, C_Q = 75 μF

The relevant waveforms are shown in Figure 5.25. The wide line-notch is evident in the waveform of v_{RECT}. The spectrum of the i_{LS} and i_{LR} is shown in Figure 5.26.

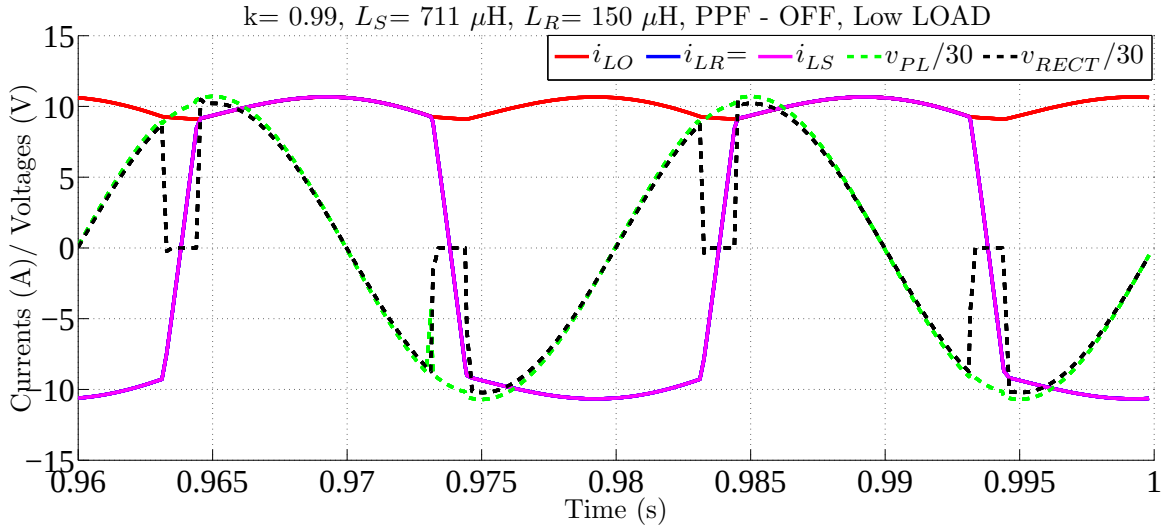

Figure 5.25: Relevant waveforms for showing the effect of Transformer leakage reactance (X_{l_T})

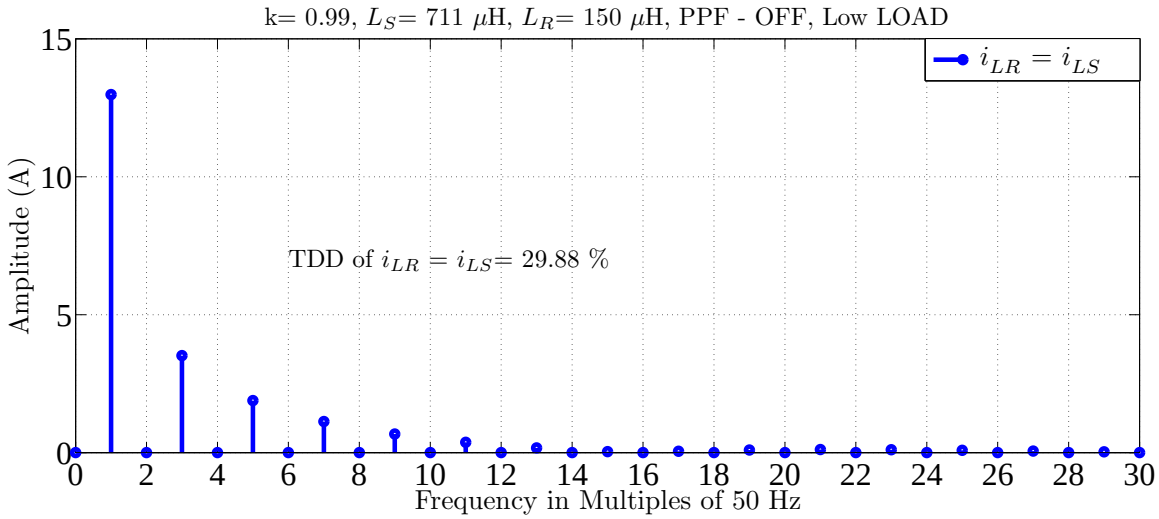

Figure 5.26: Harmonic Spectrum for showing the effect of X_{l_T}

Case-3: κ = 0.998, E_O = 12 V, PPF – ON, C_Q = 75 μF

The relevant waveforms are shown in Figure 5.27. The spectrum of the i_{LS} and i_{LR} is

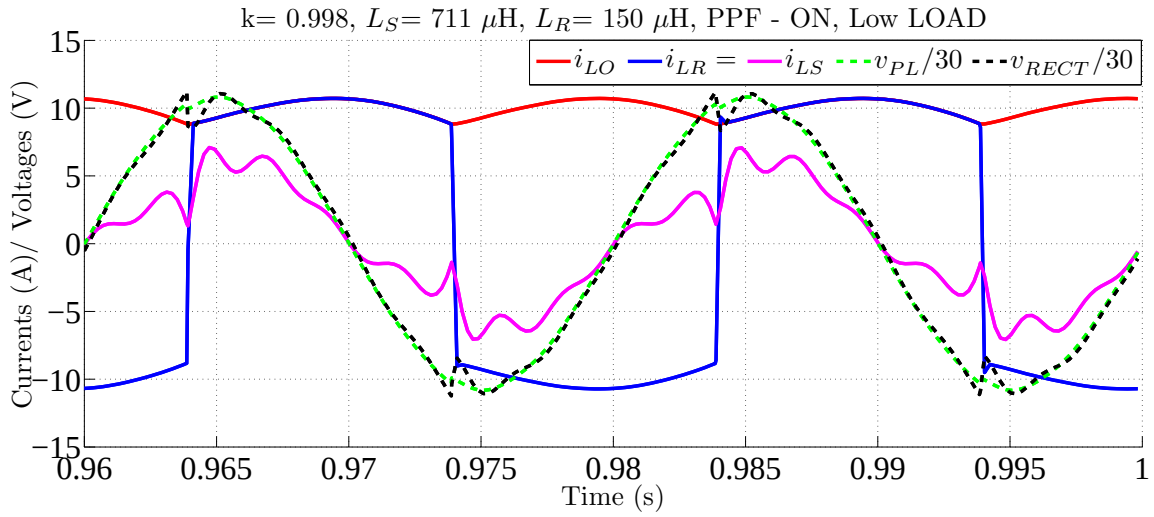

Figure 5.27: Relevant waveforms for showing the effect of Transformer leakage reactance (X_{l_T})

shown in Figure 5.28.

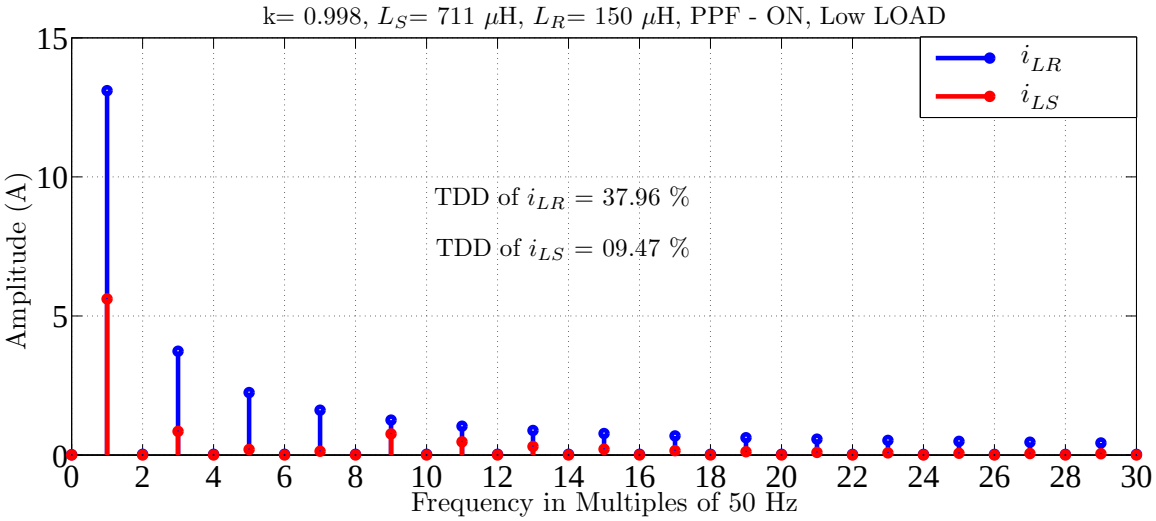

Figure 5.28: Harmonic Spectrum for showing the effect of X_{l_T}

Case-4: κ = 0.998, E_O = 12 V, PPF − OFF, C_Q = 75 μF

The relevant waveforms are shown in Figure 5.29. The spectrum of the i_{LS} and i_{LR} is

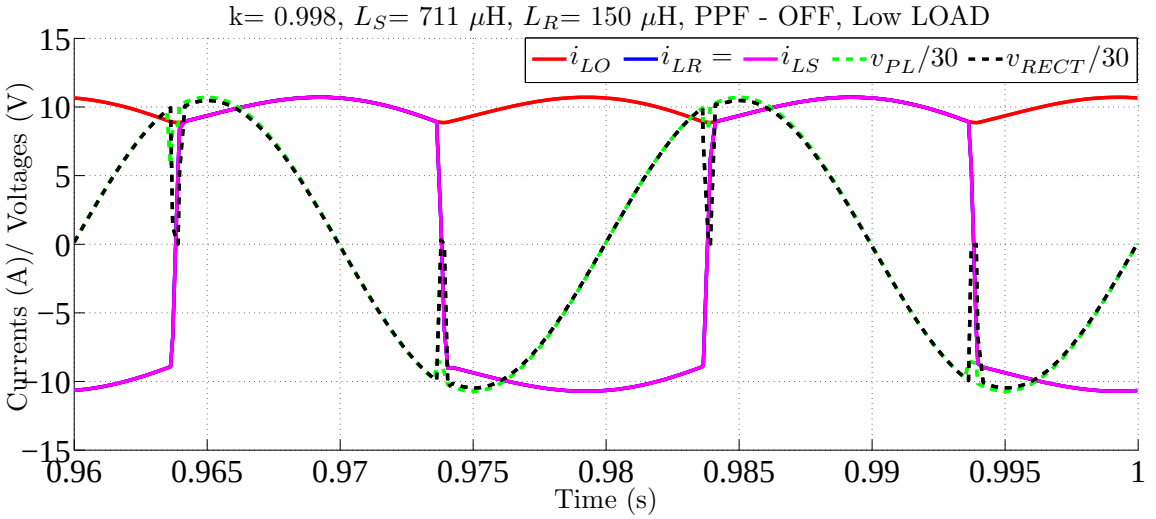

Figure 5.29: Relevant waveforms for showing the effect of Transformer leakage reactance (X_{l_T})

shown in Figure 5.30.

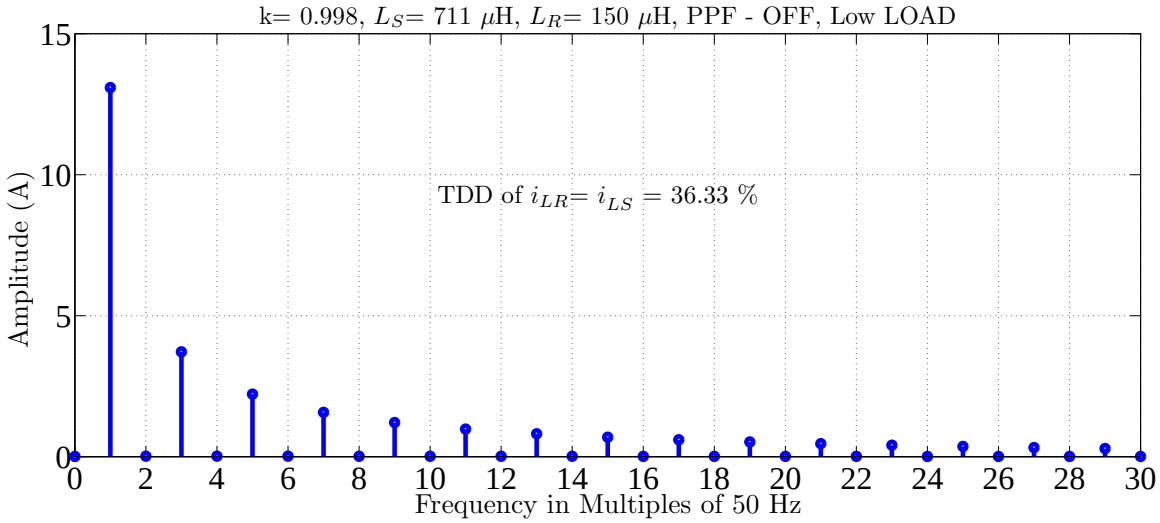

Figure 5.30: Harmonic Spectrum for showing the effect of X_{l_T}

The results are tabulated in Tables 5.2 and 5.3. The following observations are

Table 5.2: Effect of inclusion of series transformer and its coupling coefficient, κ

Case: High load (P_1)	κ	PPF	TDD (%)		RMS (A)		α (in degrees)
			i_{LR}	i_{LS}	i_{LR}	i_{LS}	
Case-1	0.990	ON	39.96	03.19	10.03	07.11	40.53
Case-2		OFF	26.98		10.05		13.26
Case-3	0.998	ON	39.16	12.05	10.03	07.07	41.92
Case-4		OFF	36.78		10.09		37.96

Table 5.3: Effect of inclusion of series transformer and its coupling coefficient, κ

Case: Low load (P_2)	κ	PPF	TDD (%)		RMS (A)		α (in degrees)
			i_{LR}	i_{LS}	i_{LR}	i_{LS}	
Case-1	0.990	ON	37.84	02.41	10.00	04.06	67.93
Case-2		OFF	29.88		10.01		51.78
Case-3	0.998	ON	37.96	09.47	10.02	04.08	68.54
Case-4		OFF	36.33		10.03		65.84

made:

- a transformer with a smaller coupling coefficient results in smoother source current, indicated by a smaller TDD, but the firing angle required for regulating the i_{LO} decreases affecting the range of control for the load.
- there is not much change in the RMS values of the i_{LR} or i_{LS} with respect to changes in κ.

- when PPF is OFF, the decrease in α required to regulate i_{LO} at 10 A is very large. The TDD of i_{LR} remains higher, though smaller than that when PPF is ON. It should be noted that the shunting effect of the PPF smooths the i_{LS} while making the current transitions in i_{LR} very fast and thus results in higher TDD for i_{LS}.

- when PPF is ON the RMS value of the i_{LS} reduces very much and the TDD of i_{LS} is very small for smaller κ. The impedance (due to L_S or X_{l_T}) to the left of the PPF plays a very significant role in filtering.

- with changing values of the series element, dictated by the changing source impedance or the inclusion or exclusion of the series transformer, there is a need to readjust the controller coefficients, of the firing angle controller responsible for regulating the load current at the desired value.

5.8.3 Conclusion

Thus inclusion of series transformer to mitigate sag/swell though has the effect of smoothing the source current, it comes with a reduced v_{RECT}, which means series compensator voltage has to include a component to overcome the series drop across X_{l_T} in addition to component due to the voltage sag/ swell at the supply end. This also has to be considered along with the range of firing angle control required under different loading conditions.

5.9 Parallel Active and Passive Filters: Simulation studies with a plausible parameter set for the tuned filter

In this Section the results of the simulation studies conducted with PAF, SPF, and PPF included together are presented. It is intended to demonstrate the suitability of the compensator structure in overcoming the problems associated with power quality

for the current source type nonlinear loads. Several cases are considered and the results for 14 cases (A.4, A.1.1) are compiled and the summary of the results are presented in the following. Only the topology that results in the best possible performance is considered namely, the left-shunt (i_{L_1} injection) arrangement with PPF, i.e., for the case with series compensator included (when the series compensator is not included there is no distinction between the right-shunt or the left-shunt). The results presented here correspond to the extraction algorithm based on the adaptation of Pettigrew's scheme. Initially few waveforms are given to validate the correctness of the simulation setup and the complete implementation. The results of the TDD are compiled for each case and plotted against the IEEE Std. 519:1992 for comparison. The practically acceptable parameters of the filter was obtained in Section 5.4.3 given in Table 5.1 and is reproduced in Appendix A.1.1. Those values are used in this set of simulations, with a view to study the topology with parameters as close as possible to the real field situations. The variable i_{RESI} used to associate with the residual current left after absorption of harmonics and reactive current from i_{LR} by the PPF is also related to the source current i_{LS} and PAF current i_1 as follows:

$$i_{RESI} = i_{LS} + i_{L_1} + i_{L_2}$$

with a negligible i_{L_2} as $R_2 = 1$ MΩ (right-shunt is OFF). The salient results are tabulated in Table 5.4

5.9.1 Results with only Parallel Active Filter

In this section the results obtained with only PAF for compensation is presented. The results for three cases are presented here, mainly to demonstrate the capabilities of the extraction algorithm and that of the hysteresis current controller in injecting the com-

pensating current. The result will also demonstrate the inability of the topology, viz. only Parallel Active Filter, in compensation at the fast transitions, characteristic of the current source nonlinear loads. The basic hysteresis with free switching is considered in **Case-1** and **Case-2**; sampled Hysteresis is considered in **Case-3**.

Case -1 (A.4)

The relevant current and voltage waveforms are shown in Figure 5.31 and Figure 5.32.

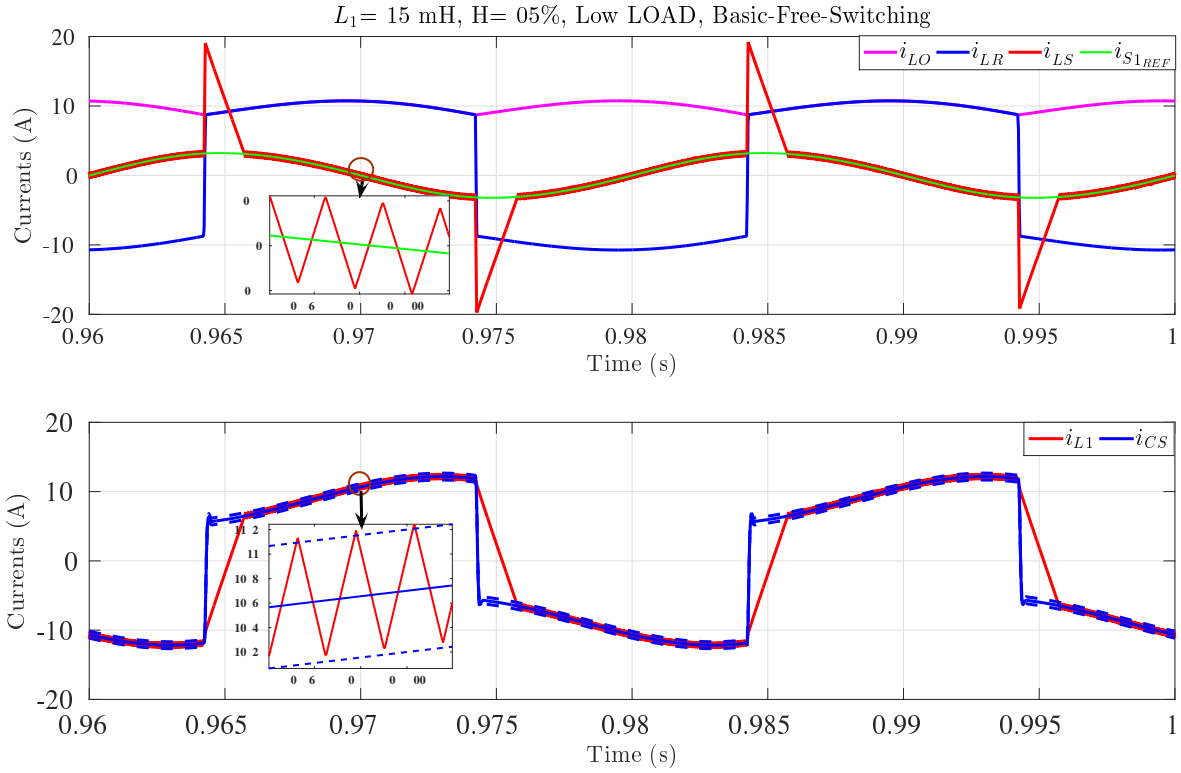

Figure 5.31: Time domain current waveforms for Case-1

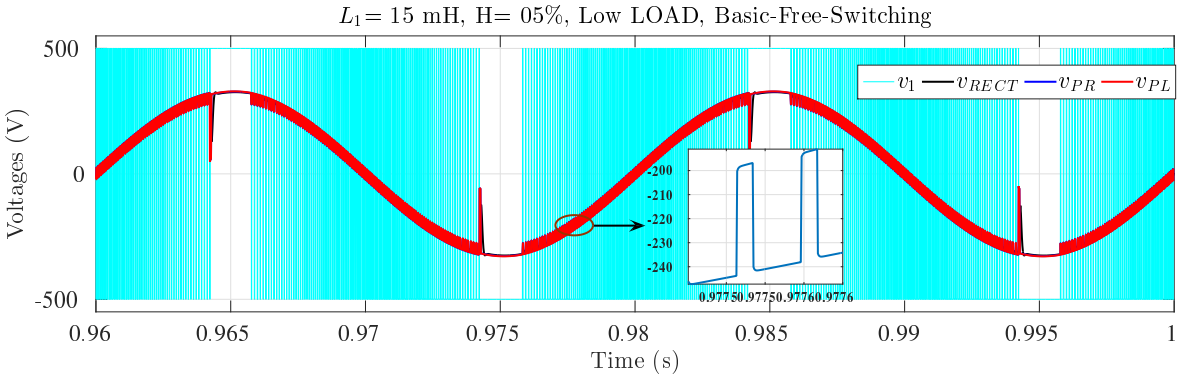

Figure 5.32: Time domain voltage waveforms for Case-1

Case-2 (A.4)

The relevant waveforms are shown in Figure 5.33. This is similar to the **Case-1** above, but for change in the load, $E_O = 110$ V.

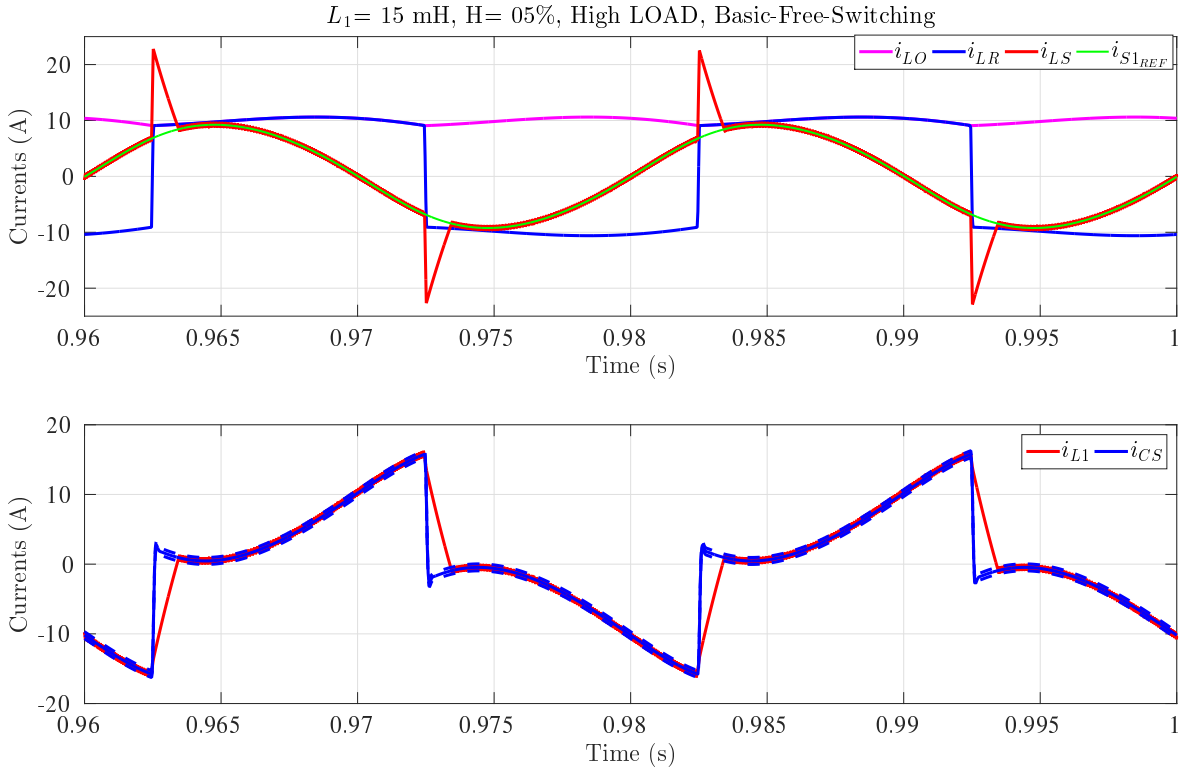

Figure 5.33: Time domain current waveforms for Case-2

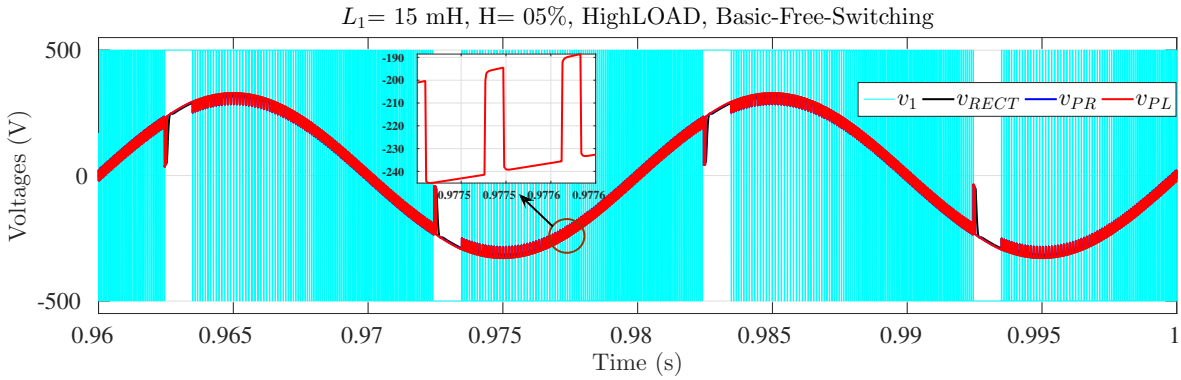

Figure 5.34: Time domain voltage waveforms for Case-2

Case-3 (A.4)

The results from the Basic Hysteresis with a Sampled Switching implementation is given below. The sampling frequency is $f_{sw} = 15$ kHz.

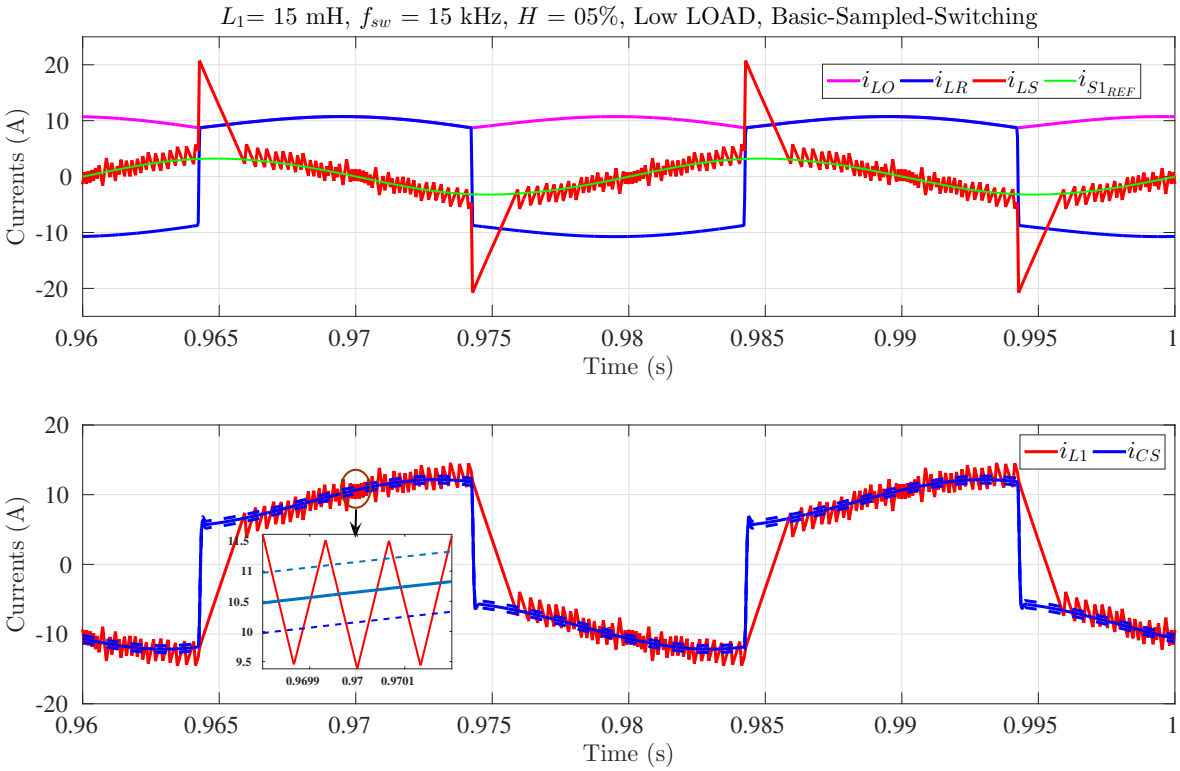

Figure 5.35: Time domain current waveforms for Case-3

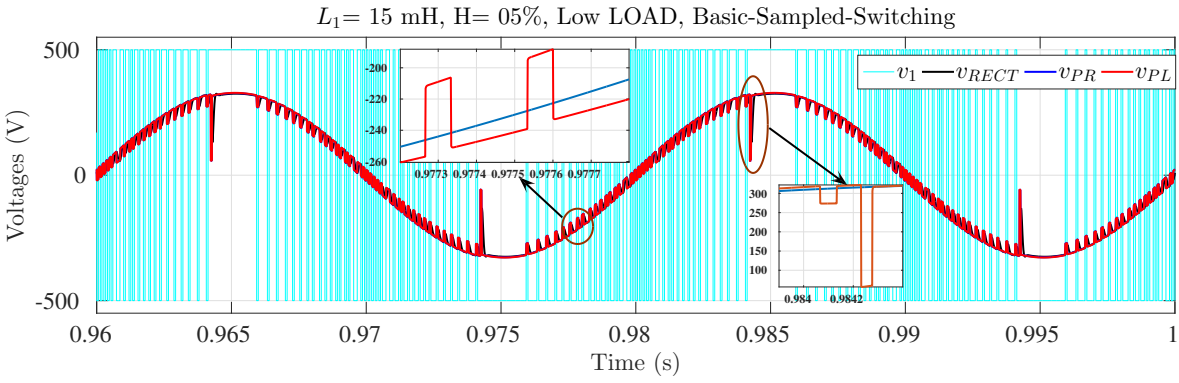

Figure 5.36: Time domain voltage waveforms for Case-3

Observation:

The i_{L_S} follows the set reference ($i_{S1_{REF}}$) except at the transitions and is the major cause of distortion. This is the limitation of compensation with only the PAF in addition to the added reactive power it has to supply. The voltage at PCC, v_{PL}, has

the share of v_1 superimposed with that from the source v_S. There will be line-notching at the current transitions. It may be noted that the PAF compensates completely except at the transitions. This is only to show the effectiveness of the compensation extraction algorithm and that of the controller along with the Hysteresis control for injection of compensating current. The system works reliably under all conditions as will be shown with more results to follow.

5.9.2 Case-4: Results with only Parallel Passive Filter(A.4)

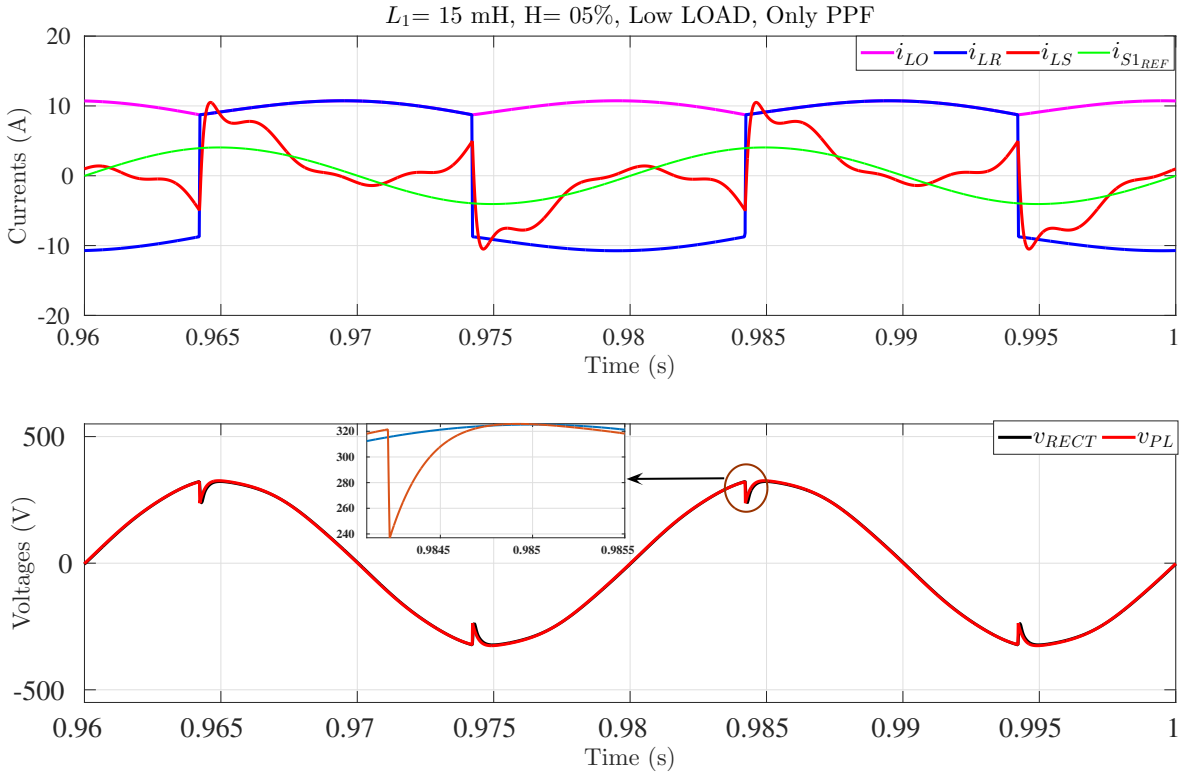

Figure 5.37: Time domain current and voltage waveforms for Case-4

This is a typical result under all working conditions. The source current is very much distorted, though the line voltage is not much distorted. There is a need to suppress the fast transitions of the current, which is possible only through a series reactor, as will be shown next.

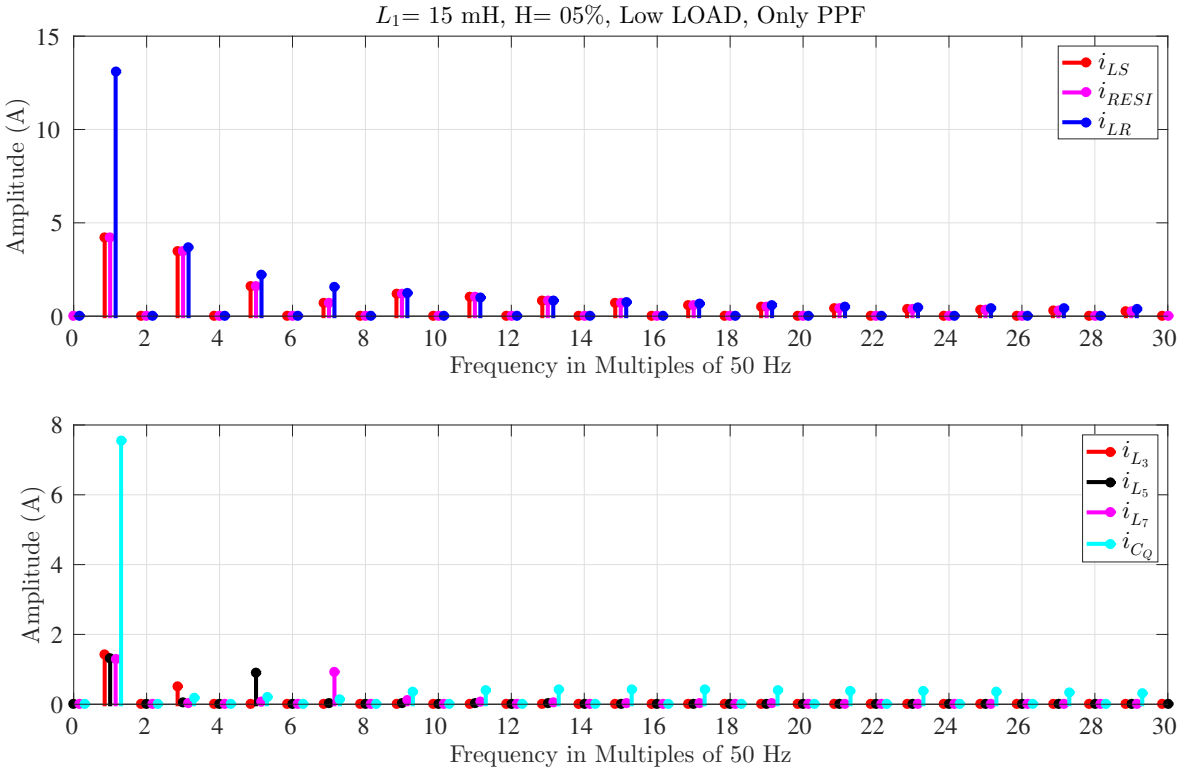

Figure 5.38: Spectrum of current waveforms for Case-4

5.9.3 Case-5: Results with only Series Passive and Parallel Passive Filters

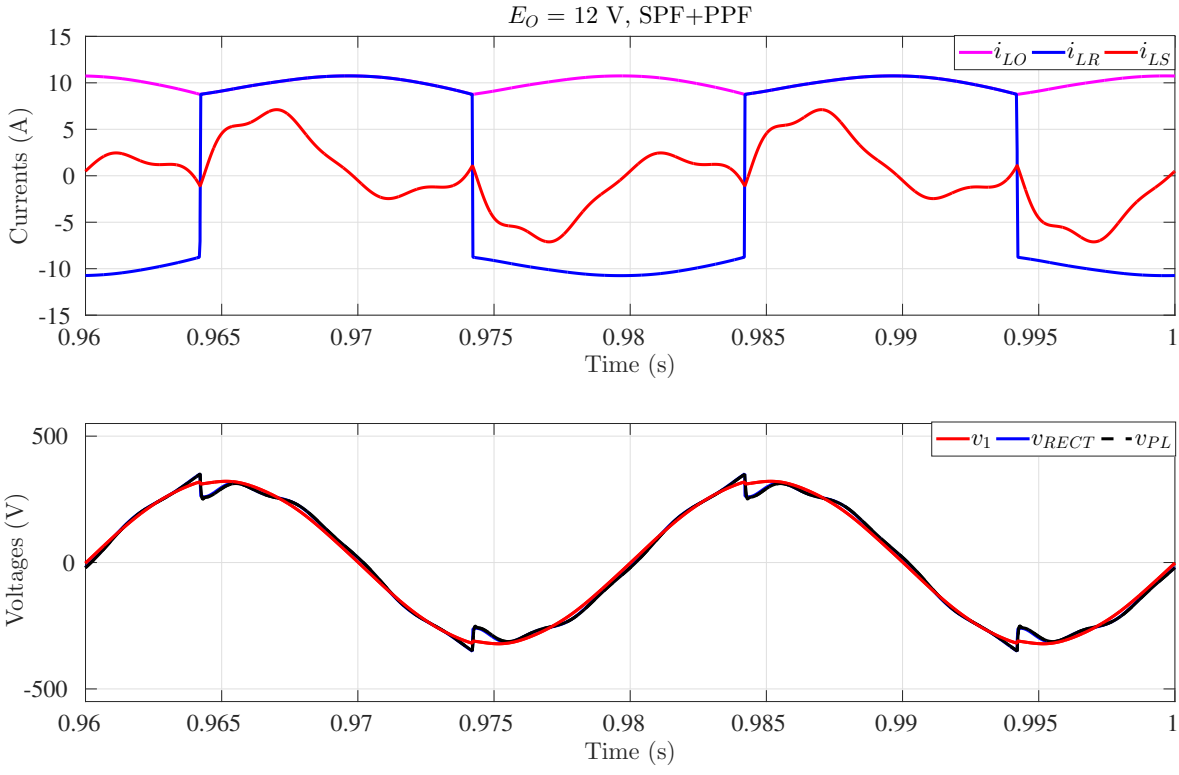

Figure 5.39: Time domain current and voltage waveforms for Case-5

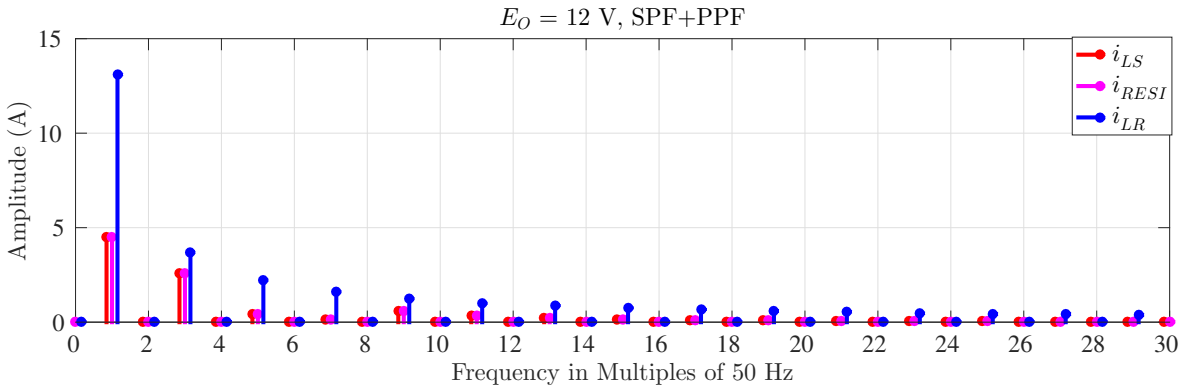

Figure 5.40: Spectrum of current waveforms for Case-5

The source current transition has softened due to the series reactor. The resulting residual current may be compensated for harmonics using the PAF as will be demonstrated in the following. But before that a study with only PAF and PPF is given in the following section.

5.9.4 Results with only PAF and PPF

Case-6 (A.4)

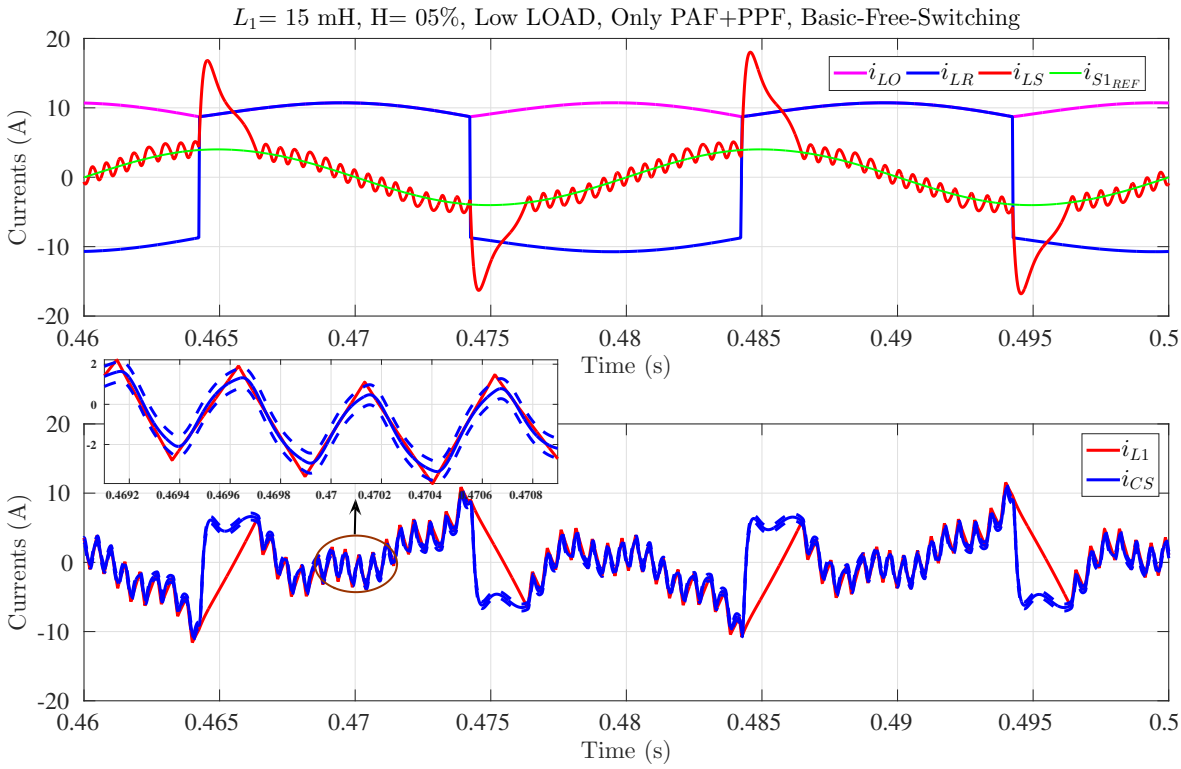

Figure 5.41: Time domain current waveforms for Case-6

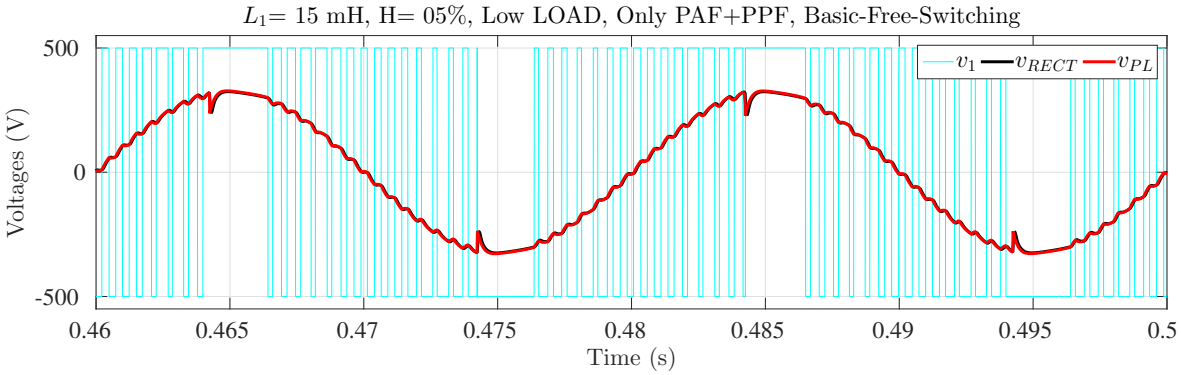

Figure 5.42: Time domain voltage waveforms for Case-6

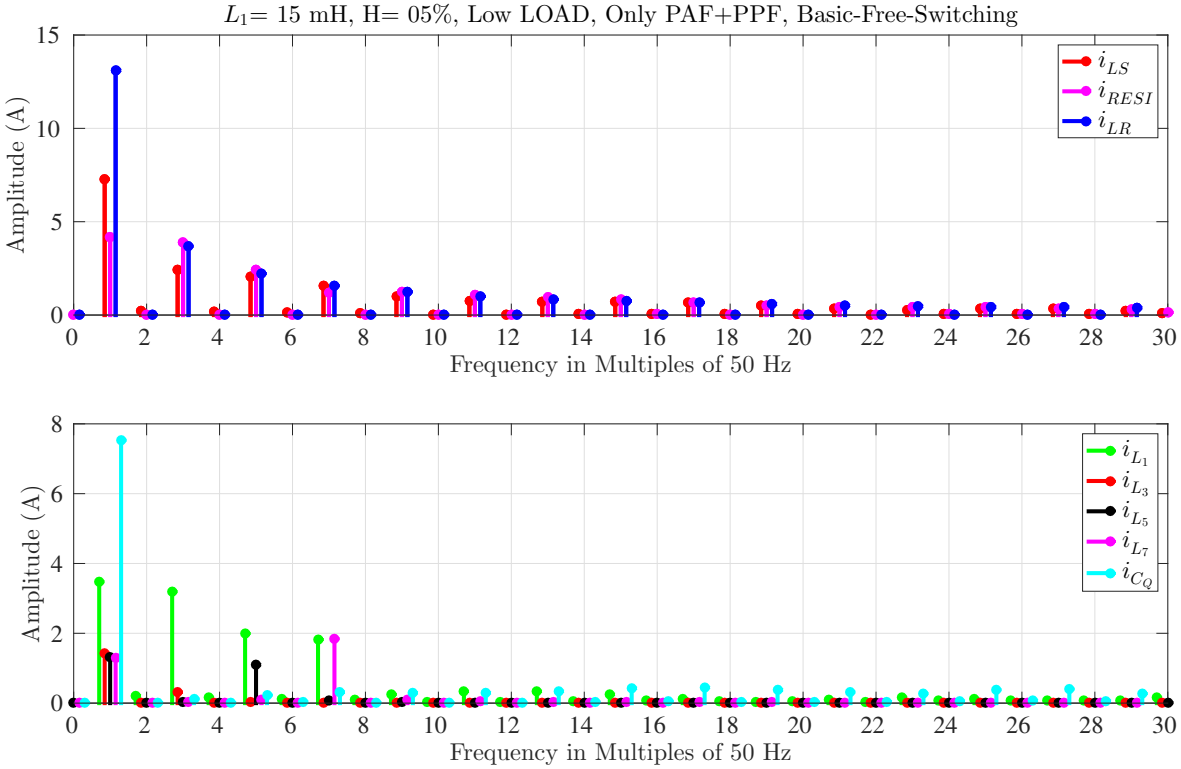

Figure 5.43: Spectrum of current waveforms for Case-6

Observation:

The connection of the PAF in shunt with the tuned filter and the Capacitor results in a ripple in the residual current i_{RESI}, which in turn determines the switching frequency, for a given L_2, with any of the variants of the hysteresis controller considered here. The source current still contains the spikes at the transitions. This can be arrested only with Power-Shield, a topology with PAF, SPF, and PPF incorporated in that order from source towards the load side. The results with Power-Shield are presented in the following section.

Conclusion:

Thus it is obvious that all the above considered topologies like, only PAF, only PPF, SPF with PPF, or PAF with PPF does not mitigate the harmonics and reactive power meeting the standards' specifications. It will be shown in the following that Power-Shield – a combination of PAF, SPF, and PPF will meet the requirements.

5.9.5 Results with Power-Shield: PAF, SPF, and PPF

Case-7 (A.4)

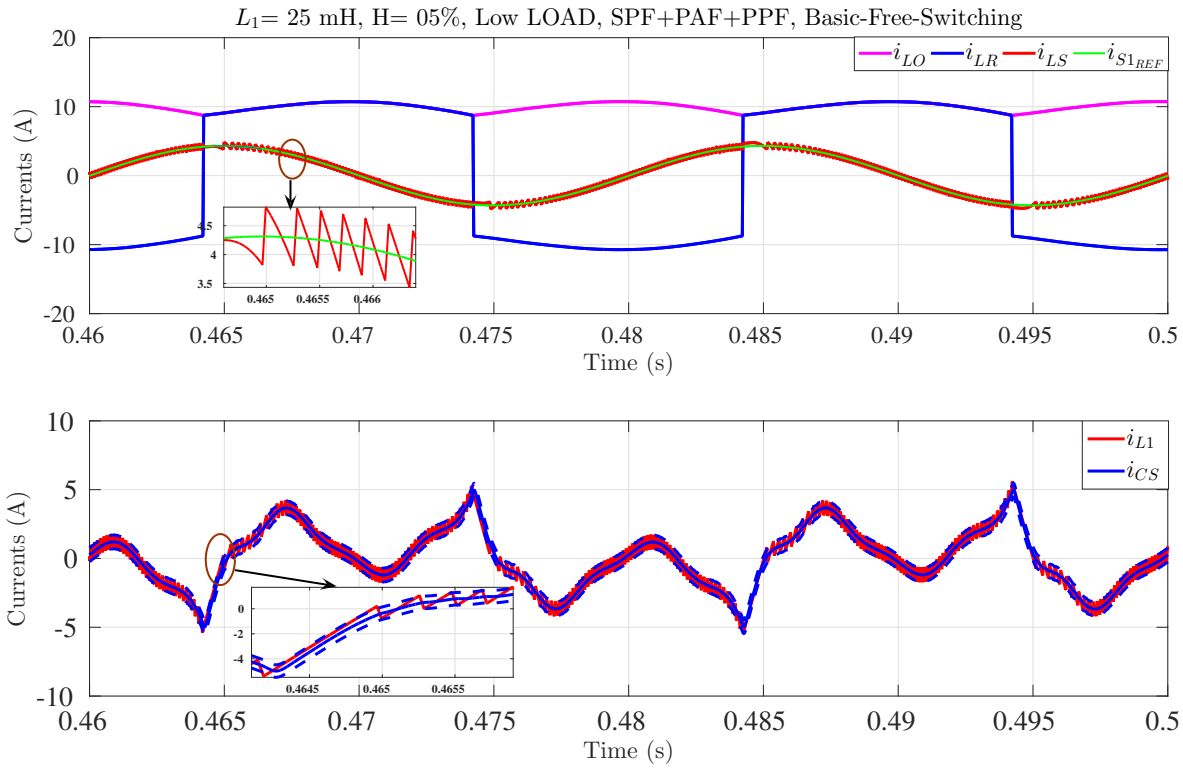

Figure 5.44: Time domain current waveforms for Case-7

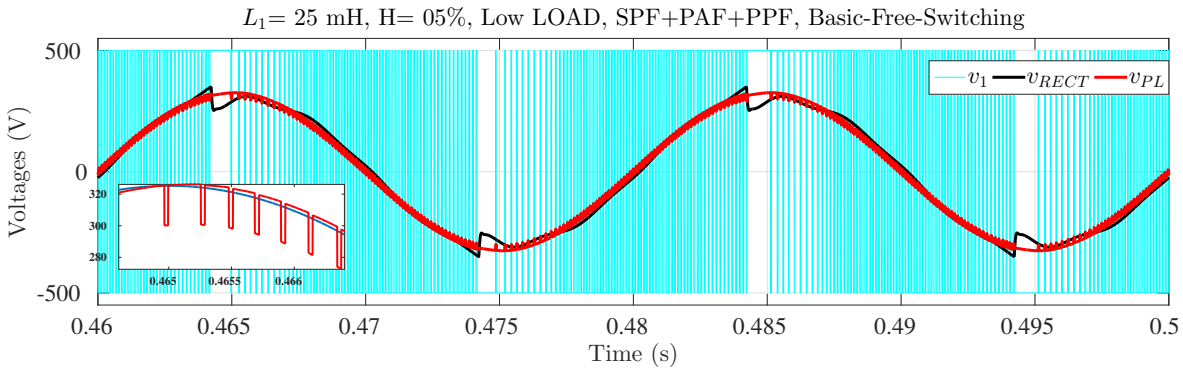

Figure 5.45: Time domain voltage waveforms for Case-7

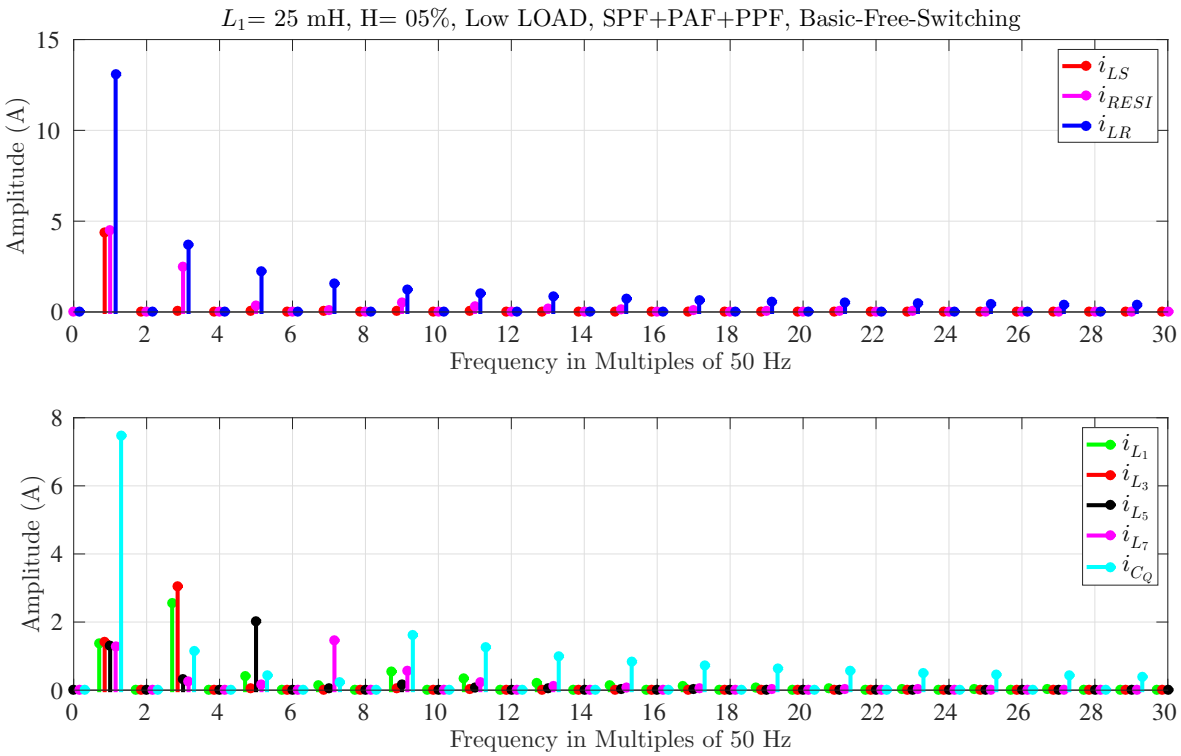

Figure 5.46: Spectrum of current waveforms for Case-7

It may be observed that the source current is close to a sinusoid, though theoretical due to the free running hysteresis, with 5% band, resulting in a high switching frequency. This is however chosen to demonstrate the effectiveness of the overall system in mitigating the harmonics and supplying the reactive power, rendering a source current very close to a sinusoid and in-phase with the source voltage. The voltage at PCC is distorted with a reflection of the PAF voltage, but within acceptable limits (Table 5.4). More results are presented in the following.

Case-8 (A.4)

For this case R_Q is set to 50 mΩ and the series compensator is configured as a series inductor only, with an intension to reduce the losses. The results presented in the Figures 5.47-5.48 and the Table 5.4 reveal that the compensation is good enough and the loss in the reactive power compensator and that of the series compensator has dropped. However the THD of the voltage at PCC is outside the desired limits.

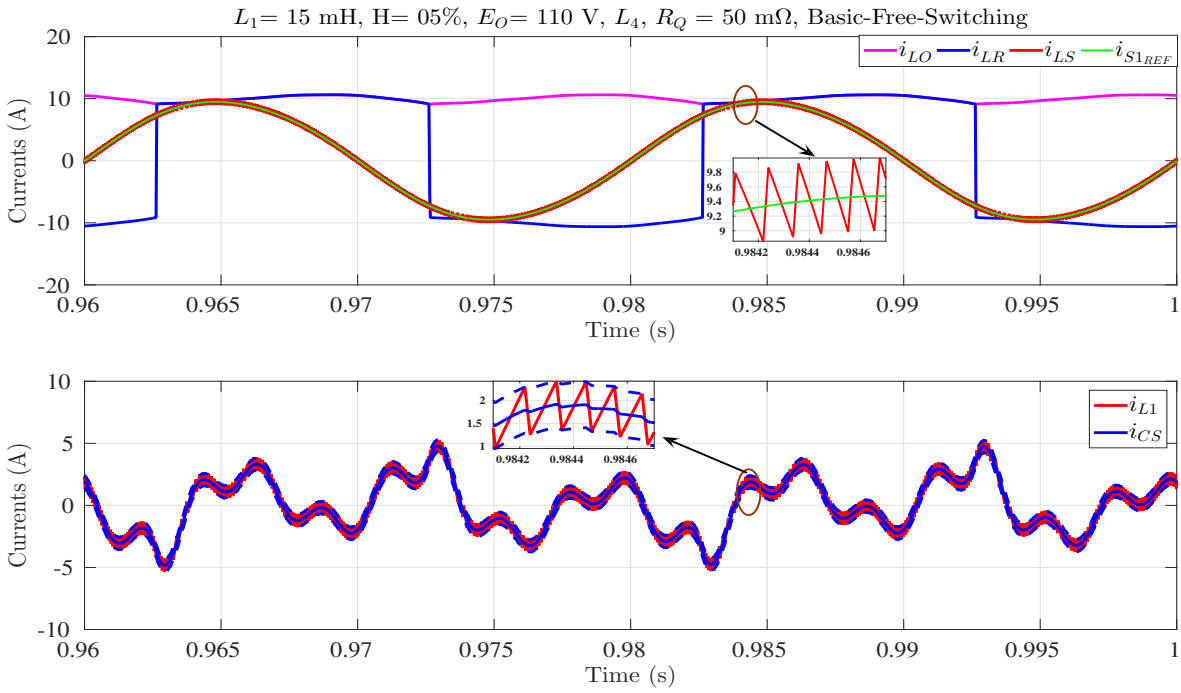

Figure 5.47: Time domain current waveforms for Case-8

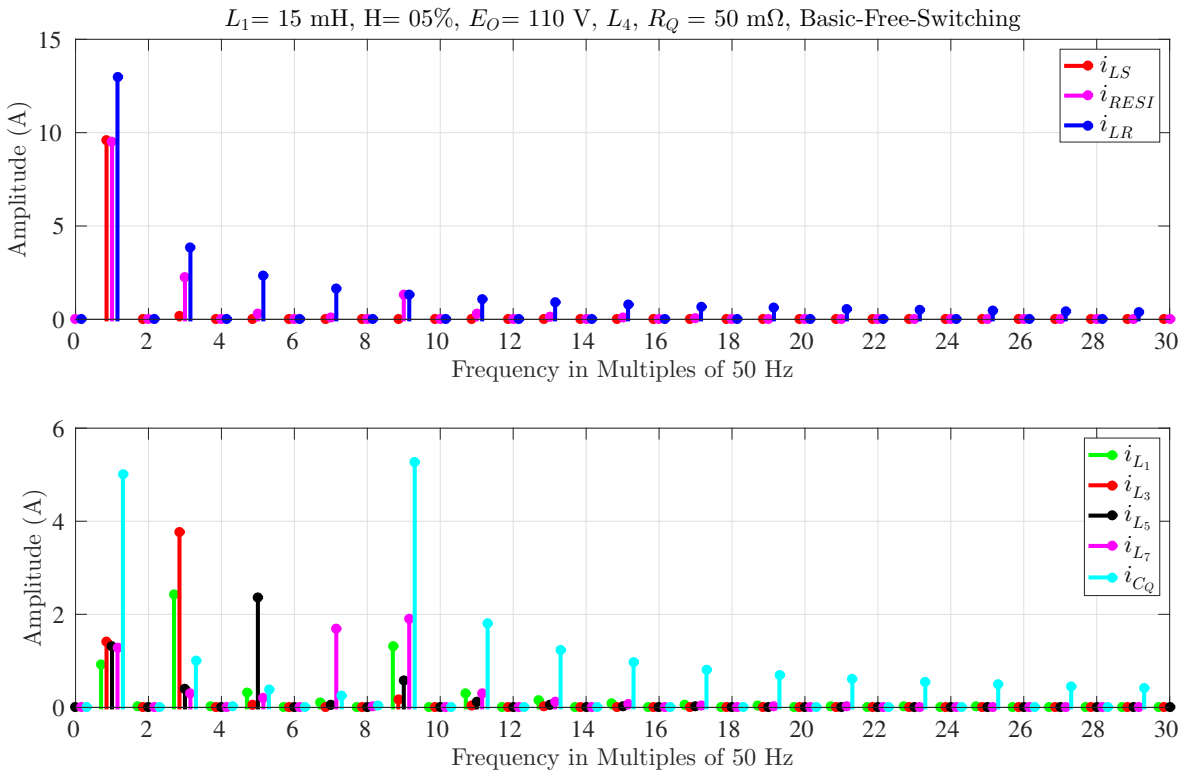

Figure 5.48: Spectrum of current waveforms for Case-8

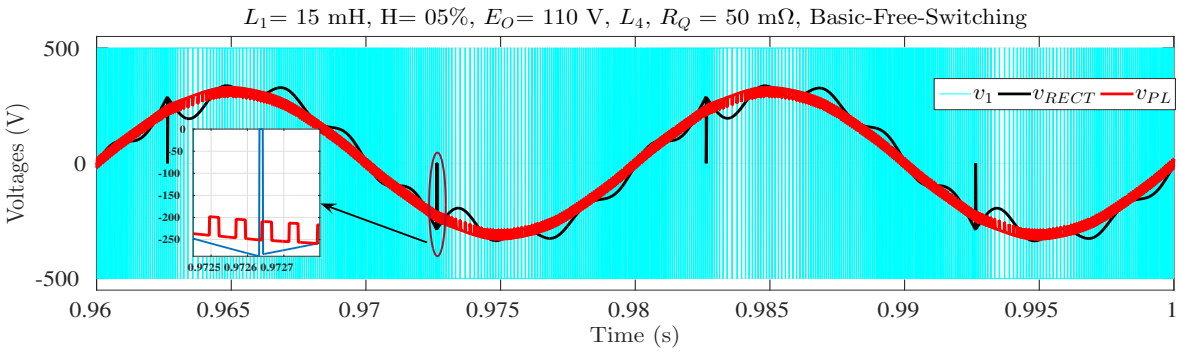

Figure 5.49: Time domain voltage waveforms for Case-8

Case-9 (A.4)

The load is E_O = 70 V and Scheme-2 hysteresis is considered. The R_Q is set to 50 mΩ but the series compensator is with the coupled transformer arrangement. There will be additional losses due to the circulation of currents in the converter side of the transformer. The THD of the voltage at the PCC is within limits.

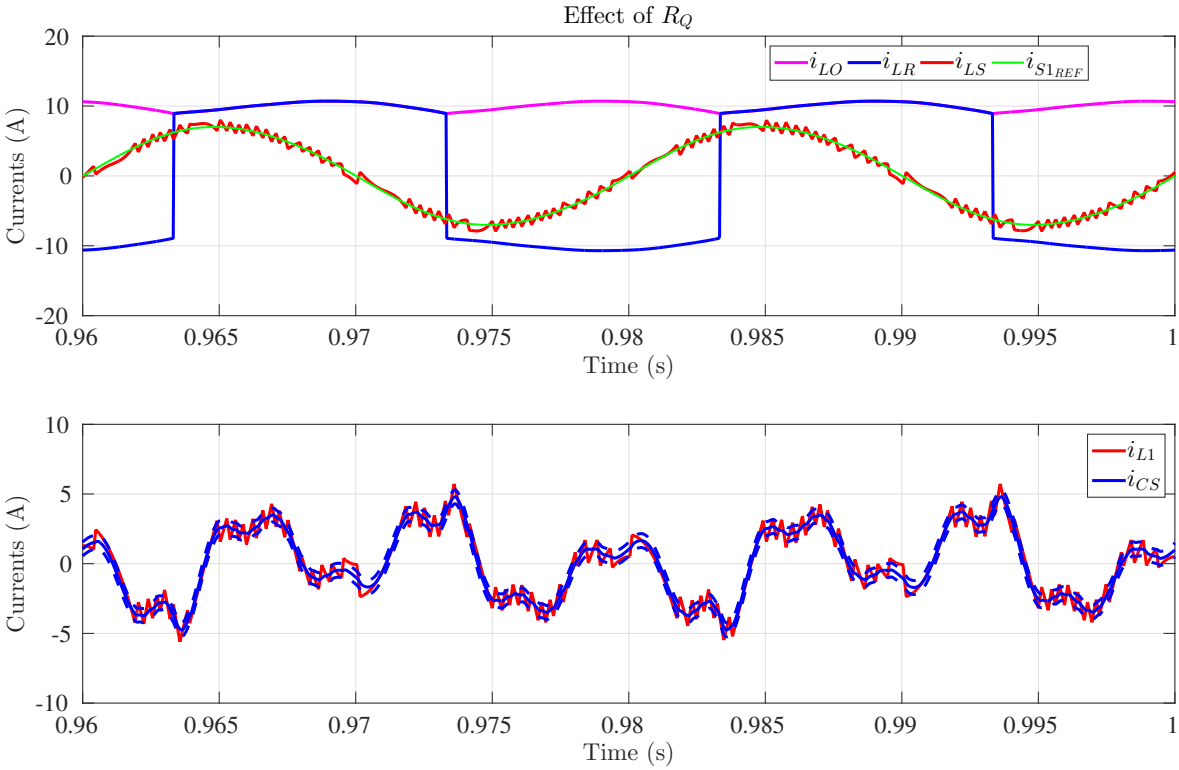

Figure 5.50: Time domain current waveforms for Case-9

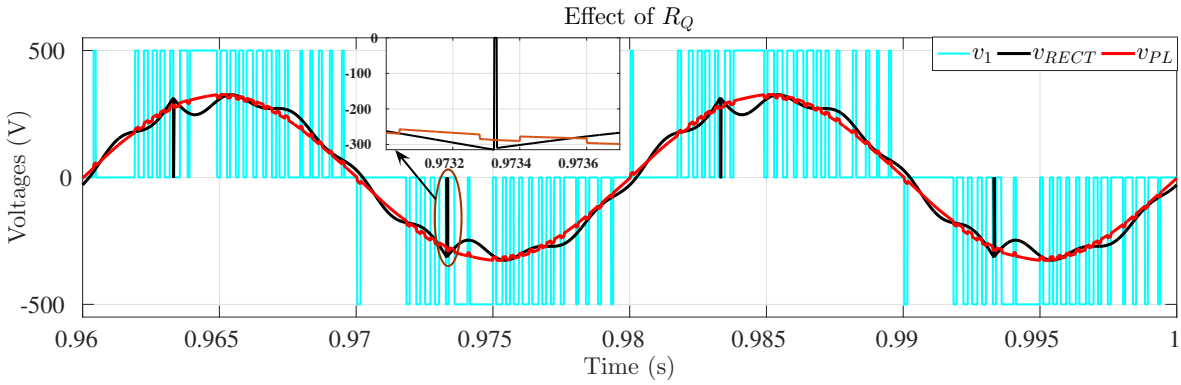

Figure 5.51: Time domain voltage waveforms for Case-9

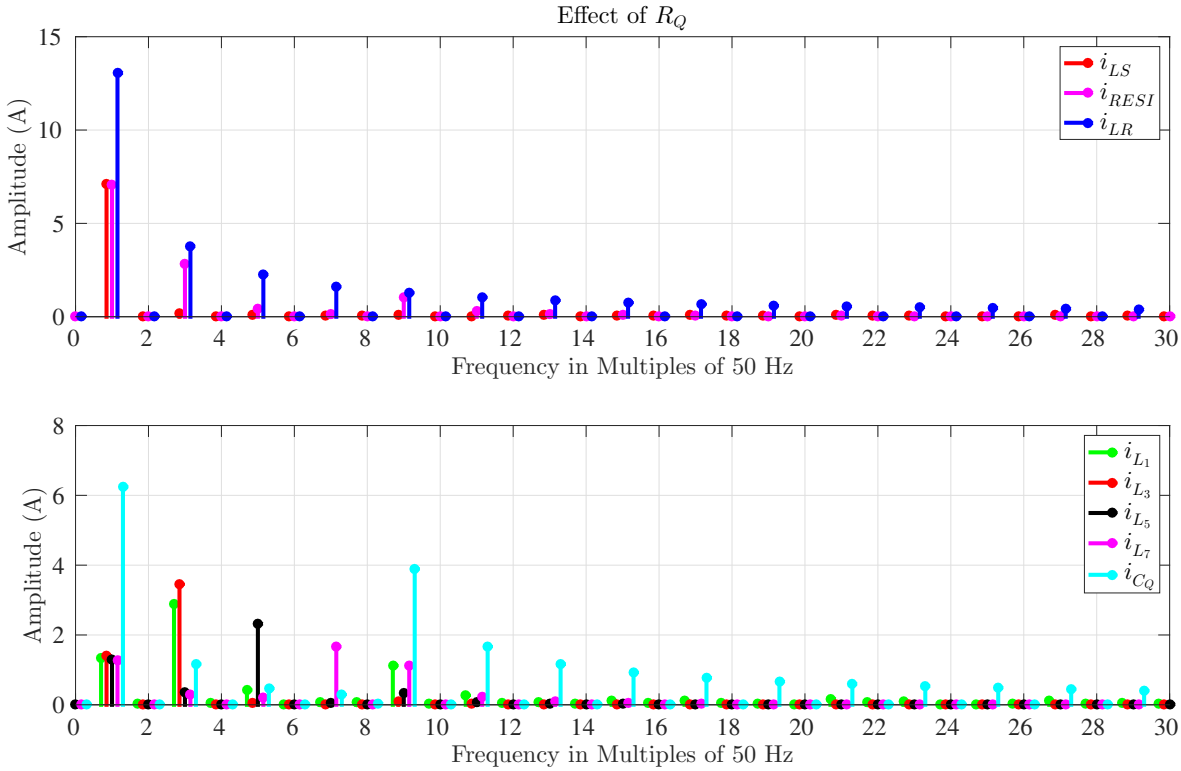

Figure 5.52: Spectrum of current waveforms for Case-9

Case-10 (A.4)

The load is E_O = 162 V and Scheme-2 hysteresis is considered. The effect of large load is studied in this case. The extended commutation-overlap is seen. The effect of extended overlap on the reduction of the reactive power demand may be observed by comparison with the results from **Case-11**.

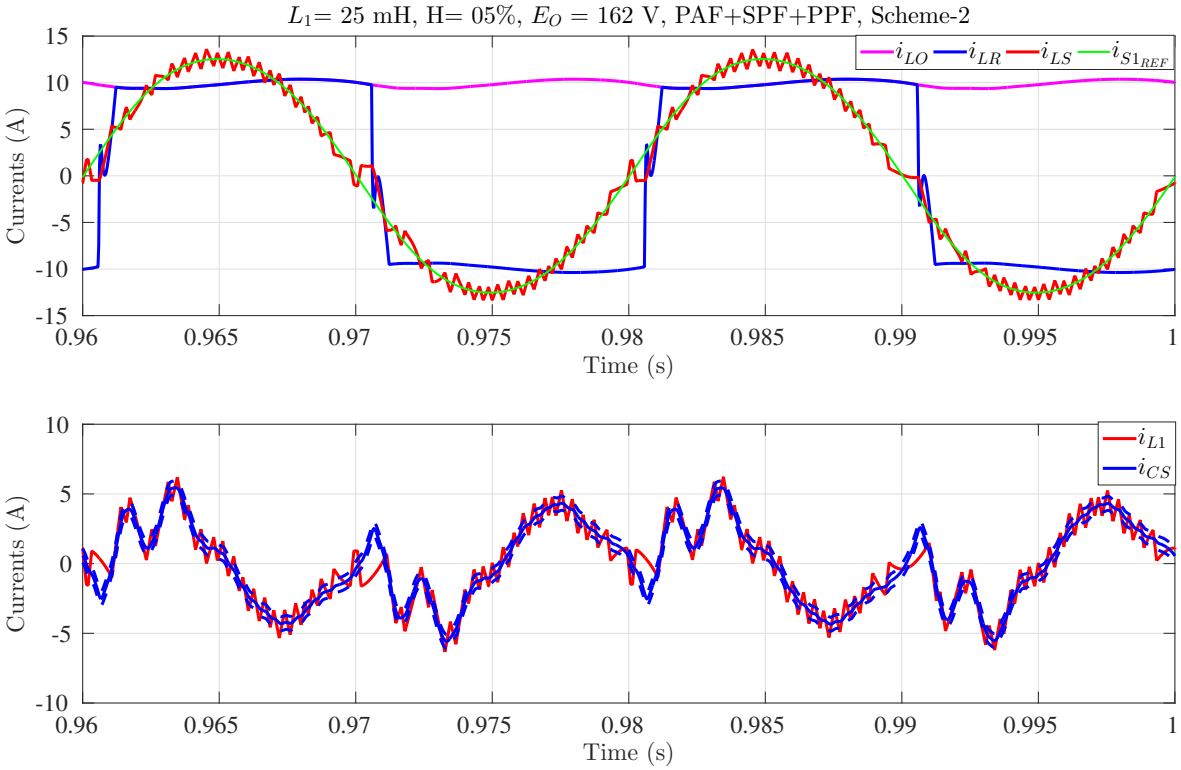

Figure 5.53: Time domain current waveforms for Case-10

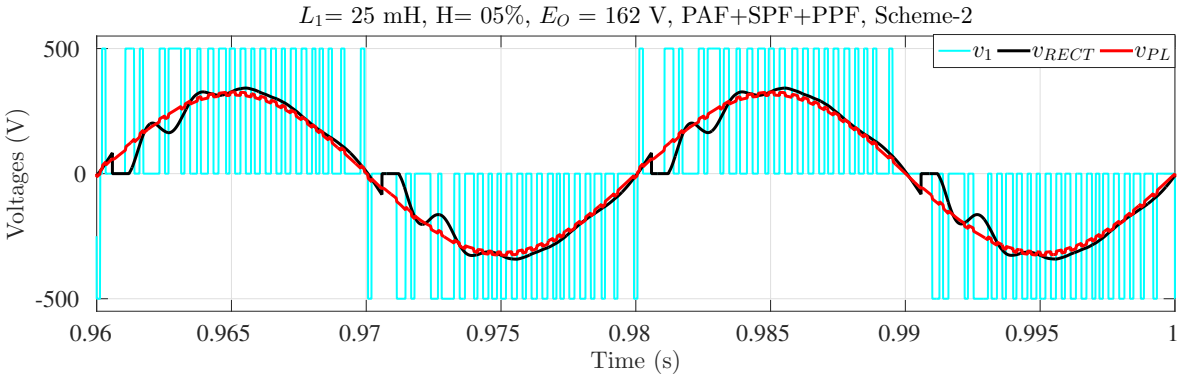

Figure 5.54: Time domain voltage waveforms for Case-10

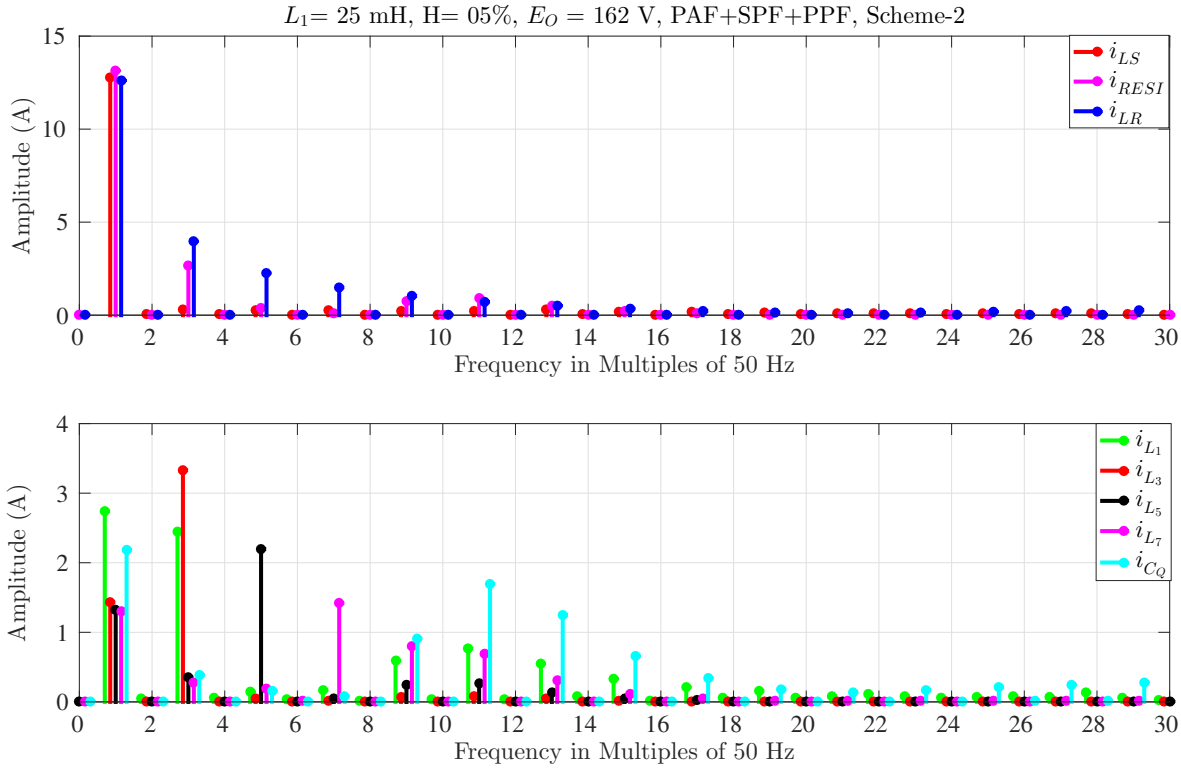

Figure 5.55: Spectrum of current waveforms for Case-10

Case-11 (A.4)

With the load at E_O = 162 V and Scheme-2 hysteresis the C_Q is switched OFF. The fundamental current compensated by the active filter is about 0.5 A (Figure 5.58), in comparison with that of **Case-10**, wherein it is 2.75 A (Figure 5.55). It is because the compensation (C_Q) provided is in excess of what is actually required. The extended commutation makes the rectifier input current trapezoidal, hence reduces the fundamental current, and the reactive power demand.

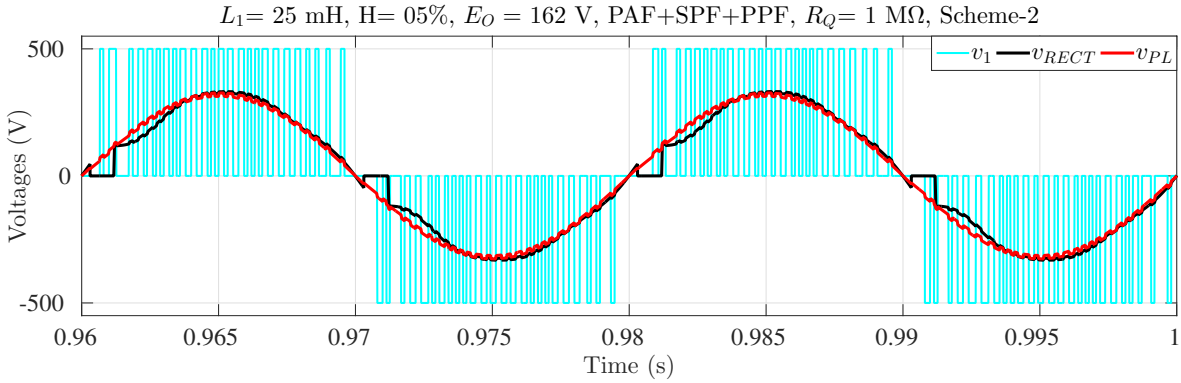

Figure 5.56: Time domain voltage waveforms for Case-11

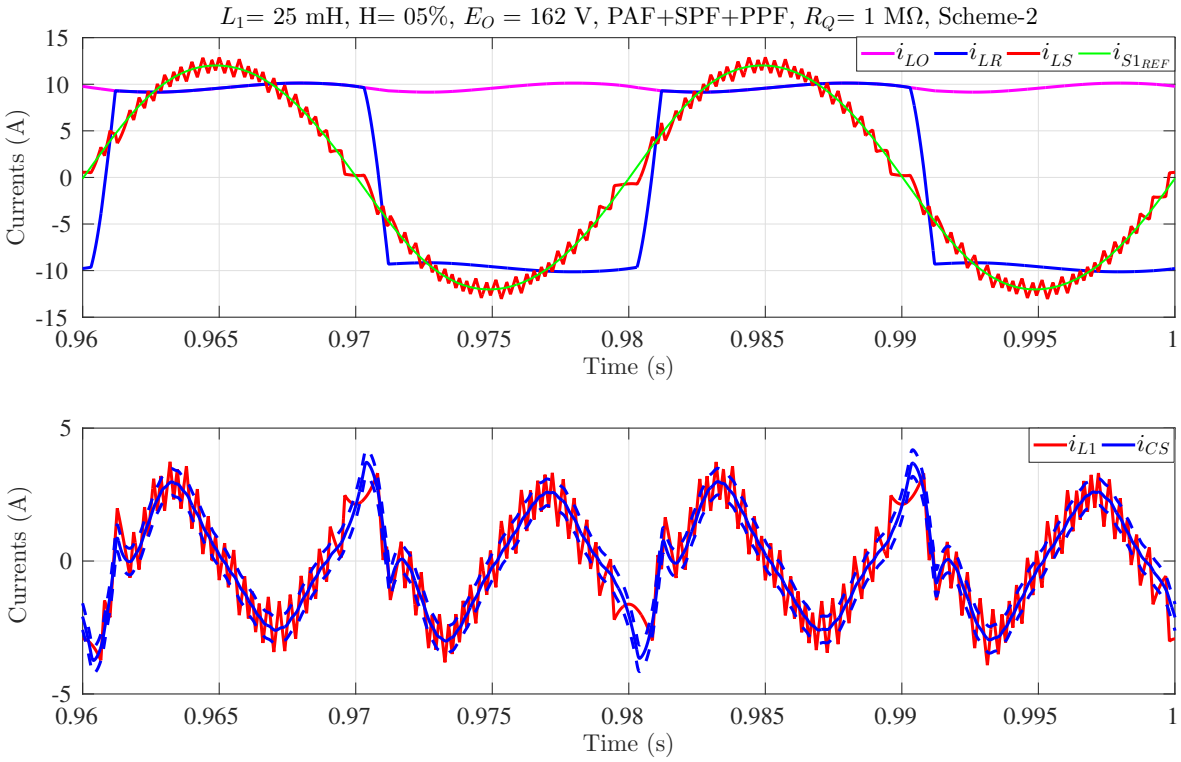

Figure 5.57: Time domain current waveforms for Case-11

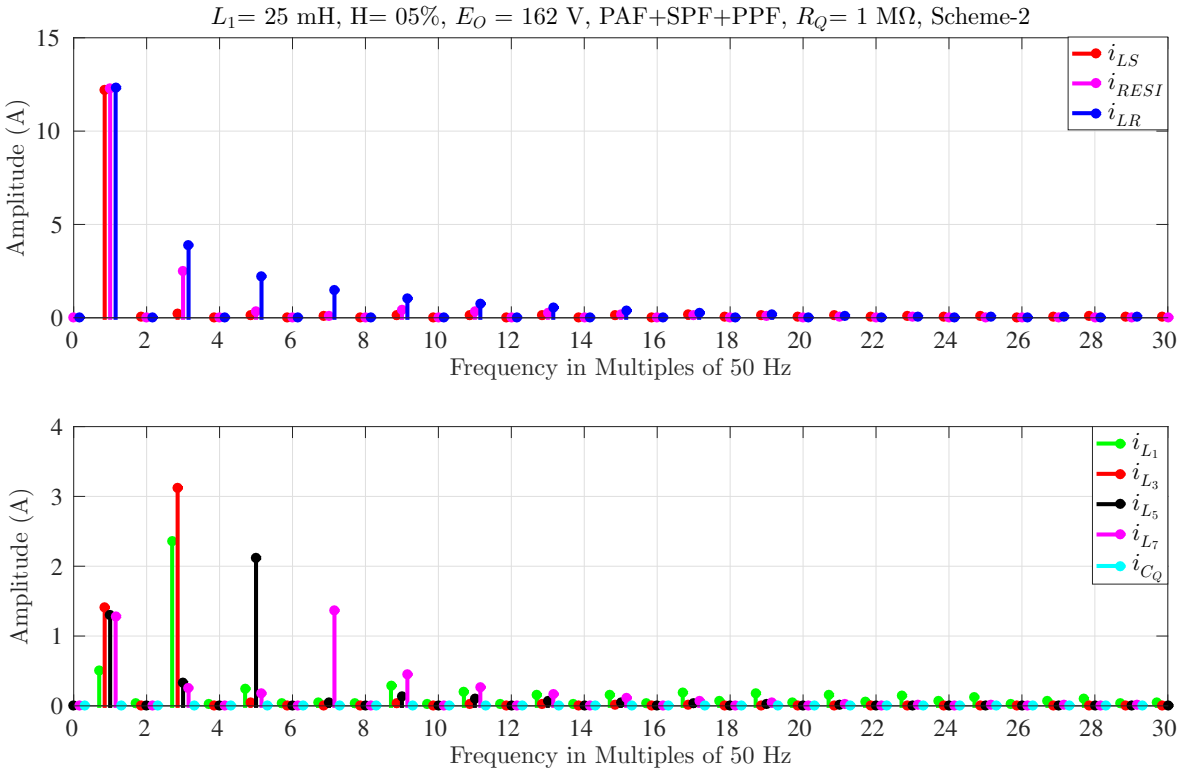

Figure 5.58: Spectrum of current waveforms for Case-11

Case-12 (A.4 and A.1.1):

Another case with a higher power requirement is presented here. The results are as shown in Figures 5.59 – 5.61 and in Table 5.4. All performance parameters are within the desirable range.

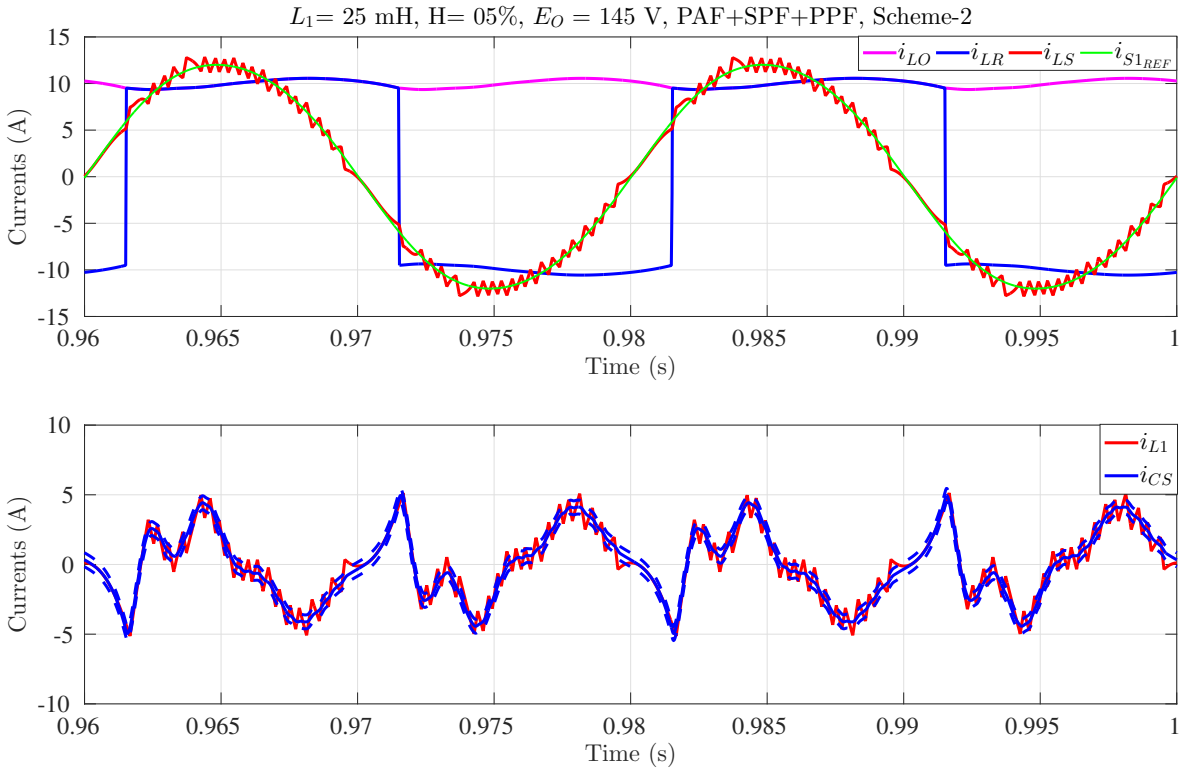

Figure 5.59: Time domain current waveforms for Case-12

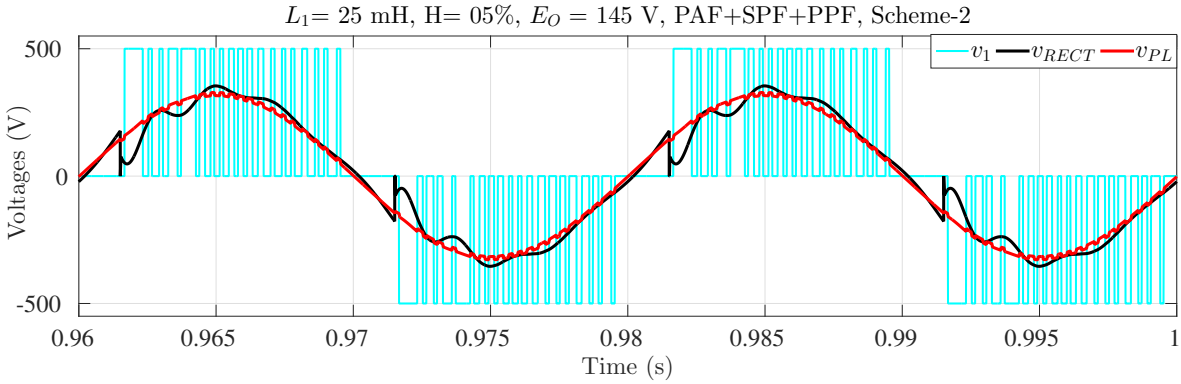

Figure 5.60: Time domain voltage waveforms for Case-12

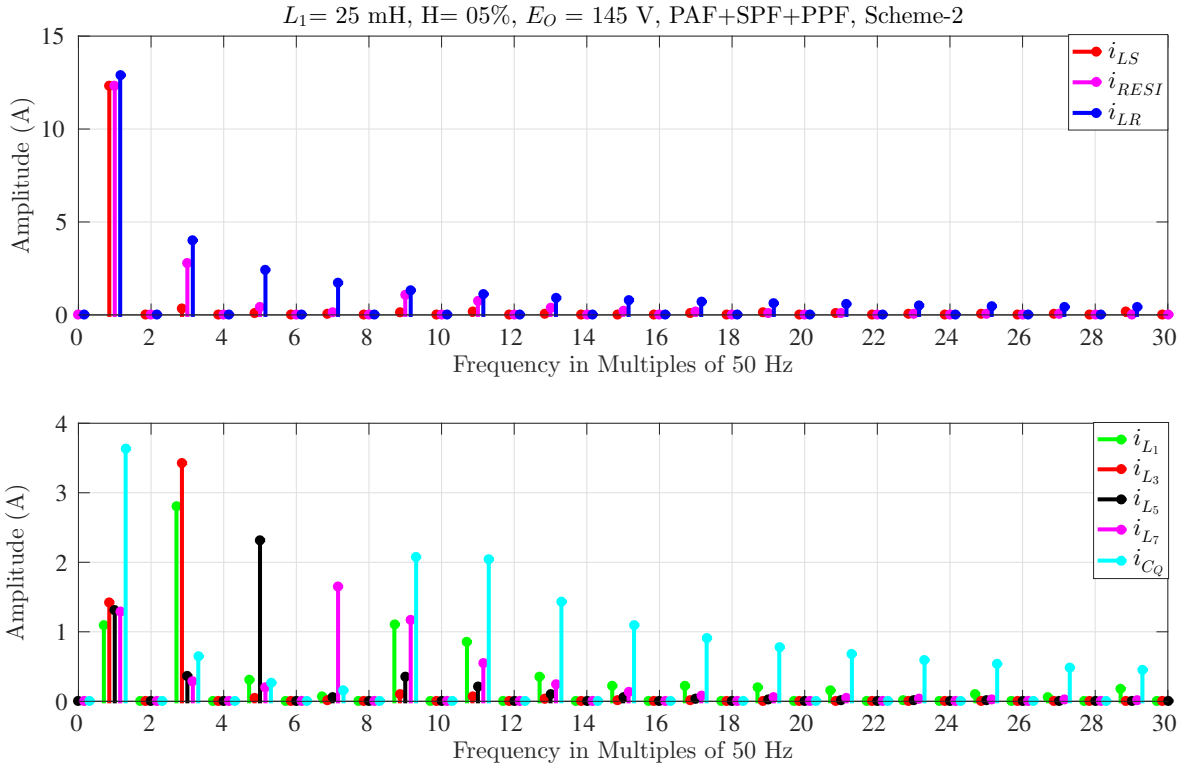

Figure 5.61: Spectrum of current waveforms for Case-12

Case-13 (A.4)

This example is a repetition of **Case-12**, with an over compensation for the reactive power where a capacitance of $C_Q = 50$ μF is inserted while the requirement is only $C_Q = 36$ μF. The effect of this excess compensation may be seen in the increase in the fundamental value of the PAF current i_{L_1} as shown in Figure 5.64 from that in Figure 5.61. So the excess reactive power generated in the overall system is absorbed by the PAF.

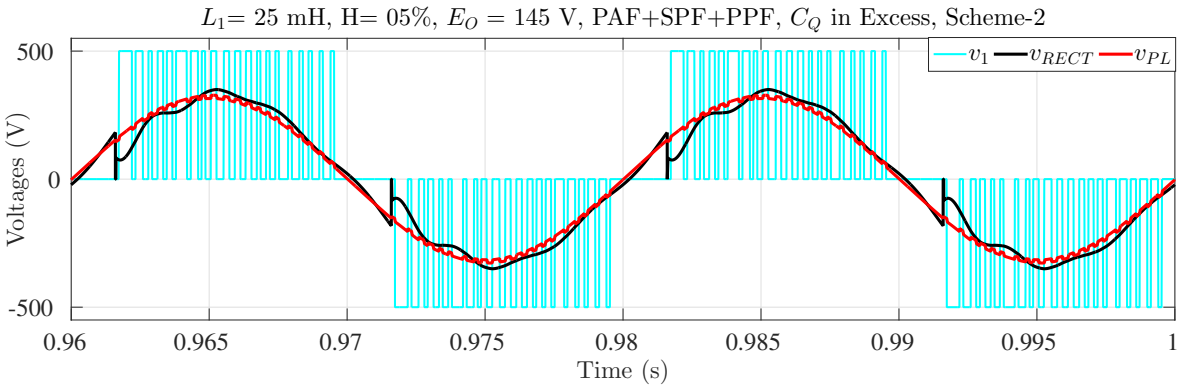

Figure 5.62: Time domain voltage waveforms for Case-13

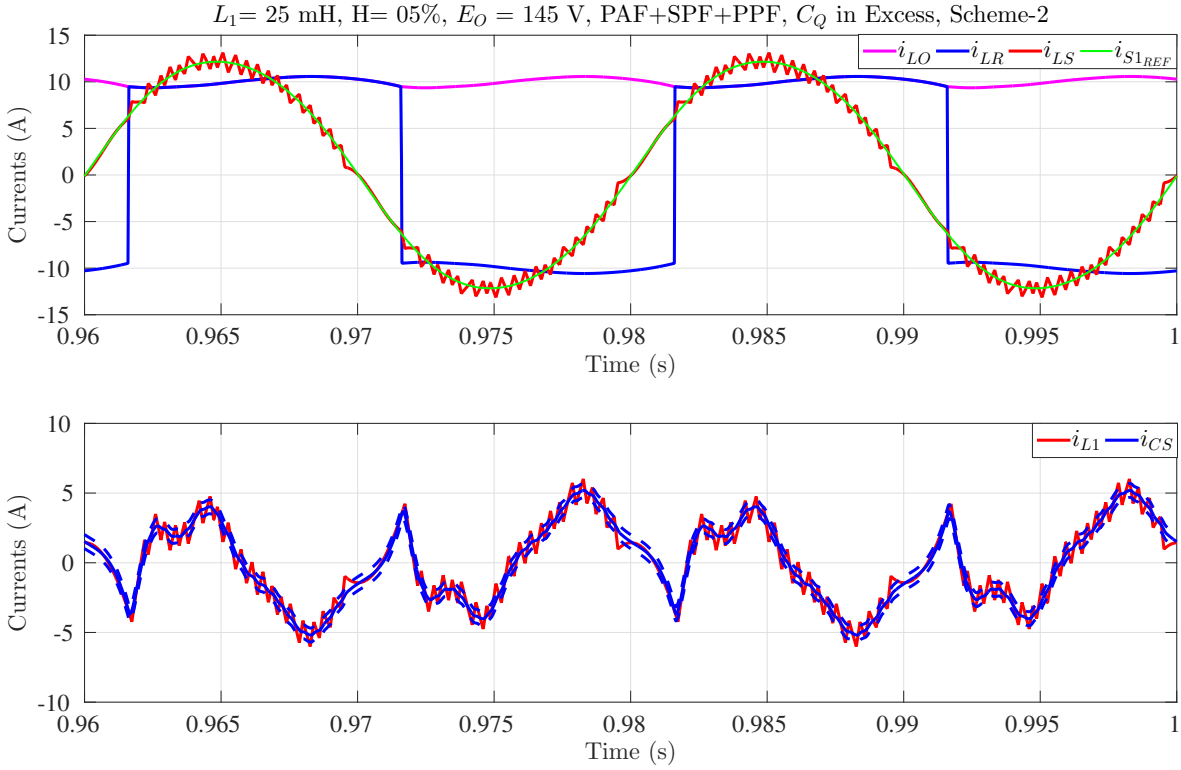

Figure 5.63: Time domain current waveforms for Case-13

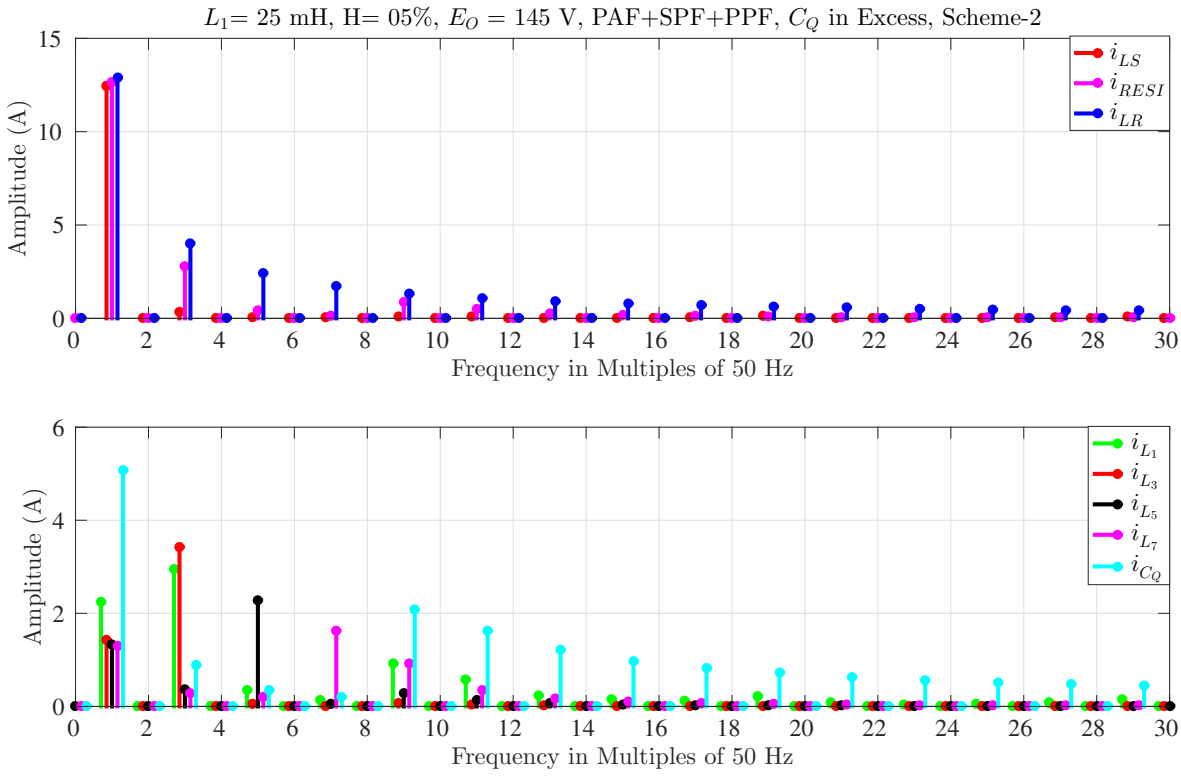

Figure 5.64: Spectrum of current waveforms for Case-13

Case-14 (A.4)

The following two results correspond to the ones emerging by the adoption of the switching **Scheme-1** to the **Case-9**. In the results shown in Figure 5.65, it may be

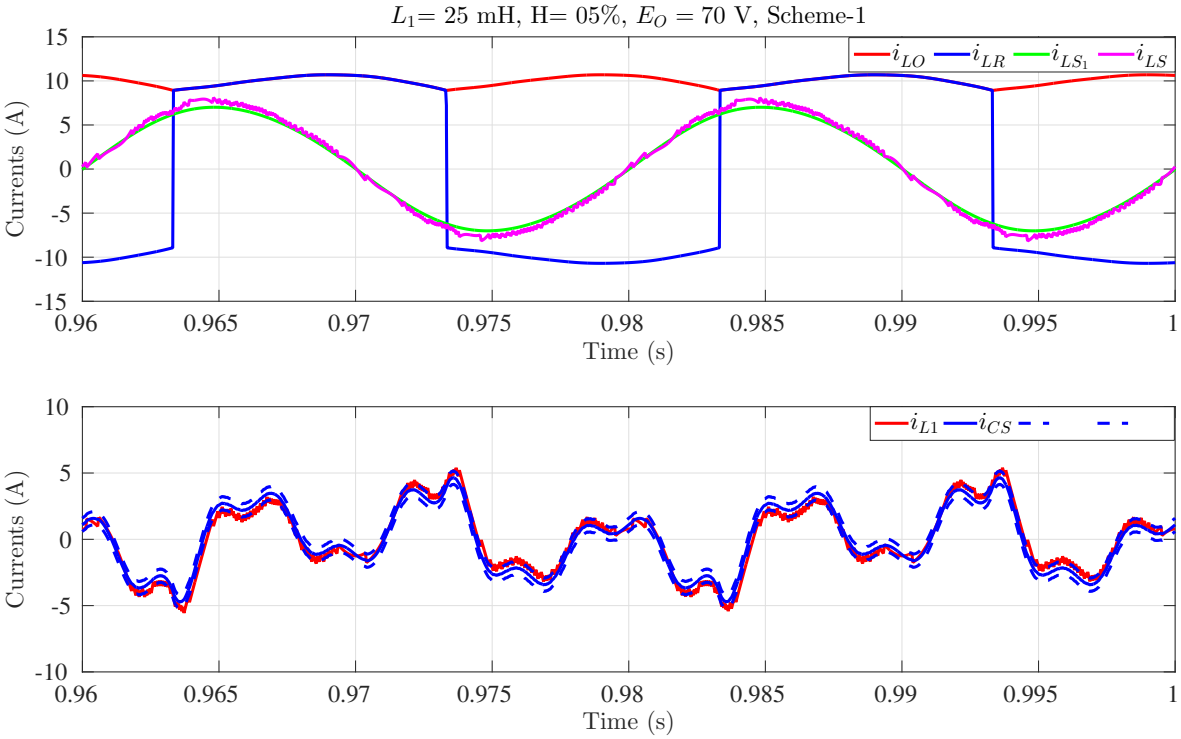

Figure 5.65: Time domain current waveforms for Case-14

observed that the source current i_{LS} deviates from the set reference current slightly. This is caused by the indirect implementation of the VSI source voltage control for the PAF; it being achieved by means of regulating the power flow from/to the VSI. It is observed that the **Scheme-1** needs an extra control effort compared to **Basic hysteresis** or the **Scheme-2**. After adjusting for the VSI power, the results are shown in Figure 5.67. It may be observed that the source current matches with the reference current. The feature of mitigating the harmonics and reactive power however is not hampered by the switching scheme; that feature being the characteristic of the topology and not that dependent on the current injection scheme.

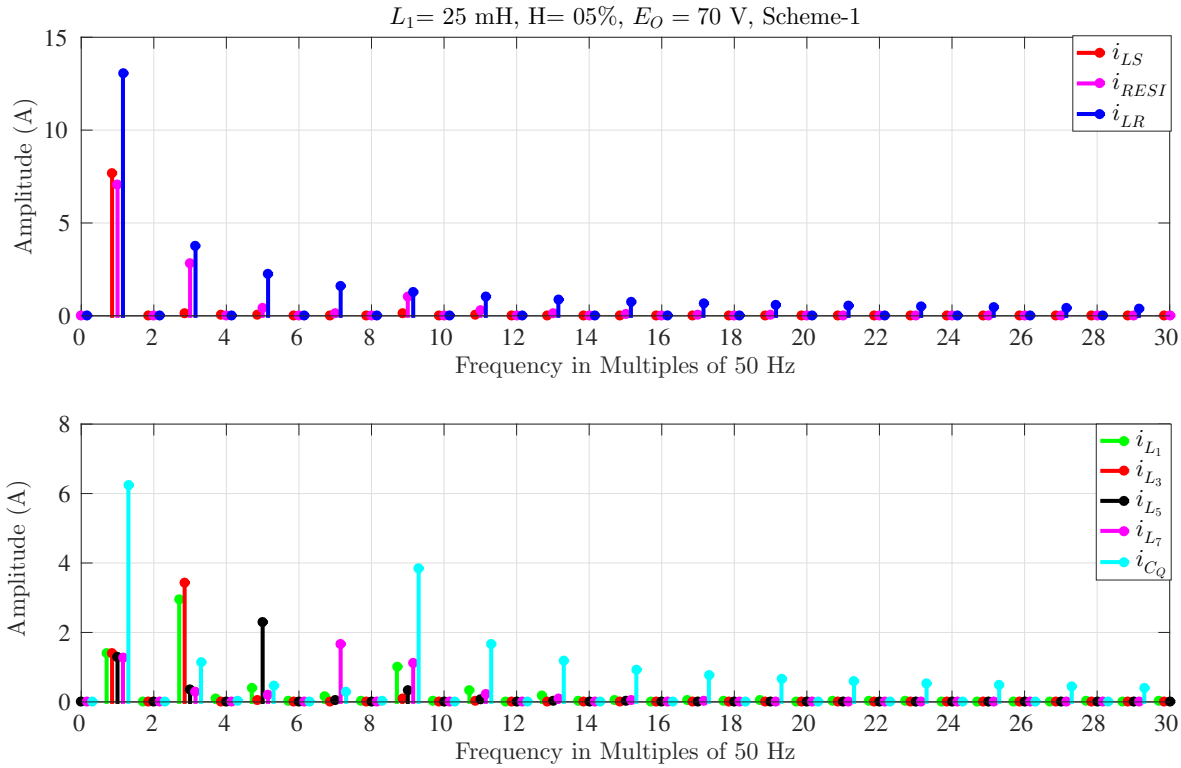

Figure 5.66: Spectrum of current waveforms for Case-14

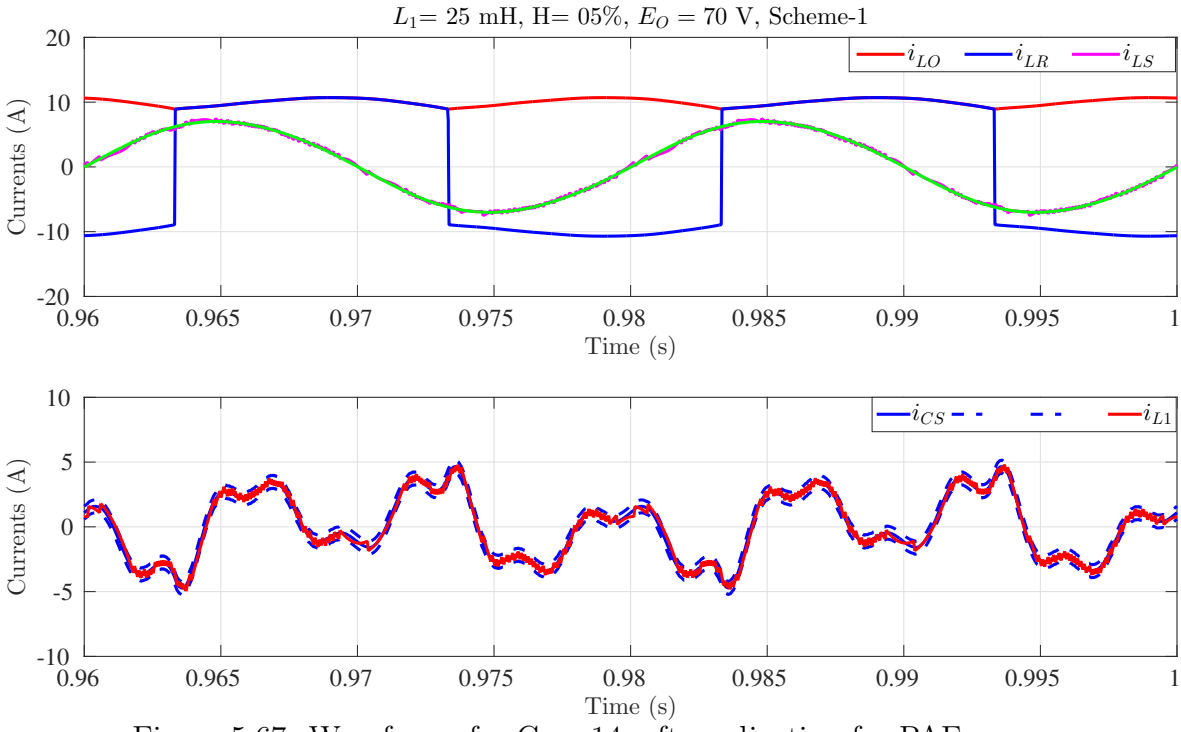

Figure 5.67: Waveforms for Case-14, after adjusting for PAF power

5.9.6 Response during Continuous Load change

The simulation set up is tested for studying its performance during continuous load change. For this purpose a battery charging requirement under constant current charging is simulated. In that case the battery voltage would keep increasing as it charges and the firing angle has to be adjusted to maintain the current. This will lead to change (decrease) in reactive power requirement. Thus C_Q will have to be changed to reduce over/under compensation. The PAF has to continuously change its compensation as dictated by the compensating current extraction program – which also has to correctly calculate under this condition. In practice the battery charging is a slow process – roughly being less than 1 V/ hour. In the simulation study a ramp up of as high as 10 V/s is used, as described in (5.43)

$$\begin{aligned} e_O(t) &= 100 \quad \text{V}, \quad 0 \leq t \leq 1 \text{ s} \\ &= 100 + 10 \cdot t \quad \text{V}, \quad t \geq 1 \text{ s} \end{aligned} \quad . \tag{5.43}$$

The C_Q compensation being at 62.5 μF for $e_O = 100$ V, it would be 50 μF at 114 V. This change takes place at $t = 2.4$ s. This and other the performances (like – tracking during $t \leq 1$ s, ramping up during $t \geq 1$ s with transients due to C_Q switching at $t = 2.4$ s) of this study may be observed in the results presented in Figures 5.68 and 5.69. It is evident that under this condition the performance is quite satisfactory. The system tracks the load changes accurately, drawing only the necessary fundamental current from the supply mains.

5.9.7 General Note:

The undesirable component of the source current is constituted by the harmonic (i_{S_h}) and the fundamental reactive component of current. It may be noted that, if there were complete compensation from the fundamental reactive power with appropriate provision of C_Q, i_{S_h} is almost independent of the load. Thus the capacity/rating of the PAF is fixed and is fully utilized under all load conditions.

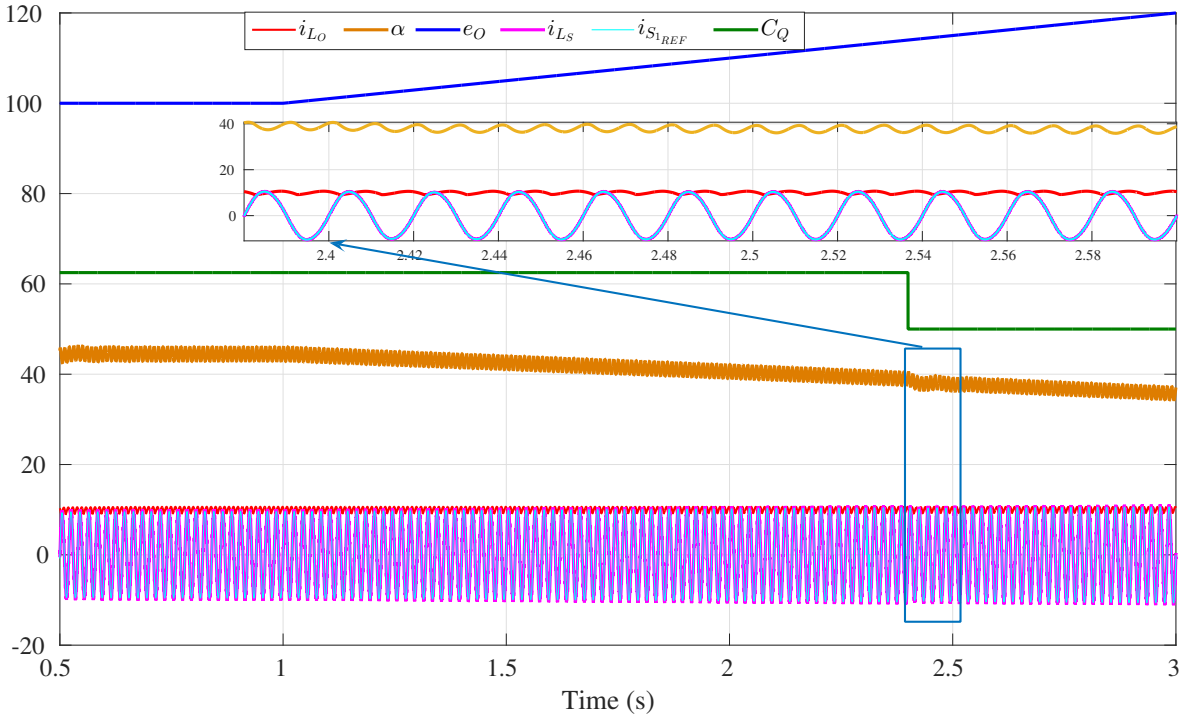

Figure 5.68: Response during Continuous load change ($i_{S_{1REF}}$, i_{L_O}, i_{L_S} in A; e_O in V; α in (°) – degrees; C_Q in μF)

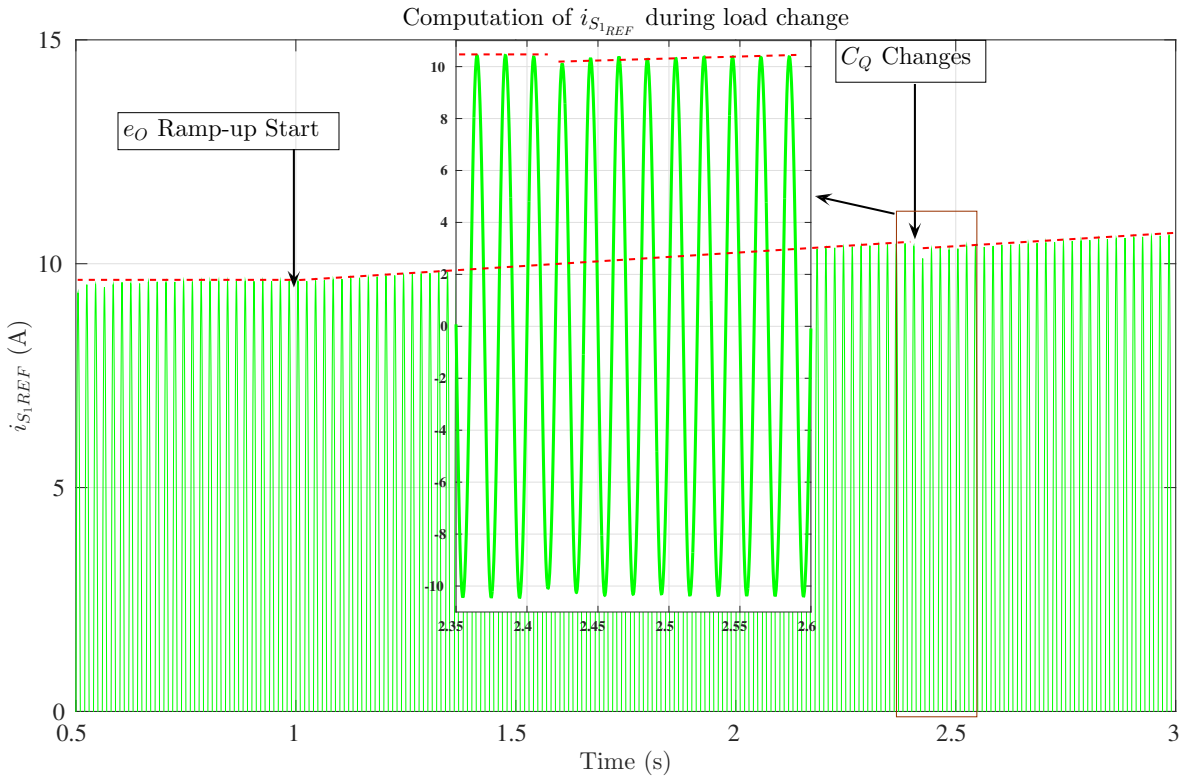

Figure 5.69: Computation of $i_{S_{1REF}}$ during Continuous load change

Table 5.4: Results of Simulation Studies Guiding Conclusion

	Case-1	Case-2	Case-3	Case-4	Case-5	Case-6	Case-7	Case-8	Case-9	Case-10	Case-11	Case-12	Case-13	Case-14	Case-15	Case-16
Power Tabulation																
Pin_Actual	508.6	1453.7	509.0	649.1	693.9	661.1	703.0	1531.0	1128.6	2062.2	1964.4	1962.7	1989.4	1129.8	1088.8	1915.5
Pout	479.8	1421.0	480.7	489.4	491.4	487.4	491.4	1438.5	1040.2	1931.7	1880.2	1790.0	1790.4	1041.8	1041.6	1785.1
P_PAF_LOSS	9.5	6.3	9.7	0.1	0.1	1.7	0.5	0.4	0.6	0.8	0.3	0.6	0.8	0.6	0.2	0.2
P_PAF_1	394.3	190.4	534.0	0.1	0.1	512.3	5.8	10.6	18.2	-15.7	-9.1	12.4	7.7	106.7	-0.8	-0.8
PSC	8.9	9.6	8.9	1.9	3.9	2.4	3.9	4.7	8.3	25.5	22.1	22.6	23.7	8.4	6.8	20.5
P_PAF_2	5.3	5.2	5.3	0.1	0.1	5.2	5.1	5.2	5.1	5.3	0.1	0.1	0.1	5.1	5.1	0.1
P_TF3	0.1	0.1	0.1	6.5	28.9	6.0	32.1	46.0	39.6	37.4	33.4	39.2	39.1	39.3	8.5	9.2
P_TF5	0.1	0.1	0.1	2.7	6.0	2.9	6.0	7.8	7.3	6.8	6.3	7.4	7.2	7.3	0.6	0.7
P_TF7	0.1	0.1	0.1	1.3	2.1	2.5	2.1	4.2	2.9	2.5	2.0	3.1	2.7	2.9	1.5	1.6
P_CQ	0.1	0.1	0.1	151.6	168.0	157.1	168.5	1.6	1.6	30.8	0.1	76.8	102.5	1.6	1.6	75.3
P_COM_F	22.9	21.9	22.9	22.9	23.0	22.9	22.9	22.9	23.0	21.3	20.2	22.9	22.9	23.0	23	22.8
P_LOSS_Total	46.8	43.1	47.0	187.0	232.0	200.8	241.1	93.0	88.5	130.5	84.5	172.7	199.1	88.2	47.3	130.3
Efficiency	**0.94**	**0.98**	**0.94**	**0.75**	**0.71**	**0.74**	**0.70**	**0.94**	**0.92**	**0.94**	**0.96**	**0.91**	**0.90**	**0.92**	**0.96**	**0.93**
Distortion Factors																
THD_vPL	11.16	10.51	11.19	3.26	0.89	4.16	4.82	8.22	2.23	2.57	2.78	2.35	2.39	2.20	2.3941	2.3431
THD_iLS	80.08	36.02	73.92	108.07	60.17	58.02	9.57	4.67	8.83	7.84	6.89	6.30	5.94	4.13	8.1755	5.7741
THD_iRESI	40.60	42.32	40.59	108.09	60.18	133.55	57.99	27.96	43.42	22.94	21.50	25.62	23.82	43.18	18.7465	13.1826
THD_iLR	40.60	42.33	40.60	40.87	40.97	40.88	40.97	43.19	41.93	40.91	40.10	45.12	44.94	41.93	41.9036	44.9617
TDD_iLS_10 A	31.47	26.16	34.58	32.18	19.16	29.92	2.96	3.16	4.44	7.09	5.95	5.50	5.24	2.24	3.899	4.8781
TDD_iLS_25 A	12.59	10.46	13.83	12.87	7.67	11.97	1.19	1.27	1.78	2.84	2.38	2.20	2.09	0.90	1.5596	1.9512
RMS Values of Currents																
IL1	9.76	7.91	9.94	0.00	0.00	4.08	2.15	2.12	2.46	2.79	1.83	2.43	2.80	2.46	1.4076	1.3633
IL2	0.02	0.02	0.02	0.00	0.00	0.02	0.02	0.02	0.02	0.02	0.00	0.00	0.00	0.02	0.0226	0.0002
IL3	0.00	0.00	0.00	1.07	2.25	1.03	2.38	2.85	2.64	2.57	2.42	2.63	2.62	2.63	2.7811	2.8917
IL4	1.69	0.19	1.69	0.07	3.72	0.07	3.71	7.01	5.46	9.55	8.88	8.99	9.21	5.47	4.9398	8.5533
IL5	0.00	0.00	0.00	1.13	1.71	1.21	1.73	1.98	1.91	1.85	1.78	1.93	1.90	1.91	1.9012	1.9516
IL6	1.68	0.19	1.68	0.06	3.56	0.07	3.52	0.00	5.18	9.06	8.42	8.53	8.73	5.19	4.6867	8.1146
IL7	0.00	0.00	0.00	1.13	1.46	1.59	1.46	2.05	1.71	1.59	1.40	1.77	1.66	1.71	1.6986	1.7596
ILV	1.68	0.19	1.68	0.06	3.56	0.07	3.52	0.00	5.18	9.06	8.42	8.53	8.73	5.19	4.6867	8.1146
ILR	10.00	9.77	10.00	10.01	10.02	10.01	10.00	10.01	10.01	9.64	9.39	10.00	10.00	10.02	10.0121	9.9709
ICQ	0.00	0.00	0.00	5.51	5.80	5.61	5.81	5.69	5.71	2.46	0.00	3.92	4.53	5.70	5.6141	3.8815

A summary of the results obtained for some of the cases considered is presented in Figure 5.70. It can be seen that the harmonic current levels are within the standard

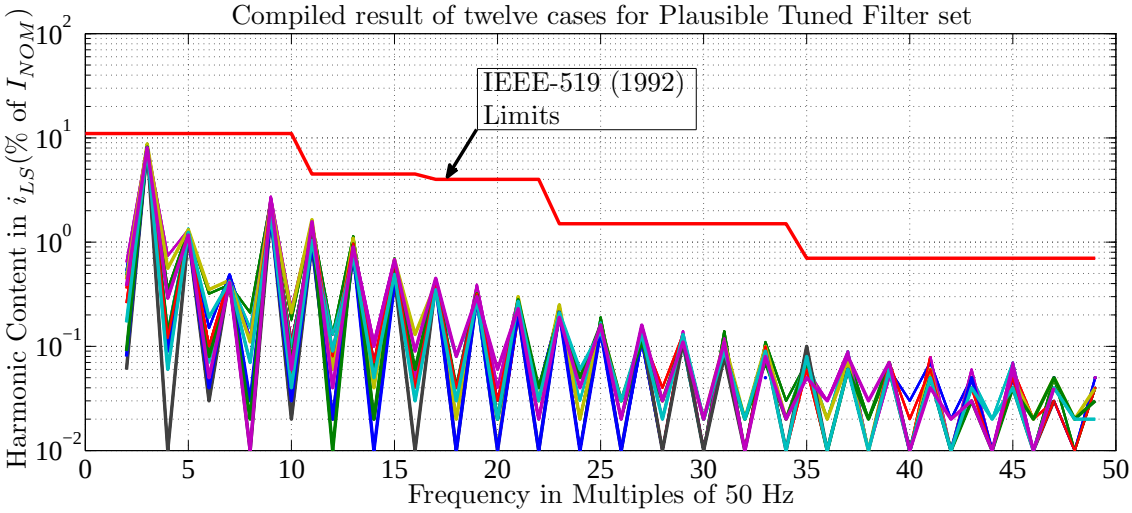

Figure 5.70: Harmonic content in i_{LS} for all the cases in comparison with the IEEE 519:1992

IEEE Std. 519:1992 for all harmonics in the range from 3^{rd} to 50^{th} harmonics. The effect of switching schemes for the cases with high load $E_O = 110$ V and series compensator bypassed is presented in Figure 5.71. It can be observed that the harmonic

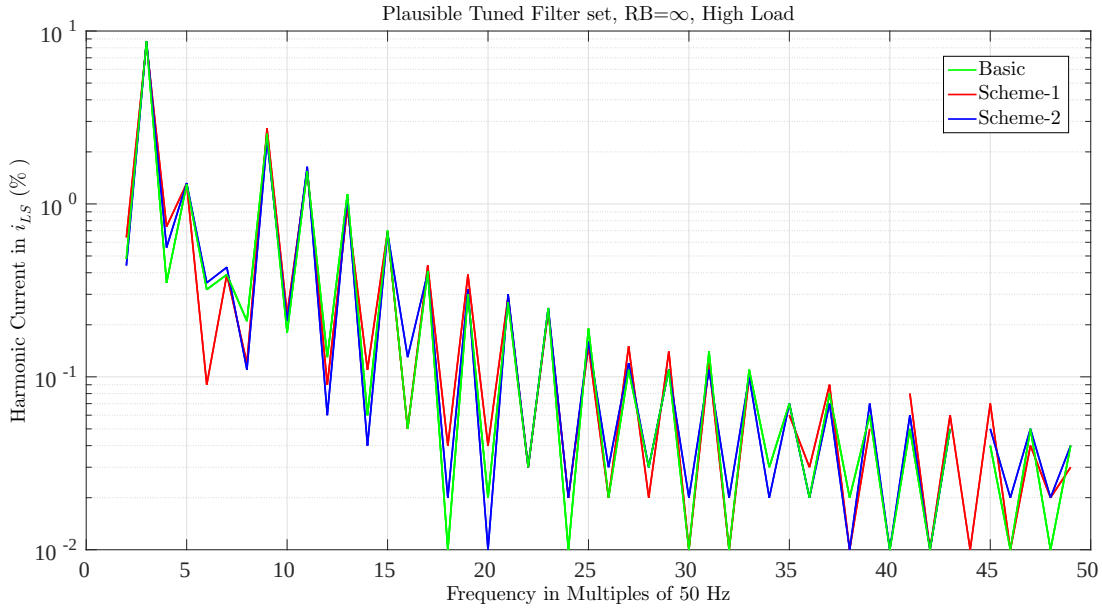

Figure 5.71: Harmonic content in i_{LS} for the Case stated with different switching schemes

content is not affected much by the different switching schemes and hence the scheme

which is more advantageous in other aspects can be chosen for implementation.

5.10 Simulation studies with an experimental parameter set

Several cases are considered and data obtained for twelve cases are compiled and the results are plotted. The simulation studies are repeated with a set of parameter values for the tuned passive filters matching with those of experimental setup. The results are presented in the following.

Case-15 (A.4, A.1.2)

The relevant current and voltage waveforms are shown in Figure 5.72. The spectra

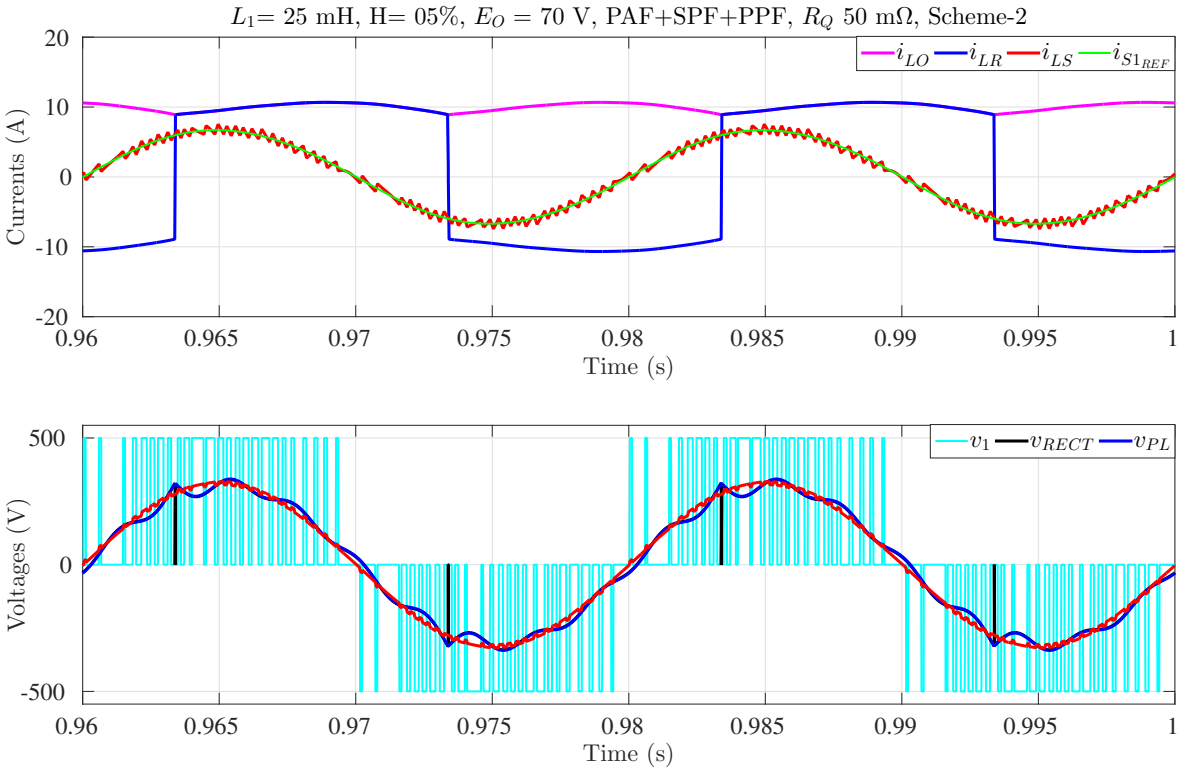

Figure 5.72: Time domain waveforms for Case-15

associated with the currents is presented in Figure 5.73.

Case-16 (A.4, A.1.2)

The relevant current and voltage waveforms are shown in Figure 5.74. The spectra of i_{L_R} shown in the Figures 5.73 and 5.75 in comparison with those of Figures 5.52 and 5.61 respectively reveal the effect of a narrow-band tuned-filter characteristics on the TDD.

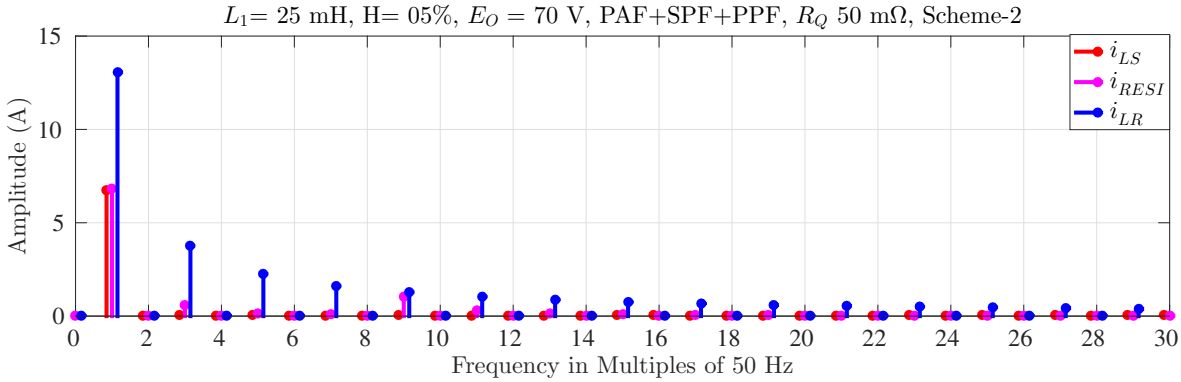

Figure 5.73: Spectra of relevant waveforms for Case-15

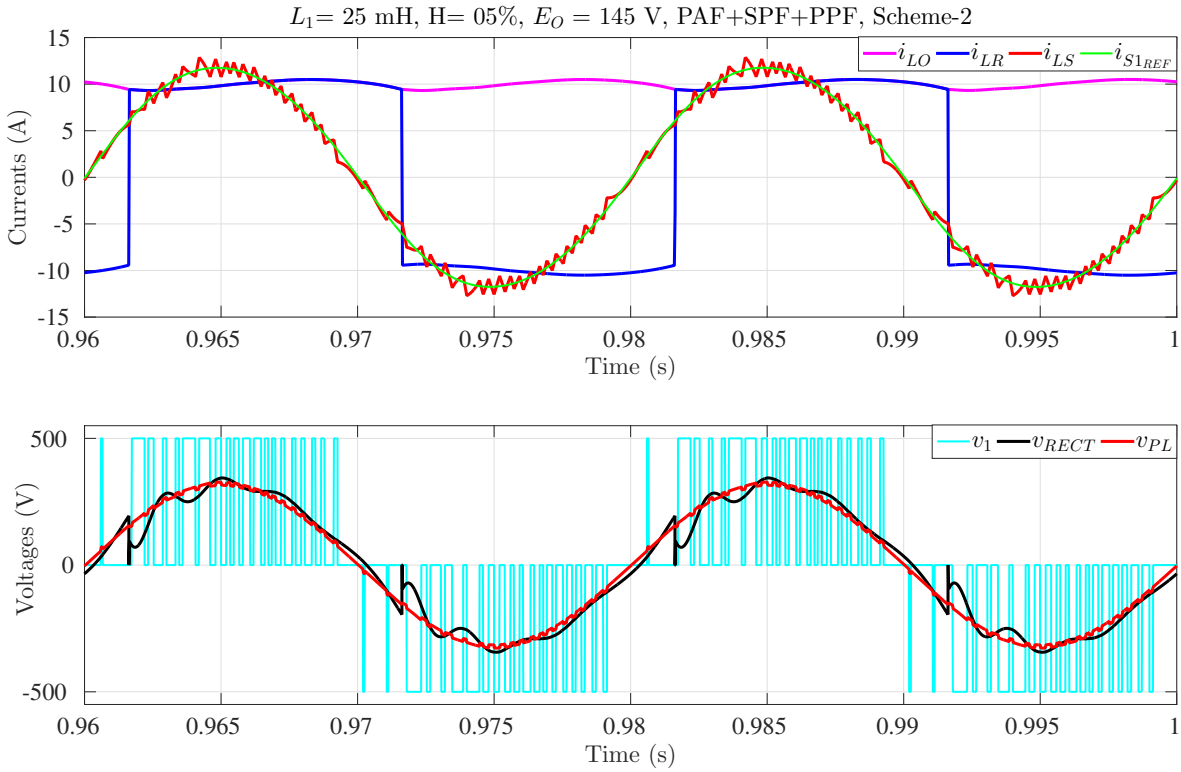

Figure 5.74: Time domain waveforms for Case-16

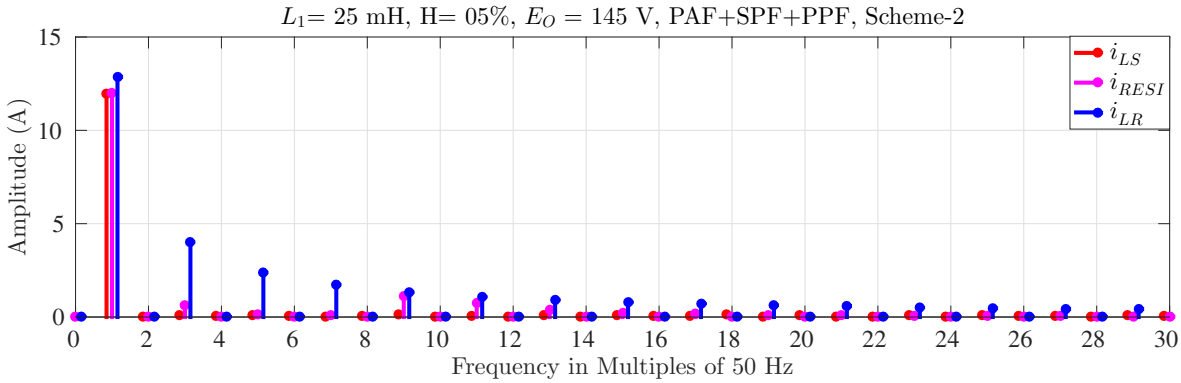

Figure 5.75: Spectra of relevant waveforms for Case-16

5.10.1 Transient performance comparison amongst switching schemes

The transient performance of different switching schemes is obtained for same system parameters and changing the switching schemes. In Figure 5.76, the variation of the load current i_{LO} and supply current i_{LS} for a sudden command change of $E_O = 35$ V to 75 V at $t = 0.5$ s is presented. It takes about 100 ms to settle to the final cyclostationary steady-state. In Figure 5.77 is presented the plots of the peaks of the

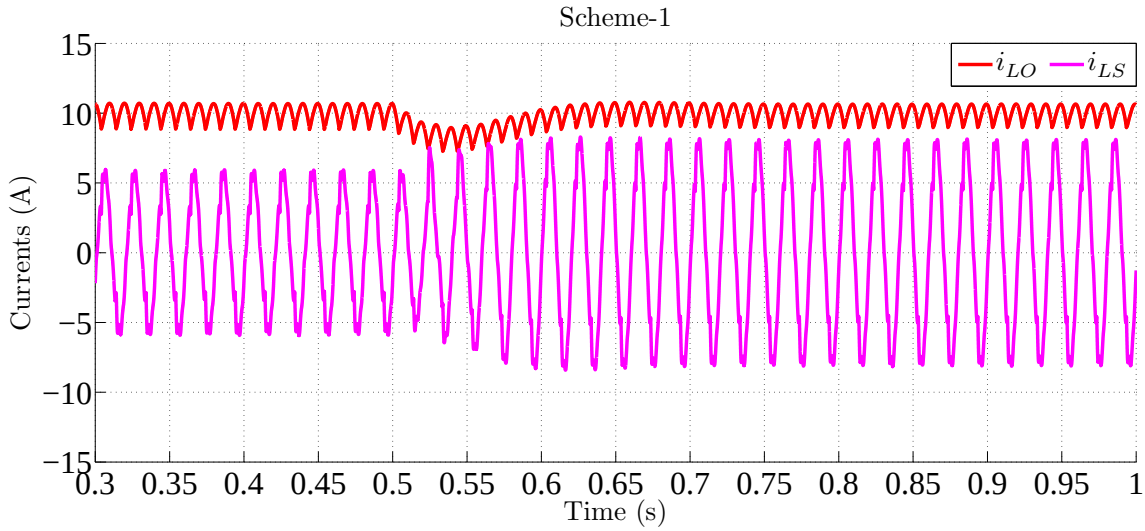

Figure 5.76: Transient performance of switching scheme-1

i_{LO} and i_{LS}, depicting the transient response for the three switching schemes. It can be observed that there is not any difference in the performances in each case. Hence the only criterion for selection of the switching scheme can be the number of switchings per cycle. And in this regard the Scheme-2 (scores lowest (GOOD)), the Scheme-1, and the Basic scheme (scores highest) fall in the decreasing order of preference.

5.11 Conclusions

It is attempted to obtain a topology suitable for improving the Power Quality for a Current-Source type of Nonlinear Load. The options reported in the literature include either one or a combination from the set comprising of – a Commutating Inductor at the input to the rectifier, Parallel Passive Filter – tuned and reactive power compensator, Parallel Active Filter, Series Active Filter, or a Series Passive Filter. However for the case of CSNL a combination that meets the requirements of limiting the distortion of

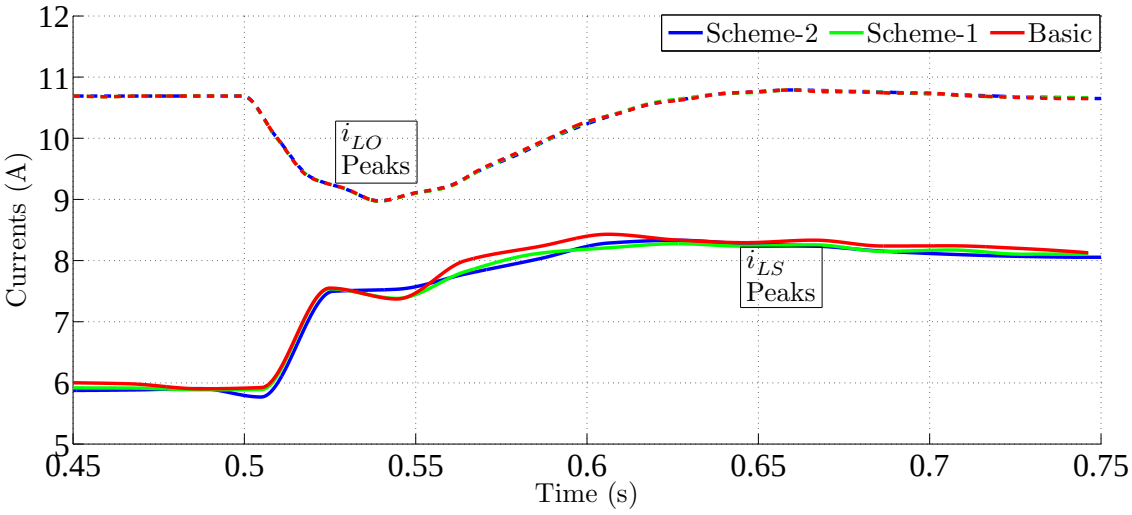

Figure 5.77: Comparison of Transient performance of switching schemes

the line current and the voltage at the PCC and that at the input to the rectifier is not reported.

In this study some favorable options guided by theoretical intuition are considered for exploration on the general topology. The guiding principles are as given below:

- The use of only Commutating Inductor will reduce the $\left(\frac{di}{dt}\right)$ and thus gives an impression that the input current distortion can be reduced. It has limited success and the negative side of the solution is that it increases the line notching of the voltage at the rectifier input and hence results in loss of (volt·second) available at the output. It also increases the distortion of voltage at the input to the rectifier which may cause difficulties in the control of the rectifier.

- The use of only SPF will result in the harmonic voltage drops across the series element given that the load is a CSNL, and thus has similar effects as that stated above.

- A Parallel Passive Filter is necessary to tame/convert the Stiff load current waveform to a smoother waveform which can be further improved.

- Thus a series compensator with a passive element is necessary and must be placed to the left of the PPF, i.e., on the upstream side of the PPF, for the same reason as mentioned earlier. This helps in further improving the source current, as well as the quality of voltage at the input to the rectifier.

- A PAF of a very low capacity placed at the PCC with the utility can be considered to supply the residual harmonic and reactive current.
- The Series Active Filter if considered can further improve the performance of the overall system.

On the basis of these guidelines a detailed study is conducted on the general topology considered. Several cases of parameters for the system and the load are considered. An analysis of the simulation results showed that a combination of a passive series compensator and a passive shunt compensator (in right-shunt fashion) is necessary to shape the source current and, to provide a quality voltage at the PCC and at the input to the rectifier. The series passive compensator may be the leakage inductance of the Series Active Compensator/ Filter as well when such an option is considered. In that case, the shunt compensator must be a right-shunt. The PAF and SAF can be called upon to correct for the residues left-over from the action of the passive compensators. The line commutating inductance of appropriate value is also included which resulted in an optimal improvement in the performance parameters.

The two novel switching techniques making use of v_{PCC} are compared with the basic hysteresis. It is found that there is not much difference in the steady-state power quality parameters nor in the transient performance. The main difference is only in the number of switchings per fundamental cycle and the voltage transitions – being $2V_{DC}$ (for the Basic Scheme), compared to V_{DC} in the two proposed techniques. In terms of the number of switchings per cycle, Scheme-2 scores better with Scheme-1, and Basic Scheme scoring highest switching and thus fall in the decreasing order of preference. Considerations to switching losses and Electro Magnetic Compatibility issues would suggest the use of Scheme-2 over the other schemes.

Chapter 6

Experimental setup and results from Hardware Implementation

6.1 Introduction

The hardware implementation of the scheme involves the design, development, fabrication, and testing of different components of the system. The power circuit (which includes active and passive filters), sensing and signal conditioning system, and the controllers are set up and tested. The passive-filter with tuned and reactive power compensation is implemented and results from various test cases are presented. The cases also involve situations of series compensation under sag or swell. Here only the sinusoidal steady-state cases are considered. A three-legged inverter module is tested for 600 V and switching frequency of up to 30 kHz, with 15 A current. It meets the requirements of the PAF (two legs with three-level switching) and a SAF or DVR (with another leg and the DC-bus midpoint acting as a half-bridge). The results from switching of one of the legs as a chopper is also presented.

6.2 Hardware Components of the Power-Shield

The various components necessary for implementation of the Power-Shield are listed here. Their design and features are explained.

6.2.1 Items designed and developed

Signal sensing Components

- Hall Effect Voltage Sensor cards: The Voltage sensing is done using the LV 25-P voltage sensors of LEM make [LEM(2014)]. This has a primary nominal current of 10 mA and the corresponding secondary current is 25 mA. Hence to sense a voltage in the range of 600 V, a sensing resistance R_S^V of 50 kΩ is used. This has a primary winding resistance of 250 Ω. The output current has to be converted to an appropriate voltage using a Current-to-voltage converter. The 50 kΩ is implemented as a series combination of two 10 kΩ and 15 kΩ each, to minimize the effect of variation of R_S^V with heating.

- Hall Effect Current Sensor cards: The Hall current sensor used is LA 55-P of LEM make [LEM(2014)], which has a nominal current input of 50 A-turn (RMS), with a corresponding secondary current output of 50 mA.

- Current-to-Voltage (C-V) converter: The output of the current and voltage sensors are available in the form of current, and hence it has to be converted into voltages of appropriate range to match with the Digital Signal Controller (DSC) to be interfaced with. In this regard, the inbuilt ADC on the the DSC TMS320F28335 [Texas Instruments(2012)] – a floating point processor, has a unipolar input range of 0-3 V. This requires that the output of the C-V converter has to be in the range of ±1.5 V, which with a DC shift of 1.5 V, will make the signal at the ADC input to be unipolar. This leads to a measuring resistance of R_M^V of 64Ω for the voltage sensors and R_M^I of 20Ω for the current sensors. This gives a gain of G_V= 314.0625 V (input)/V (output) for the voltage channels and G_I= 50 A(input)/V (output) for the current channels. The TMS320F28335 eZDSP starter kit [Texas Instruments(2013)], also has an external ADC interface card, which can take a larger voltage range of ±10 V. Hence another C-V converter card is made by choosing R_M^V= 330 Ω for the voltage sensors and R_M^I= 470 Ω and 220 Ω for the current sensors. This gives the gains of 60.909 V (input)/V (output) for the voltage channels and 2.127 A (input)/V (output) and 4.54 A

(input)/V (output) for the corresponding current channels respectively.

Signal Conditioning and Level Shifting Cards

- Digital level-shifter boards: This card serves as an interface between the Digital Controllers which have a digital signal level of 0 and 3 V and the other circuits like – the gate-drive cards for the IGBTs and the sequencing and protection systems which work at higher voltage level, here it is at ±15 V. Thus the signals which are at ±15 V level from the outside world (to the DSC) are lowered down to 0/3 V, using fast comparators and with appropriate zener protection at the output. Similarly the signals which are at 0/3 V level from the DSC are stepped up to ±15 V level. It is also made sure that an open circuit will force a low at the input to the DSC to prevent a shoot-through fault.

- Analog level-shifter boards with anti-aliasing filter: The voltage and current signals are to be sampled for implementation of the controller. Considering up to the 20^{th} harmonic (i.e. 1000 Hz on 50 Hz fundamental) an anti-aliasing filter of 3 kHz is chosen. A switching frequency of 10 kHz is chosen for Active-Filter implementation. If the inbuilt ADC on the DSC is used the bipolar signals in the range of ±1.5 V, from the C-V converters have to be level shifted to be in the range of 0-3 V. This is achieved by an adder with a reference voltage of +1.5 V, added to each channel. A precise adder unity gain is obtained by matching resistances (with 1% tolerance) making the adder circuit. The output has also a 0-3 V limiter.

Inverter module

A three-legged VSI module is fabricated, consisting of the SKM 75GB123D, 1200 V, 75 A Semikron make [Semikron(2012)] IGBT modules; parallel plate DC bus; EPCOS make [EPCOS(2010)] 3300 μF, 450 V, DC capacitors' bank; the high frequency damping circuit comprising of 50 kΩ, 10 W resistors with 1 μF, 1000 V DC Alcon [Alcon Electronics Pvt. Ltd.(2010)] make capacitors; heat sink and the cool-

ing fan. The DC bus is made up of parallel brass-plates separated by NOMEX® [NOMEX(2010)] insulation.

Other associated and auxiliary components

- Power supply: The implementation requires regulated power supplies (±3.3 V, ±5 V ±15V) for analog and digital circuits. It is decided to use separate power supply for analog and digital circuits. In all cases appropriate linear regulators are used. These linear regulators are supplied from unregulated voltages (±6 V, ±9 V, and ±20V.) from diode rectifiers fed from multiple secondaries of a power supply transformer. Common DC bus rail is provided for tapping the appropriate source.

- Test-zig for testing IGBTs/ MOSFETs and their Gate drives: A Test-zig for testing IGBTs/ MOSFETs and the Gate drives is developed and fabricated. It has features of isolated DC power supply with two steps of voltage; loading inductor – 10 A with 0-1-2-3-4-5 mH; DC bus discharging arrangement; a power supply for the gate drive card; and a micro-controller based programmable (Frequency and duty ratio) dual and complementary Pulse-width-modulated waveform generation unit. This unit also has facility for power sockets required for Oscilloscopes and other equipment. It serves a very good purpose during the development phase of such hardware.

6.2.2 Other Systems and components

- Gate drive cards: Each gate drive card has features of two 0/15 gate inputs; a power supply +15 V input. It gives out two isolated gate drives ±15 V and a fault signal of +15 V, in the event of a V_{CE} saturation due to a shoot-through fault. The isolation is provided by opto-couplers and a fly-back converter based isolated power supply regulated by a 15 V linear regulator.

- Passive filter components

Inductors: The specifications for the iron cored inductors with linear characteristics required for Line Coupling, Tuned Filter, and load are obtained and are purchased. Of them are the 0-125-250-375-500 mH, 10 A and the 0-1-2-3-4-5 mH, 10 A. The tuning of the harmonic filters is achieved by choosing appropriate terminals from the required set of inductors.

Capacitors: Electrolytic capacitors required for the DC bus is EPCOS 3300 μF, 600 V; and Metalized polypropelene capacitors are used for AC circuits. Of them are 12.5μF, 400 V; 36μF, 400 V; 50 μF,400 V; each with an RMS current rating of 10 A. They are of EPCOS and Keltron make [Keltron(2010)].

- Nonlinear load: A single-phase current-source type of nonlinear load in this case is a single-phase controlled rectifier feeding a large inductive load with back EMF. The rectifier load consists of 500 mH, 10 A inductor and a separately excited DC motor feeding a three-phase alternator with lamp-load. The required back EMF (as dictated by the firing angle setting on the rectifier for different loads) and the current (10 A fixed) is obtained by either adjusting the load at the output of alternator or the field current of the DC motor.

The circuit diagrams and photographs of the components discussed above are given in the Appendix - B.

6.3 Results of experiment with the Passive-Filter

The experimental setup for implementation of the scheme are shown in Figures C.1 to C.3. All quantities referred in this section have been indicated in the figure. Various cases for testing can be obtained for different combinations of the switches marked in the corresponding circuit diagram. The tuned filters have the following parameters: From (5.30) $C_h \cong 12.5\mu$F $\forall$h. Then the required inductance L_h is obtained from (5.31) for different tuned filters and the results are tabulated in Table 6.1.

6.3.1 Experiments with direct-on-line performance

The load-filter system is connected to the utility system directly without the series compensation arrangement or the autotransformer. This is intended at studying the

Table 6.1: Tuned filter parameters

Order (h)	Inductance (mH) (L_h)	Capacitance (μF) (C_h)	Resistance (Ω) (R_h)	Tuning frequency (Hz) (f_h)	Q-factor (Q_F)
3	90.50	12.5	1.0964	149.64	012.35
5	32.85	12.5	0.1789	248.37	286.00
7	16.92	12.5	0.5179	346.07	071.04

performance when the system is directly connected to the utility as is the case in actual implementation. In such a case the effect of source impedance can clearly be seen on the performance of the passive tuned filters. The experiment is conducted for various values of firing angle and with and without the passive filter insertion. The results are tabulated in Table 6.2. Some typical waveforms corresponding to the cases of 30°and 72°are shown from Figures 6.1 through 6.3. The waveforms are captured on the 4-channel TDS 2014C, 200MHz, 2GS/s, Digital Storage Oscilloscope.

Table 6.2: $V_{PR} = V_{PL} = V_s$, L_R=1.4066 μH, I_0 = 10 A, R_B=0

α	Filter	V_S (V)	I_S (A)	V_{RECT} (V)	V_0 (V)	P_0 (W)
30°	OFF	228.3	10.0	224.2	166.5	1665
	ON	228.1	09.0	223.3	166.6	1666
45°	OFF	224.9	09.9	220.9	129.0	1290
	ON	225.9	07.5	221.4	130.8	1308
60°	OFF	226.0	10.0	220.0	086.5	0865
	ON	227.5	06.2	223.1	089.4	0894
72°	OFF	225.2	09.9	222.1	051.5	0515
	ON	229.0	04.9	225.0	054.0	0540

The results for this case are summarized as follows: There is a reduction in the RMS value of the source current; the extent of reduction is more when displacement factor is small or the the firing angle is large. The source current THD will not improve, as the decrease in the harmonic current is small compared to the decrease in the fundamental current. The load on the parallel active filter is considerably reduced and hence it can be switched at a higher frequency to cover more number of harmonics. The waveforms

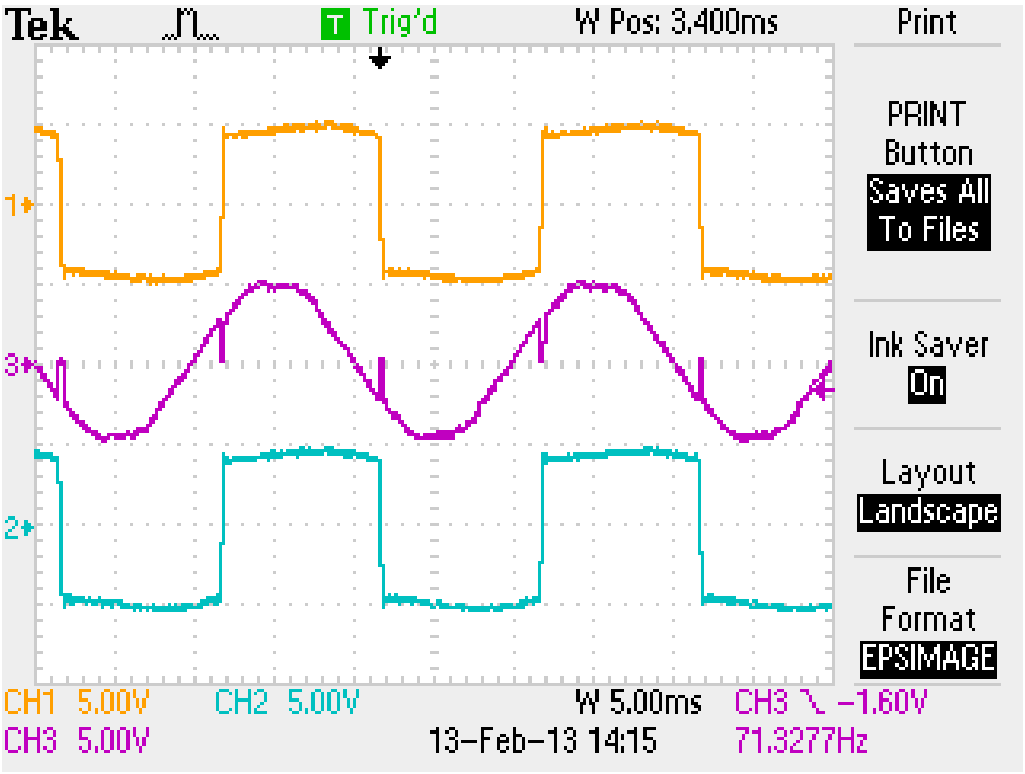

Figure 6.1: α=30°, without filter; Scale: Ch1 (Source current, i_S) and Ch2 (Load current, i_O) is 2.127 A/V and Ch3 (Input Voltage, v_{RECT}) is 60.909 V/V

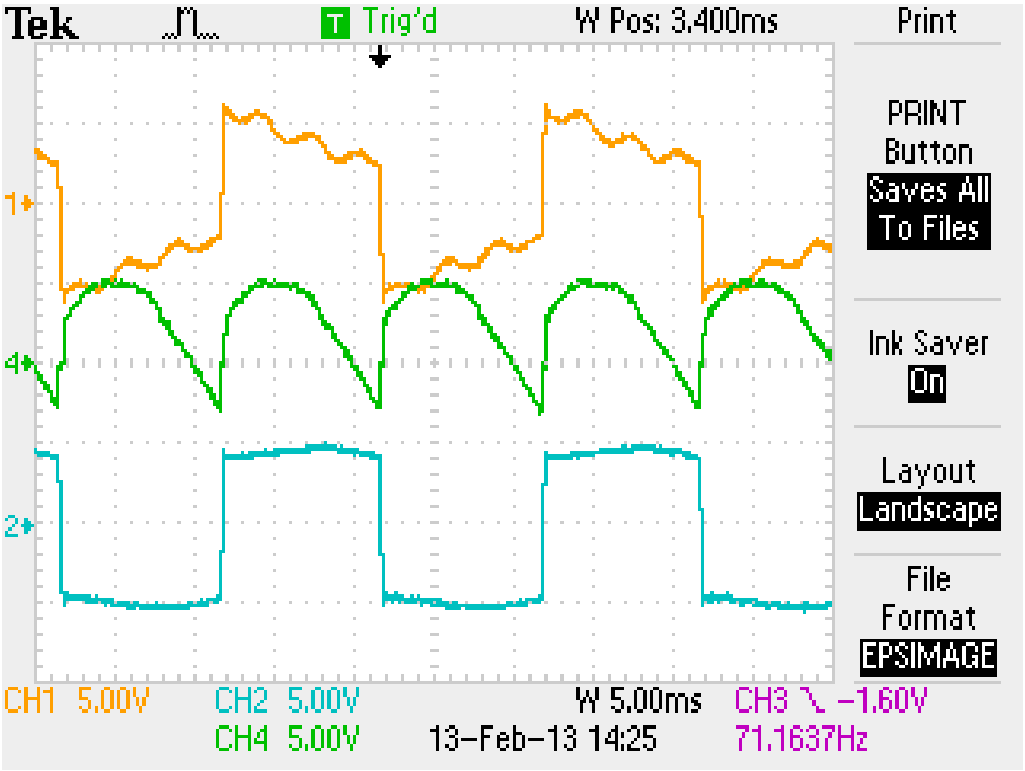

Figure 6.2: α=30°, with only tuned filter; Scale: Ch1 (Source current, i_S) and Ch2 (Load current, i_O) is 2.127 A/V and Ch4 (Output Voltage, v_O) is 60.909 V/V

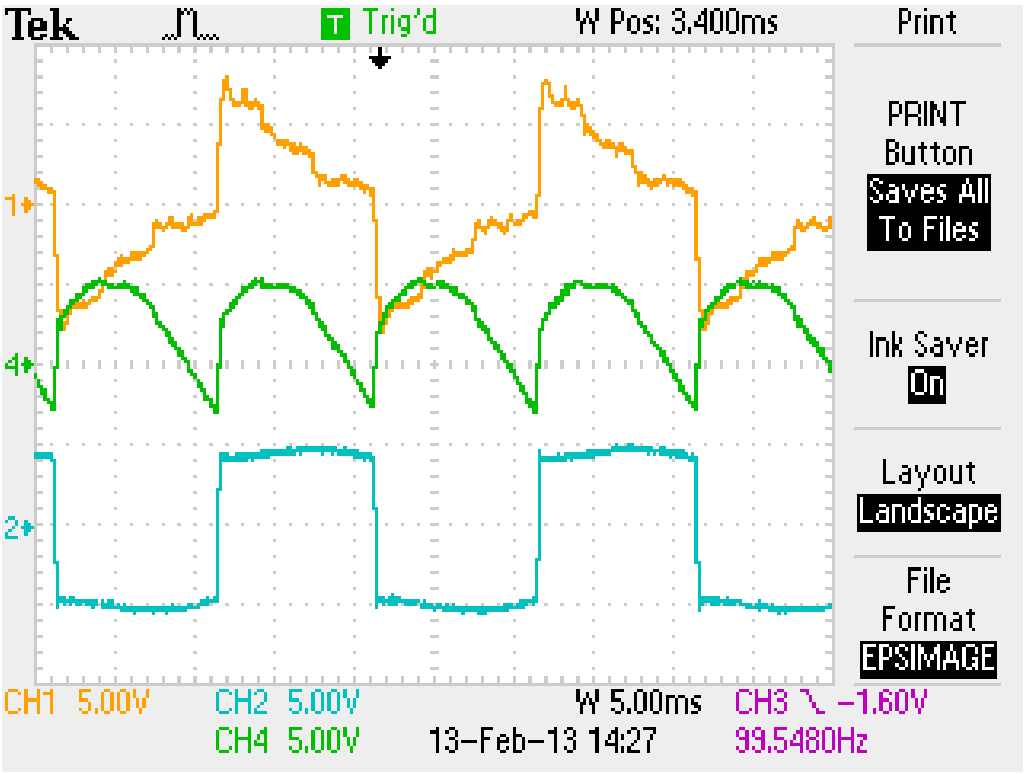

Figure 6.3: α=30°, with tuned filter and reactive power compensator; Scale: Ch1 (Source current, i_S) and Ch2 (Load current, i_O) is 2.127 A/V and Ch4 (Output Voltage, v_O) is 60.909 V/V

recorded are further analyzed and the fundamental current is extracted and plotted in time synchronization with the source voltage. Some waveforms for the case of 72° is shown in Figures 6.4 and 6.5.

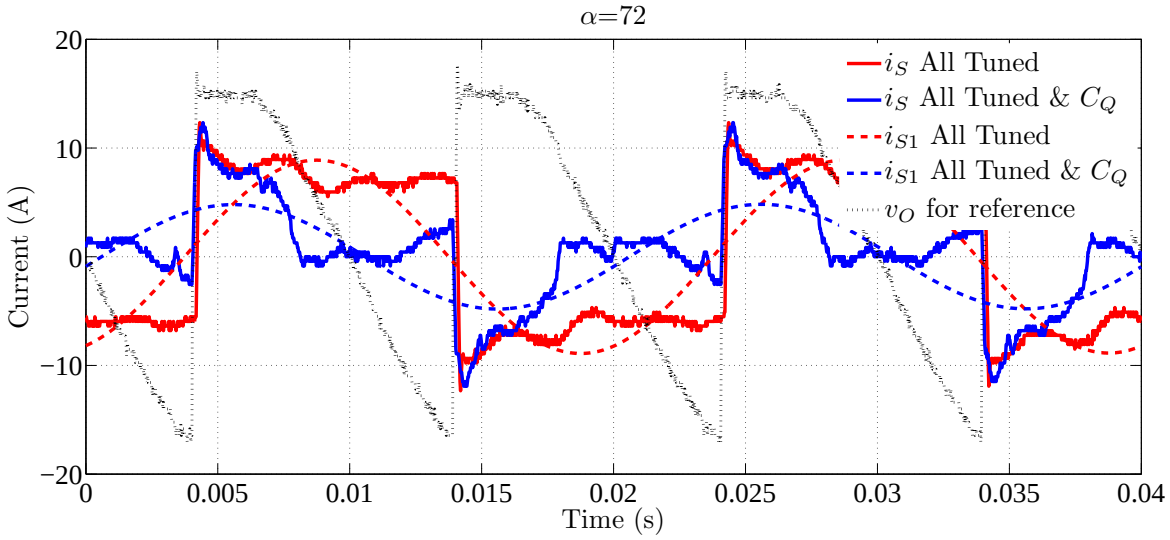

Figure 6.4: Comparison of Source Current with and without filters: Time domain analysis (post-processed).

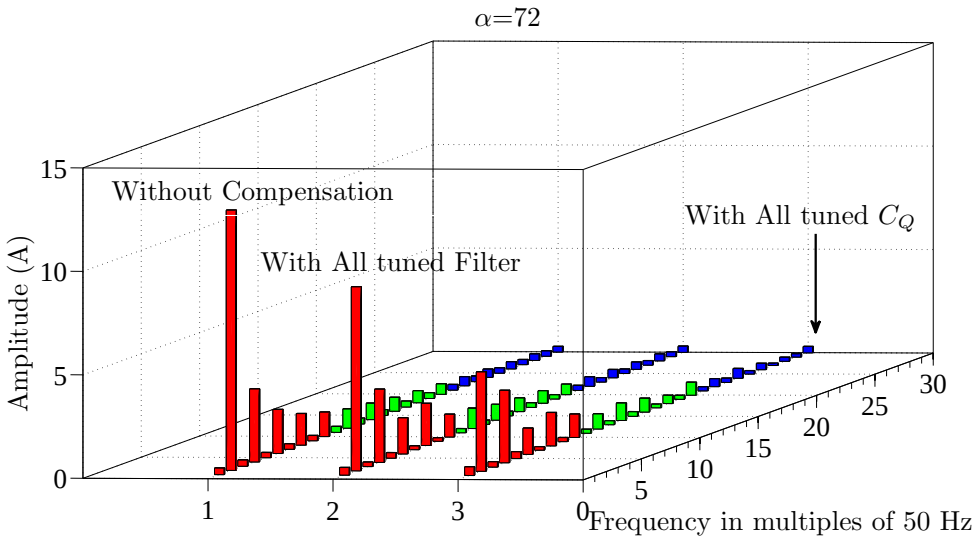

Figure 6.5: Comparison of Source Current with and without filters: Frequency domain analysis (post-processed).

The drastic reduction in the RMS value of the source current is visible in the Figure 6.4 and 6.5 and the source current i_{S_1} is lagging the source voltage only slightly. This justifies the use of reactive power compensator. However the passive tuned filters are not very much effective in absorbing the harmonics.

6.3.2 Case: α=30°, with series transformer, and $V_C = 0$

This experiment is concerned with studying the effect of the series transformer on the commutation overlap and on the additional voltage compensation necessary to account for the series drop. This is due to the leakage inductance of the series injection transformer. The inclusion of the series transformer results in a drop of voltage available at the rectifier input. This also increases the commutation overlap. The results presented here correspond to the first row of Table 6.3. Figures 6.6 through 6.8 represent the results for this case. The RMS voltage (V_{PR}) drops from 230 V to 216 V (without filter) or 220 V (with filter) when the series transformer is introduced. The series compensation has to consider this drop along with the sag/ swell at the supply input. The voltage spikes generated on the load side of the series transformer can be noted on v_{CL} in Figure 6.7 and 6.8.

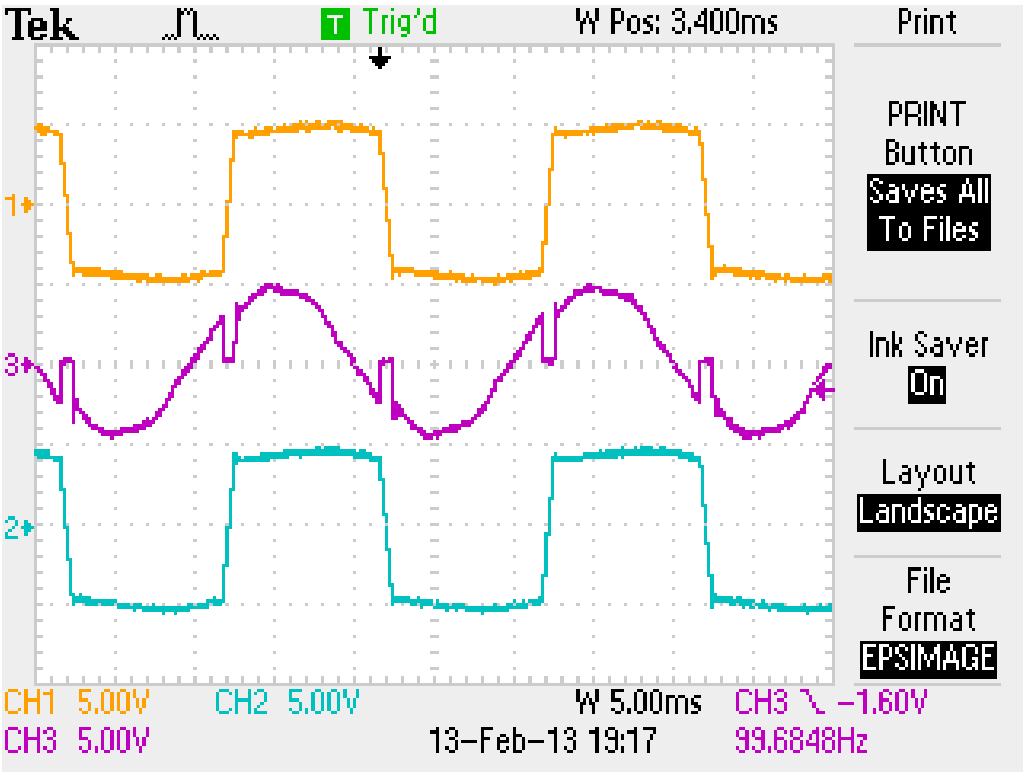

Figure 6.6: α=30°, Filters OFF; Scale: Ch1 (i_S) and Ch2 (i_{RECT}) is 2.127 A/V and Ch3 (v_{RECT}) is 60.909 V/V

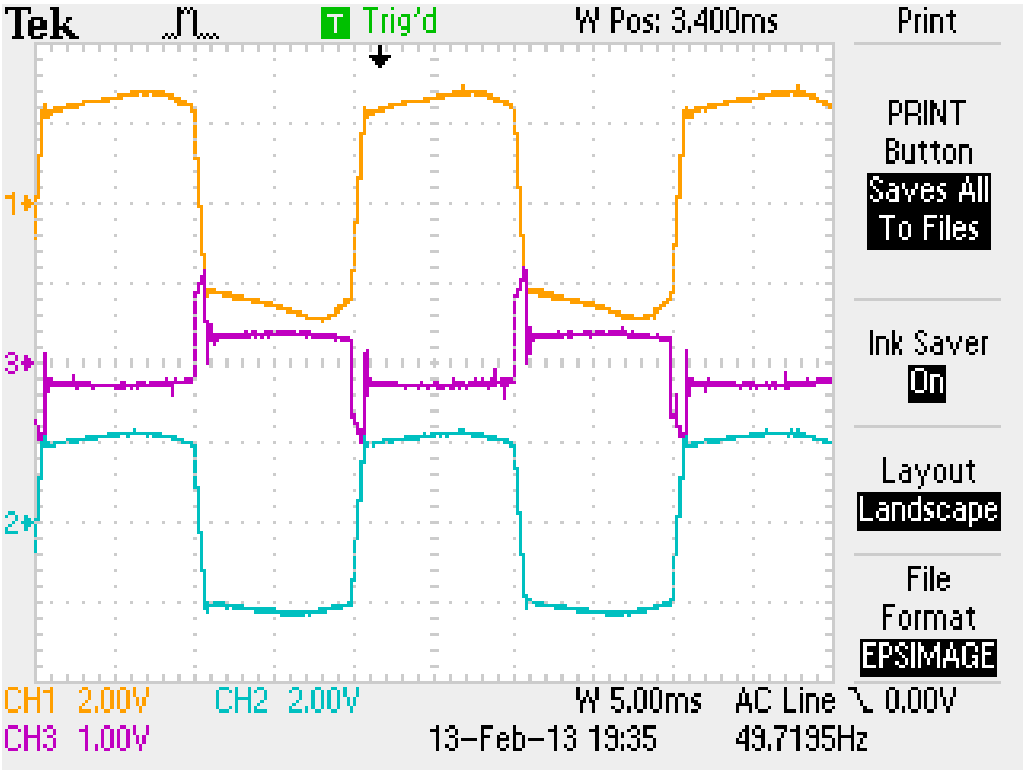

Figure 6.7: α=30°, Filters OFF; Scale: Ch1 (i_{ST}) and Ch2 (i_{CC}) is 4.54 A/V and Ch3 (v_{CL}) is 60.909 V/V

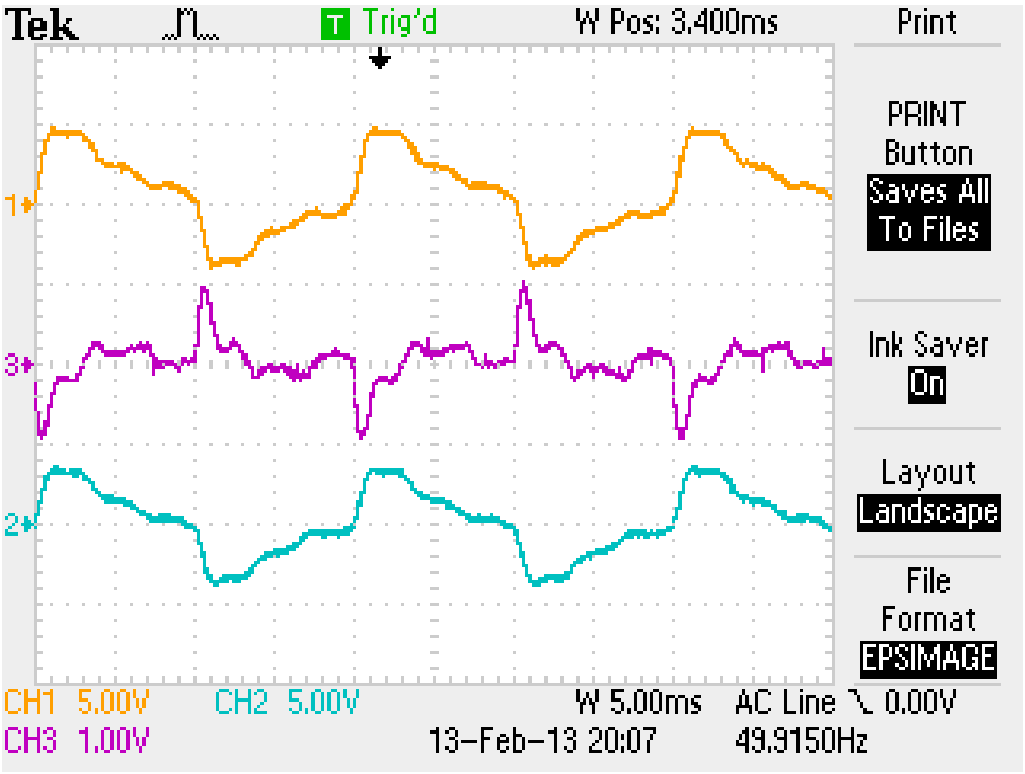

Figure 6.8: α=30°, Filters ON; Scale: Ch1 (i_{ST}) and Ch2 (i_{CC}) is 4.54 A/V and Ch3 (v_{CL}) is 60.909 V/V

6.3.3 Experiments with series compensation: Large commutating Inductance = 1.406 mH

In this case the source voltage is varied for few cases of load firing angle. The series compensator is adjusted to keep the voltage V_{PR} constant at 230 V. The voltage V_{CC} required for compensation for these cases are recorded. Various readings are tabulated in Table 6.3. The reduction in the RMS source current for all the cases is evident from the table. The extent of voltage compensation V_{CC} required in each case and the voltage V_{CL} gives an idea about the series drop because of the transformer leakage inductance. Typical waveforms for the case α=45°and V_{PL}=200 V (Sag) are shown in Figures 6.9 through 6.12. Off-line analysis of the waveforms is carried out and the fundamental source current is plotted along with other waveforms. It can be seen that i_{S_1} with passive filter is almost in-phase with the supply voltage. The waveforms are further analyzed and the results are plotted in Figures 6.13 and 6.14. It can be seen that even with the presence of series transformer the tuned passive filters are not very effective in absorbing the harmonic current.

Table 6.3: Series Compensation: V_{PL} varied; V_{PR}=230 V (maintained by series compensation); L_R=1.4066 mH, $I_0 = 10$ A, R_B=∞

α	Filter	V_{PL} (V)	I_S (A)	I_{ST} (A)	I_C (A)	V_{CC} (V)	V_{CL} (V)	V_{PR} (V)	V_{RECT} (V)	V_0 (V)	P_0 (W)
30°	OFF	230.8	9.7	11.6	9.8	0	23.8	216	212.6	145.7	1457
	ON	230	9.2	10.65	9.33	0	21.23	219.6	217	163	1630
45°(Sag)	OFF	200	9.6	12.3	9.95	45.4	41.5	230	228	116	1160
	ON	200	7.4	9.5	7.8	41.4	33.8	230	226	131.3	1313
60°(Swell)	OFF	260	9.6	11	9.8	23	42.5	230	228.1	88	880
	ON	260	7.3	7.8	7.4	19.6	33	230	226.8	118	1180
72°(Sag)	OFF	200	9.7	11.7	9.95	41.5	38.4	230	230	43.5	435
	ON	200	4	4.5	4.3	34.2	30.8	230	227.6	46	460
30°	**ON**	**230**	**9.4**	**11.5**	**9.4**	**11.48**	**29.8**	**230**	**227.8**	**170.2**	**1702**

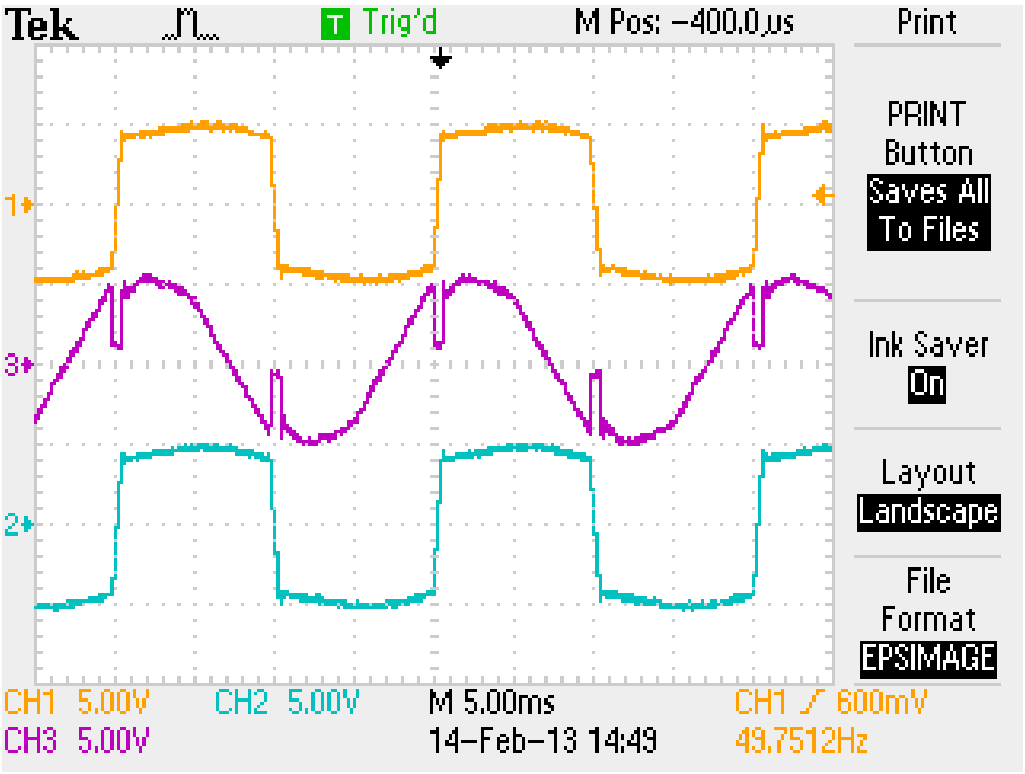

Figure 6.9: α=45°, Filters OFF; Scale: Ch1 (i_S) and Ch2 (i_{RECT}) is 2.127 A/V and Ch3 (v_{RECT}) is 60.909 V/V

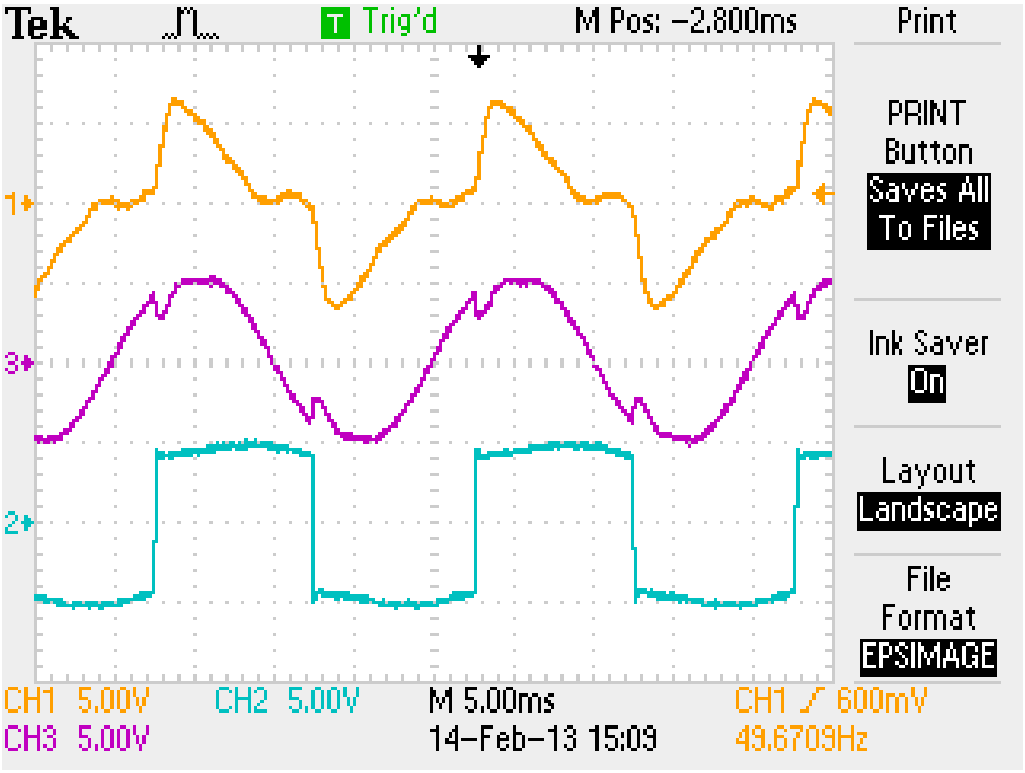

Figure 6.10: α=45°, Filters ON; Scale: Ch1 (i_S) and Ch2 (i_{RECT}) is 2.127 A/V and Ch3 (v_{PR}) is 60.909 V/V

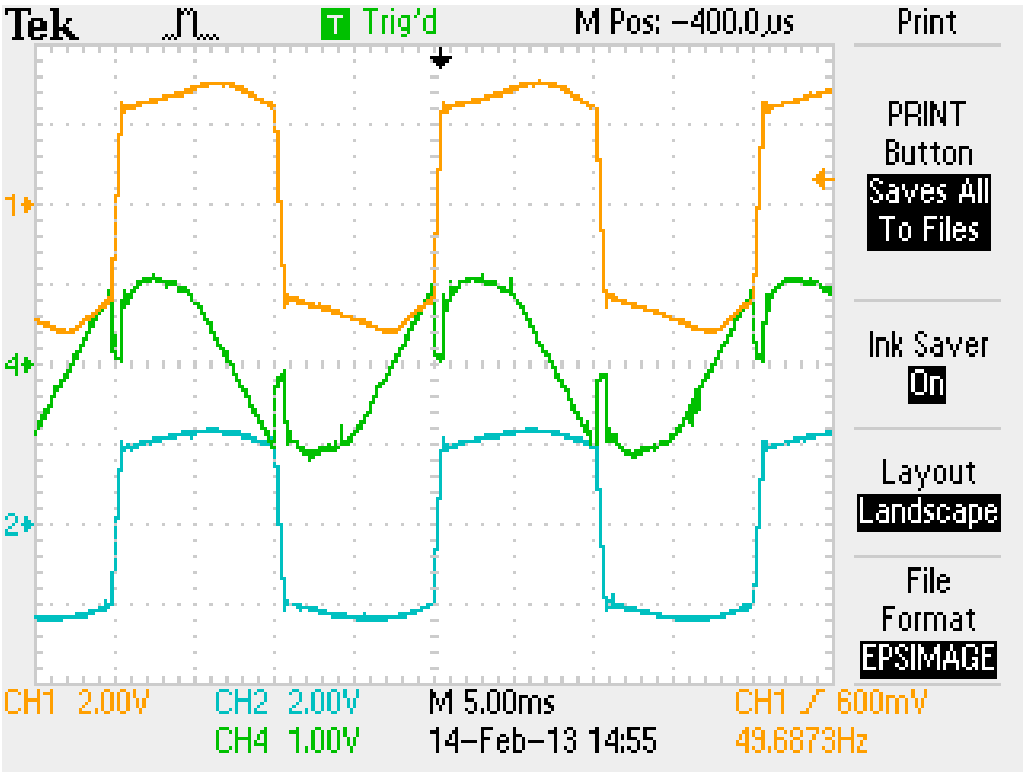

Figure 6.11: α=45°, Filters OFF; Scale: Ch1 (i_{ST}) and Ch2 (i_{CL}) is 4.54 A/V and Ch4 (v_{CC}) is 60.909 V/V

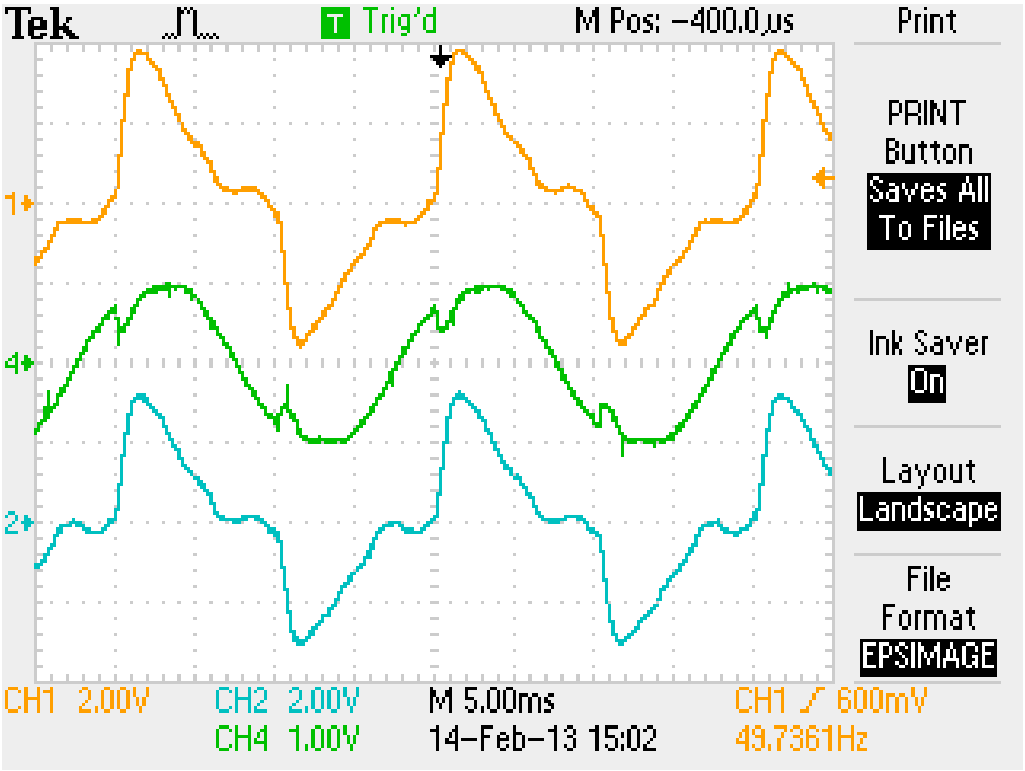

Figure 6.12: α=45°, Filters ON; Scale: Ch1 (i_{ST}) and Ch2 (i_{CL}) is 4.54 A/V and Ch4 (v_{CC}) is 60.909 V/V

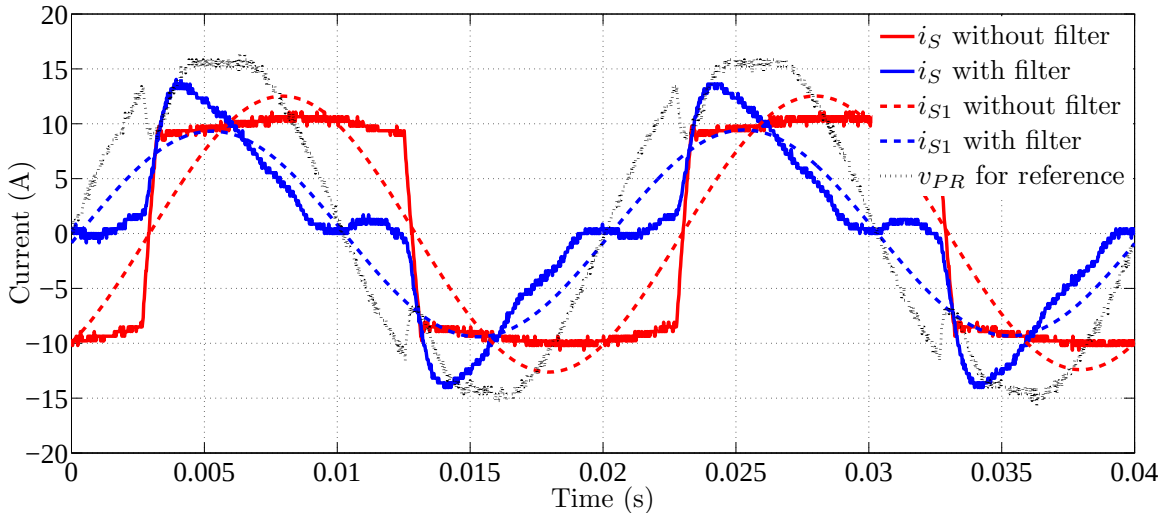

Figure 6.13: Comparison of Source Current with and without filters: Time domain

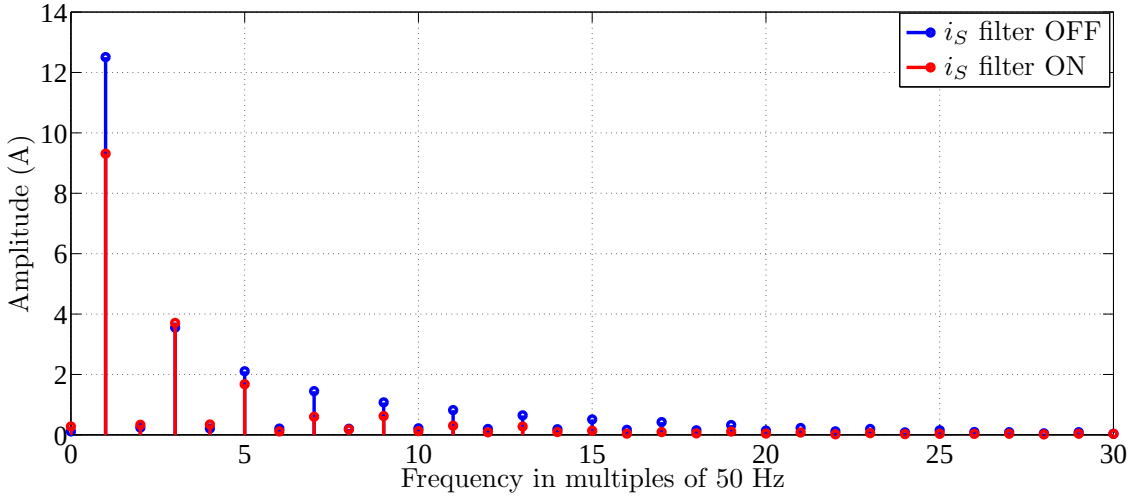

Figure 6.14: Comparison of Source Current with and without filters: Frequency domain

6.3.4 Experiments with and without series compensation: small commutating Inductance = 150 μH

In this experiment the commutating inductance is reduced to 150 μH and the voltage compensation is done with and without passive filter for two firing angles α. This is intended at studying the effect of commutating inductance on the current harmonics. The input voltage is maintained constant at 230 V. The voltage at the input to the rectifier V_{PR} is also maintained constant at 230 V, by series compensation (whenever $R_B = \infty$). The steady-state performance is tabulated in the Table 6.4. Some typical waveforms for the case of 60°are shown in Figures 6.15 through 6.18. And the post-processed waveforms are shown in Figures 6.19 through 6.22. It is observed that for the case of current source type of nonlinear loads there is not much change in the harmonic contents of the load current and hence that of the source current.

Table 6.4: $V_{PL} = V_{PR} = 230$ V, $L_R = 150$ μH, $I_O = 10$ A

α	Filter	I_S (A)	I_{ST} (A)	I_C (A)	V_{CC} (V)	V_{CL} (V)	V_{RECT} (V)	V_0 (V)	R_B (Ω)	P_0 (W)
30°	OFF	9.8	11.7	0	–	–	228.5	166.5	0	1665
	ON	8.8	10.1	0	–	–	227.5	164.5		1645
	OFF	9.6	11.4	9.9	36.5	20	228.6	155	∞	1550
	ON	9.4	11.5	9.6	36.54	17.27	229	172.1		1721
60°	OFF	9.85	11.5	0	–	–	227.6	99	0	990
	ON	7.0	7.9	0	–	–	229	**117.6**		**1176**
	OFF	9.8	12	10	36.9	26.6	229	78.2	∞	782
	ON	6.8	8	7	37	12.4	228.7	113.6		1136

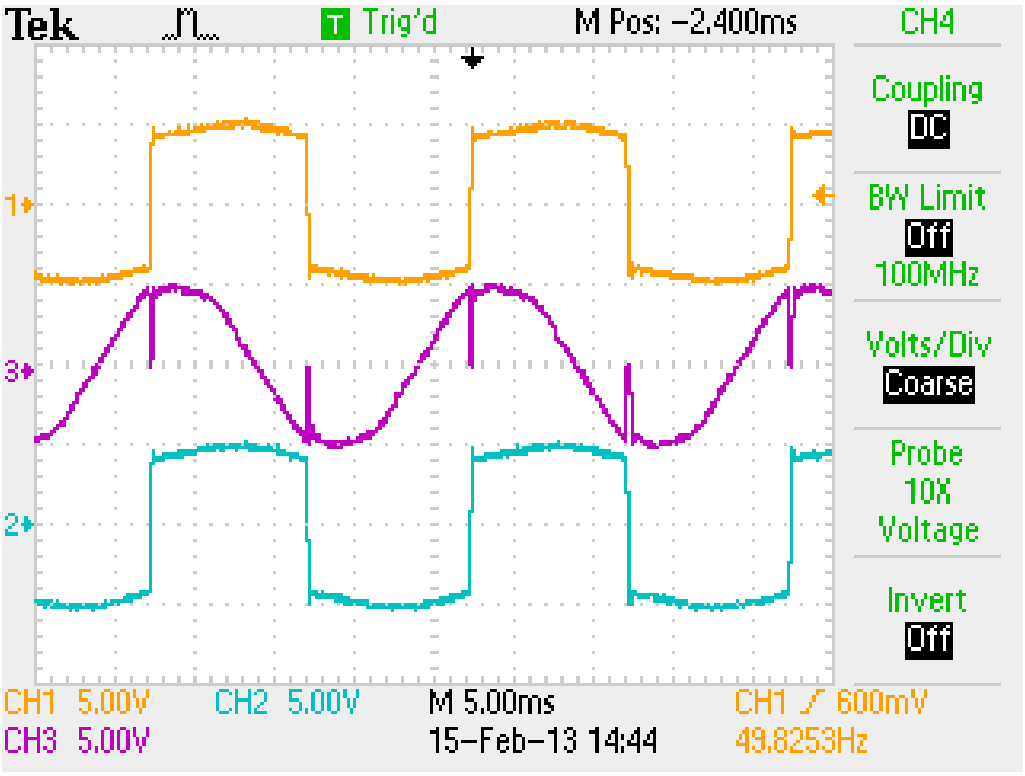

Figure 6.15: $\alpha = 60°$, Filters OFF, $R_B = 0$; Scale: Ch1 (i_S) and Ch2 (i_{RECT}) is 2.127 A/V and Ch3 ($v_{PR} = v_{PL}$) is 60.909 V/V

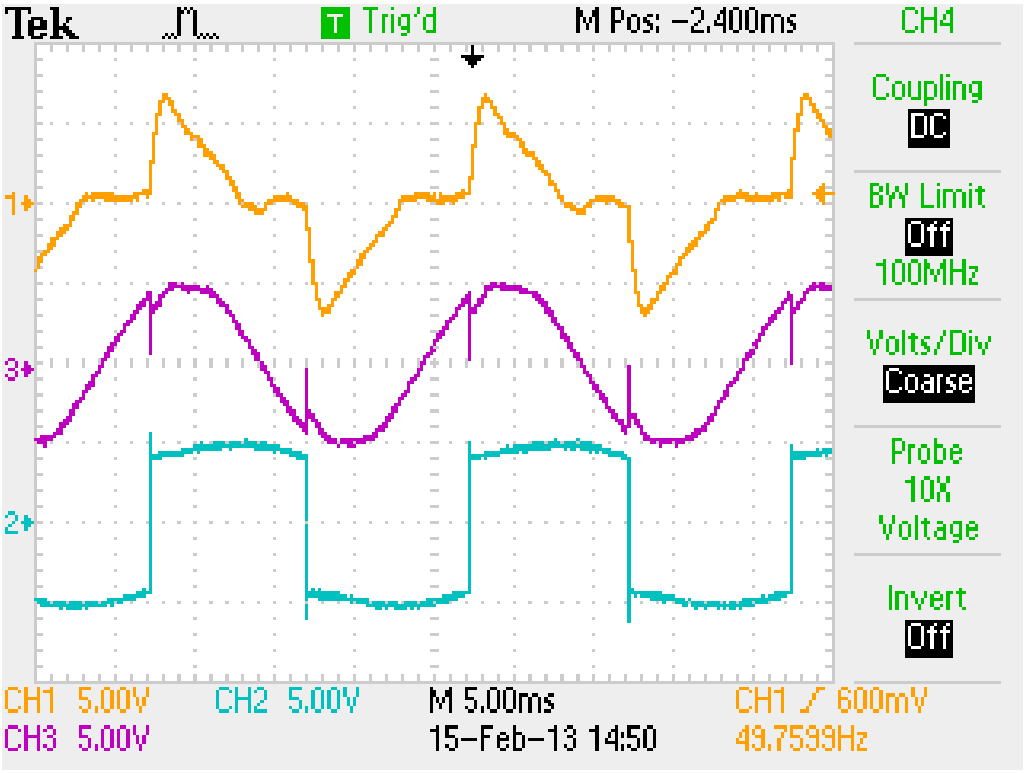

Figure 6.16: $\alpha = 60°$, Filters ON, $R_B = 0$; Scale: Ch1 (i_S) and Ch2 (i_{RECT}) is 2.127 A/V and Ch3 ($v_{PR} = v_{PL}$) is 60.909 V/V

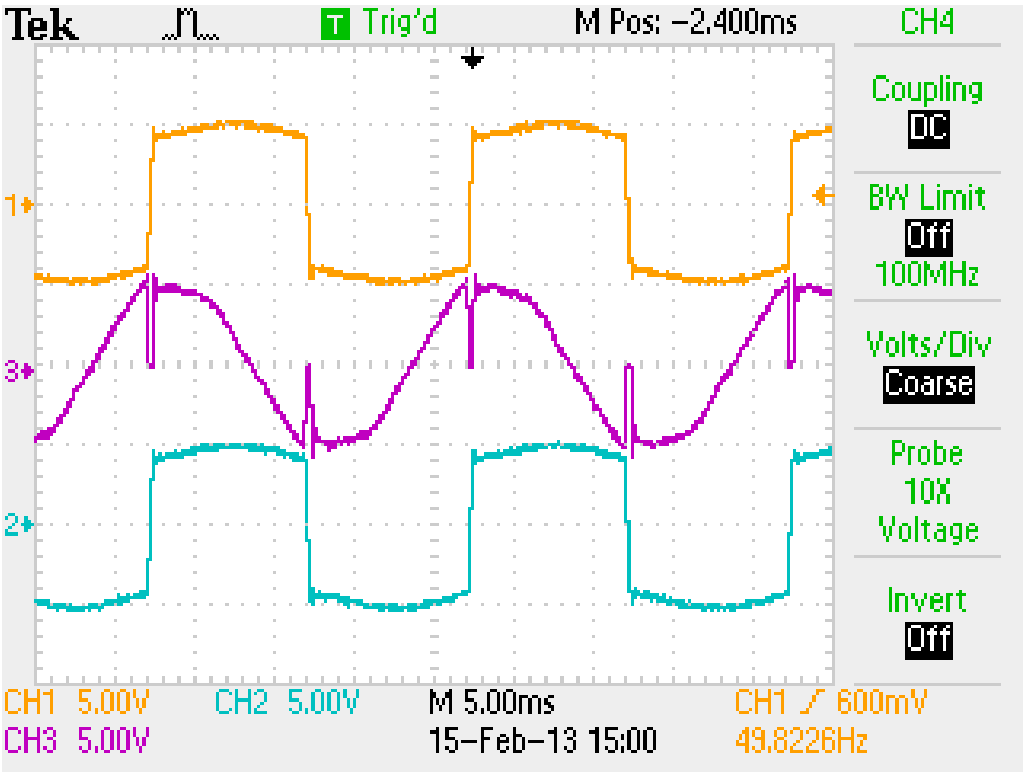

Figure 6.17: $\alpha = 60°$, Filters OFF,$R_B = \infty$; Scale: Ch1 (i_S) and Ch2 (i_{RECT}) is 2.127 A/V and Ch3 (v_{PR}) is 60.909 V/V

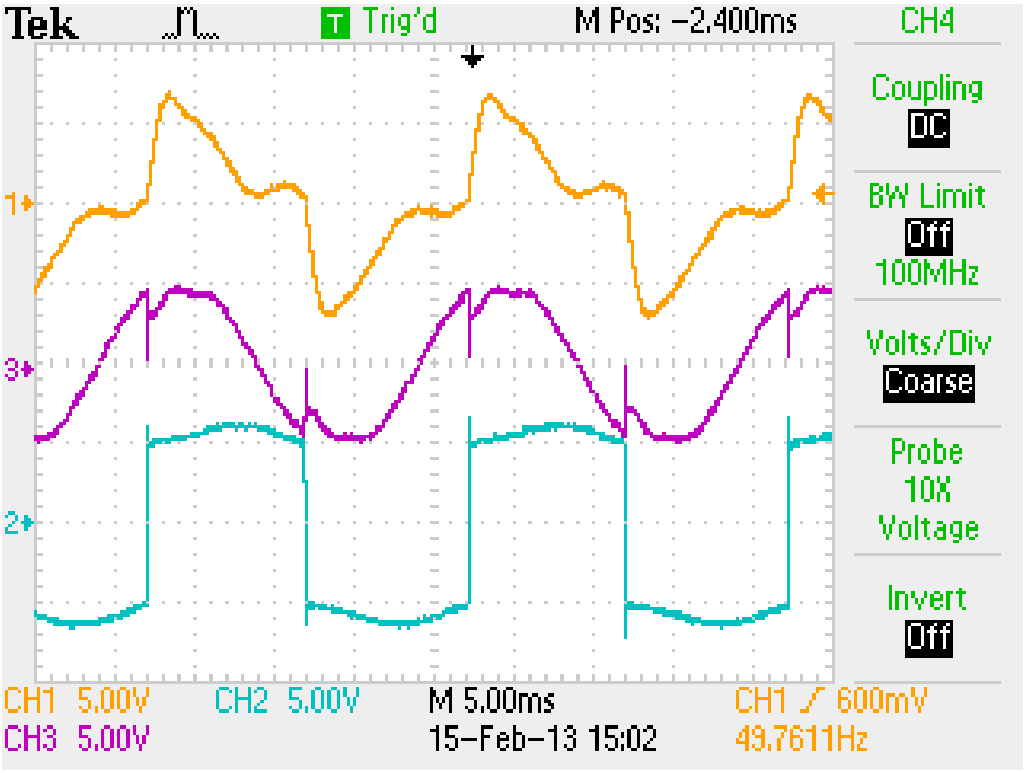

Figure 6.18: $\alpha = 60°$, Filters ON, $R_B = \infty$; Scale: Ch1 (i_S) and Ch2 (i_{RECT}) is 2.127 A/V and Ch3 (v_{PR}) is 60.909 V/V

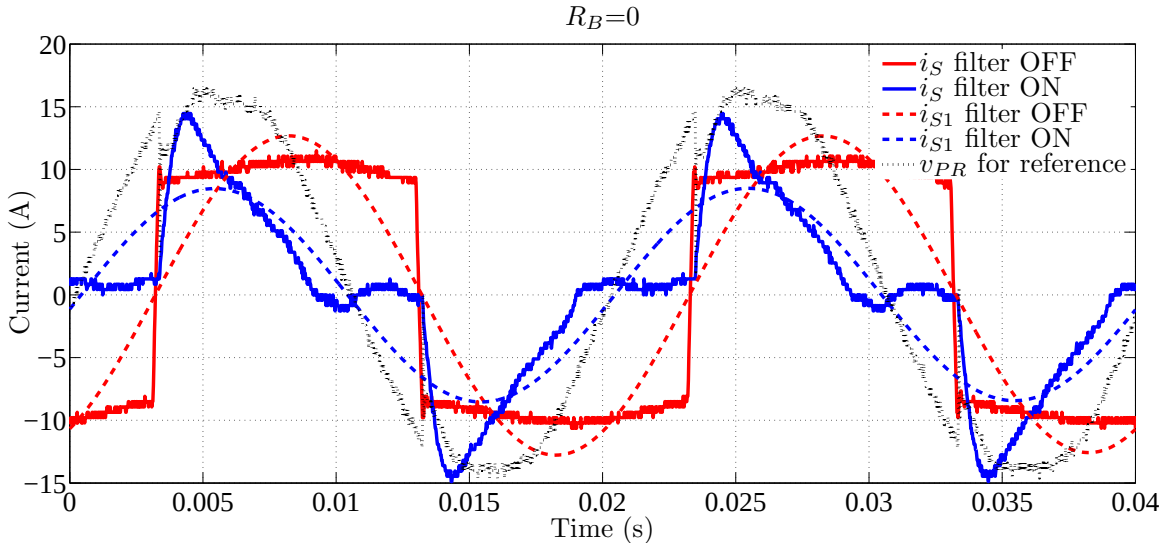

Figure 6.19: Comparison of Source Current with and without filters: Time domain

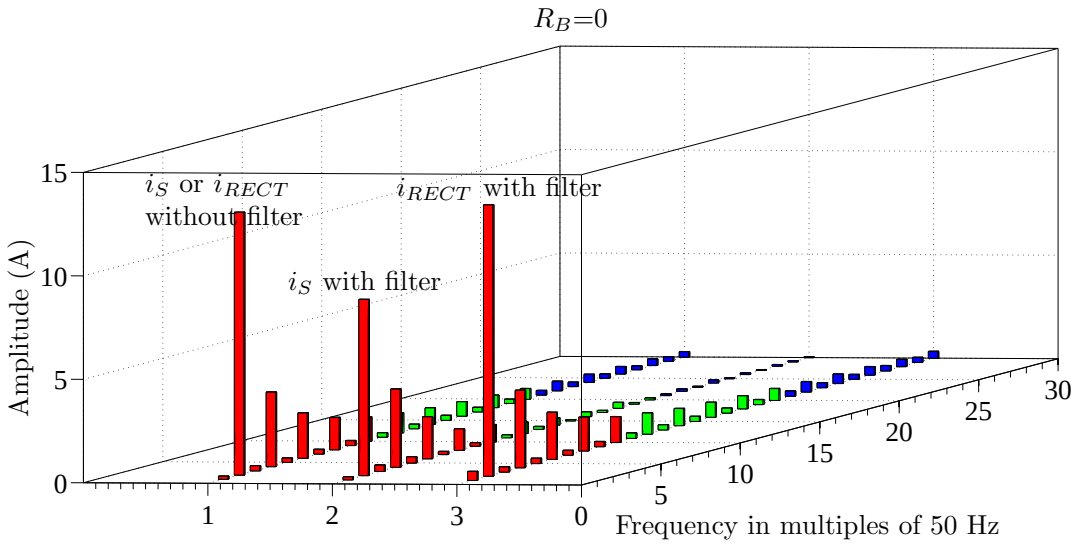

Figure 6.20: Comparison of Source Current with and without filters: Frequency domain

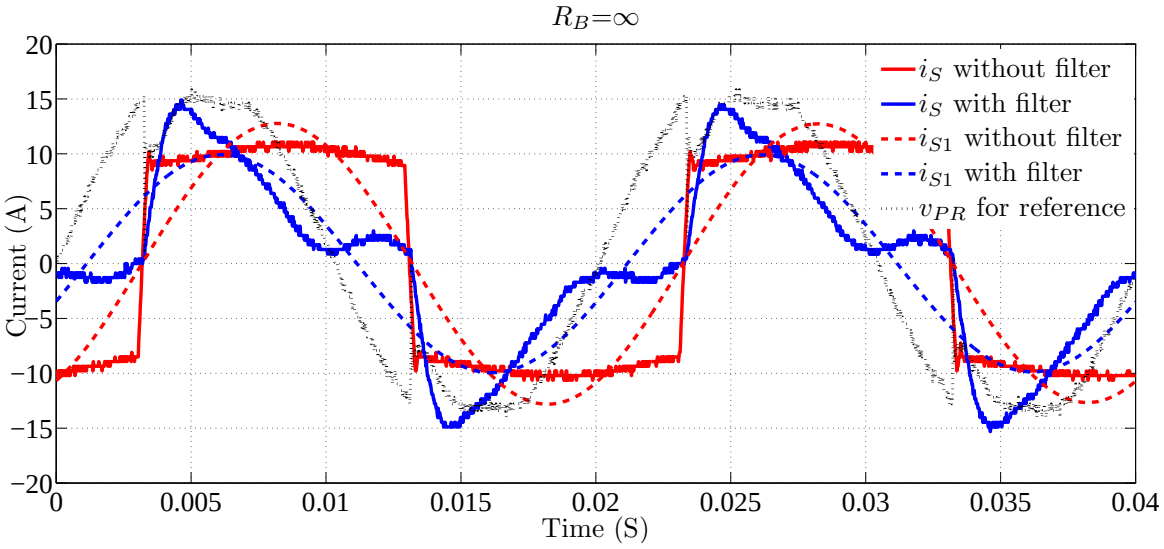

Figure 6.21: Comparison of Source Current with and without filters: Time domain

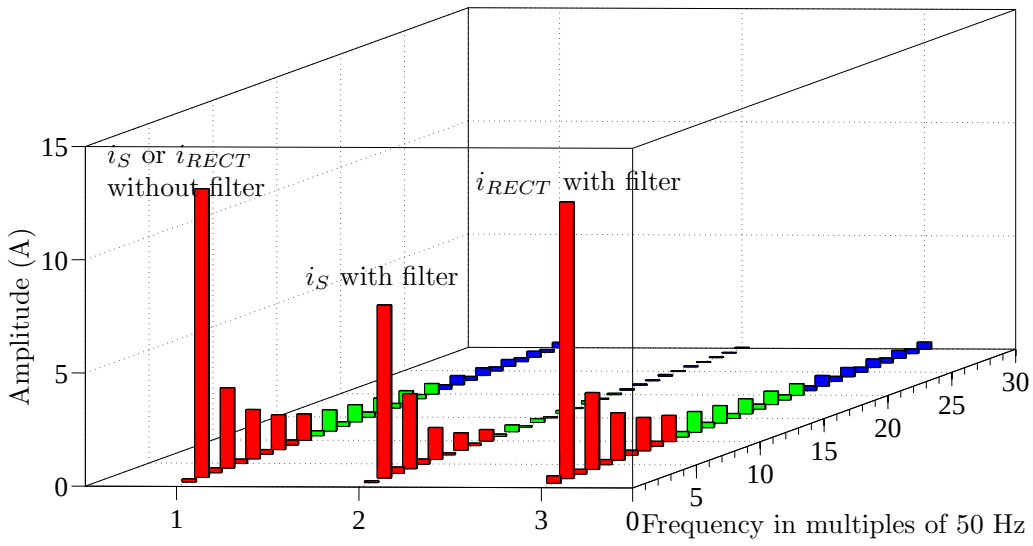

Figure 6.22: Comparison of Source Current with and without filters: Frequency domain

6.4 Results of experiments on inverter

The experimental setup for testing of the inverter are shown in Figures C.4 and C.5. This inverter can be used as a shunt current compensator with the two legs for single-phase three-level output and the other leg with the mid-point of the capacitor-bank can be switched as a half-bridge single-phase inverter to provide the series compensation. The inverter module is tested for operation under different conditions, with each leg tested as a chopper. The load consists of an inductor of 3.6 mH, in series with a capacitor of 3300 μF in parallel with a lamp-load as shown in Figure C.4. The inverter legs are tested with the DC bus voltage up to 600 V, the switching frequency up to 32 kHz, and an average current of up to 15 A in the inductor. It is tested for different duty ratios. The test results for few cases are presented in the following, with V_{DC} set to 400 V. The waveforms are captured directly with the TDS 2014C, 200MHz, 2GS/s, 4-channel DSO, without the Hall sensors to show the switching speed of the inverter legs. Only output voltage and the current waveforms are shown here,

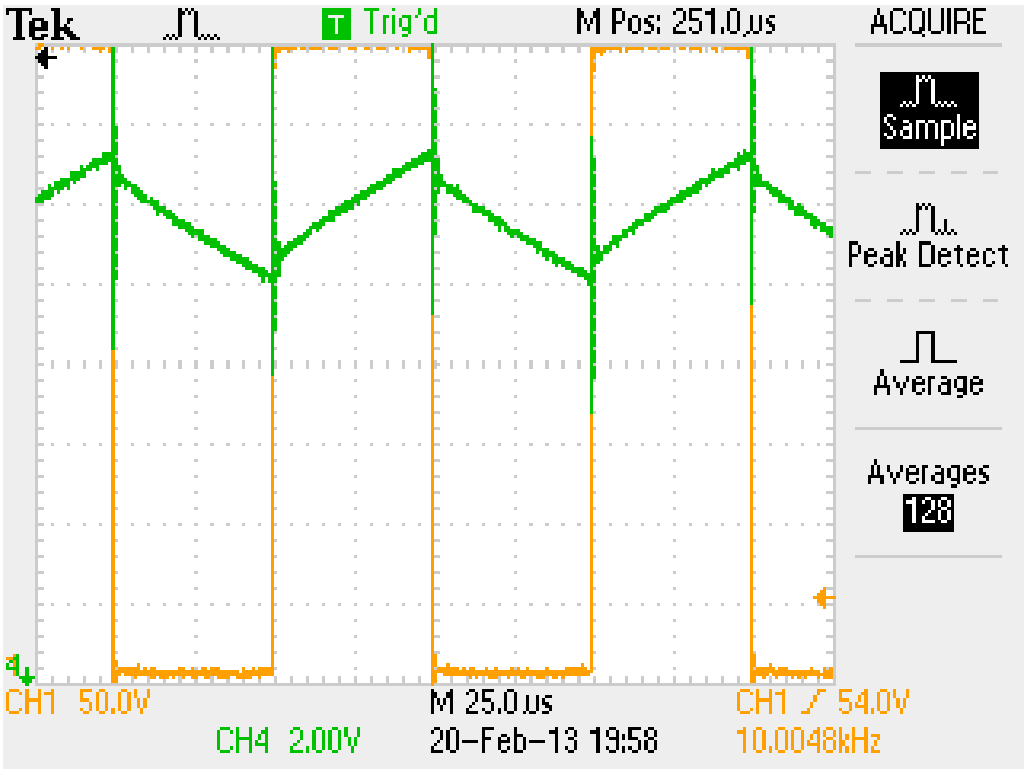

Figure 6.23: Inverter test waveform for the Case-1: Duty ratio=50 %, f_s=10kHz, I_{AVE}=12A; Legend (Scale): orange – voltage (V/V), green – current (A/V)

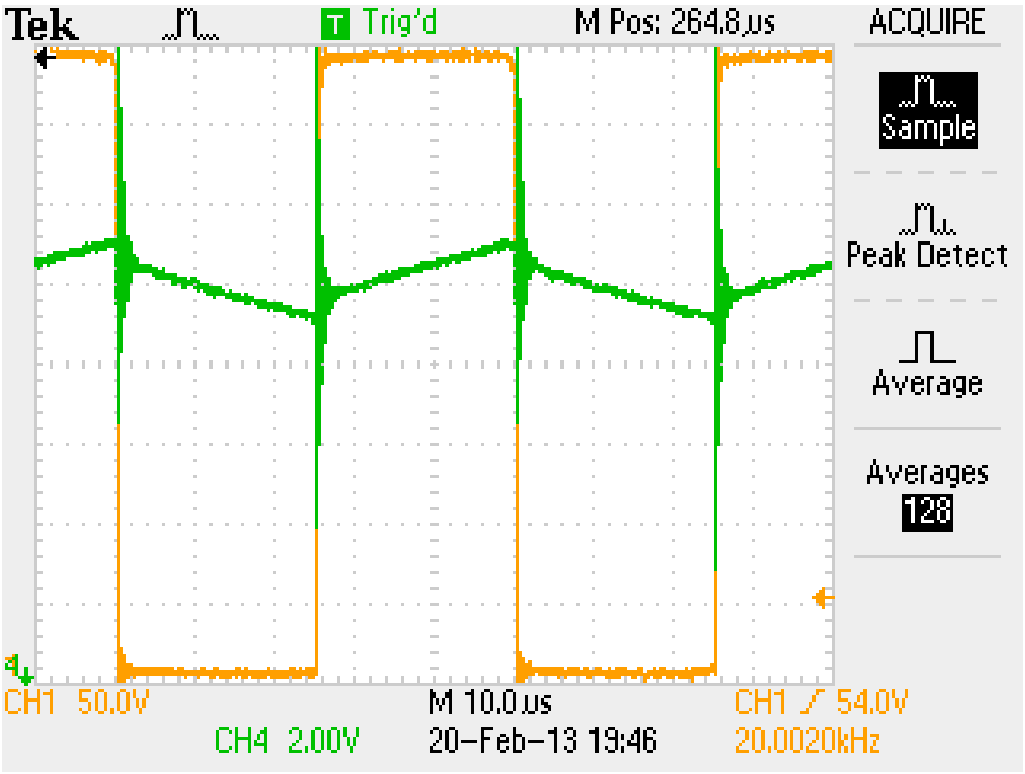

Figure 6.24: Inverter test waveforms for the Case-2: Duty ratio=50 %, f_s=20kHz, I_{AVE}=10A; Legend (Scale): orange – voltage (V/V), green – current (A/V)

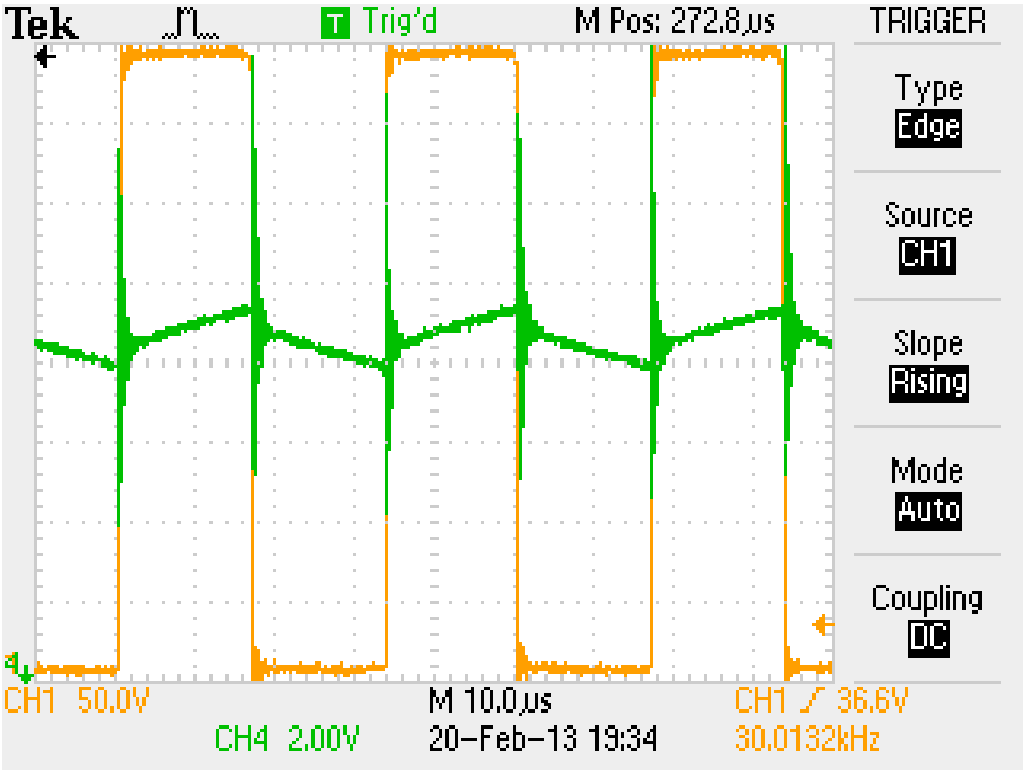

Figure 6.25: Inverter test waveforms for the Case-3: Duty ratio=50 %, f_s=30kHz, I_{AVE}=9A; Legend (Scale): orange – voltage (V/V), green – current (A/V)

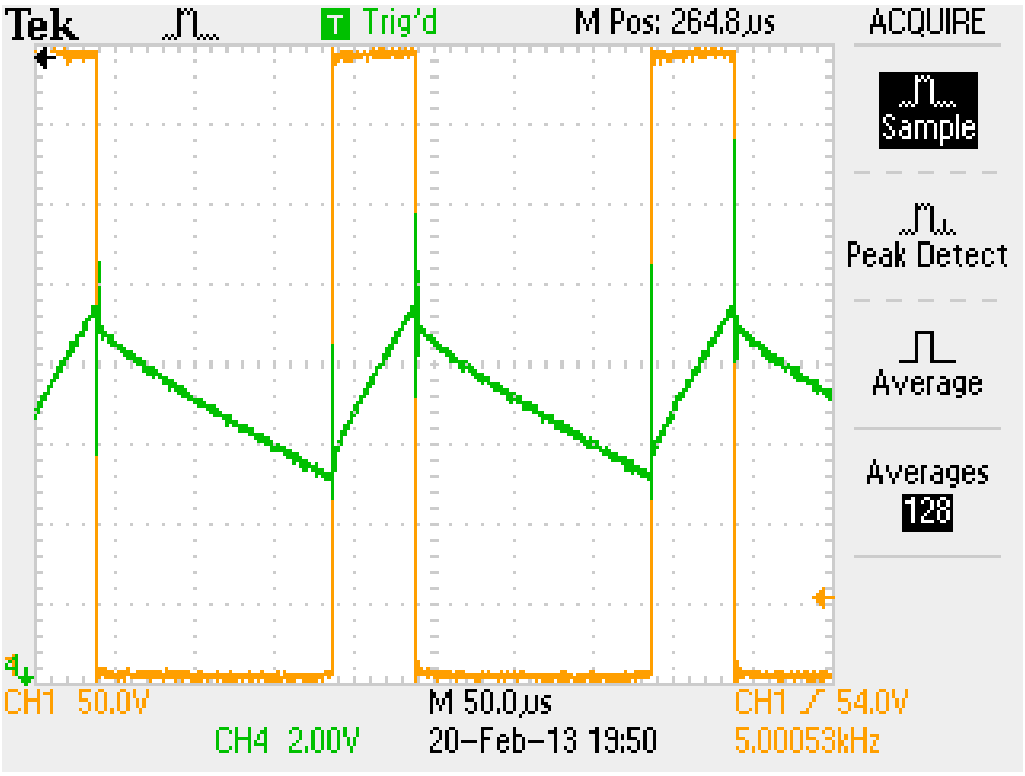

Figure 6.26: Inverter test waveforms for the Case-4: Duty ratio=25 %, f_s=5 kHz, I_{AVE}= 07 A; Legend (Scale): orange – voltage (V/V), green – current (A/V)

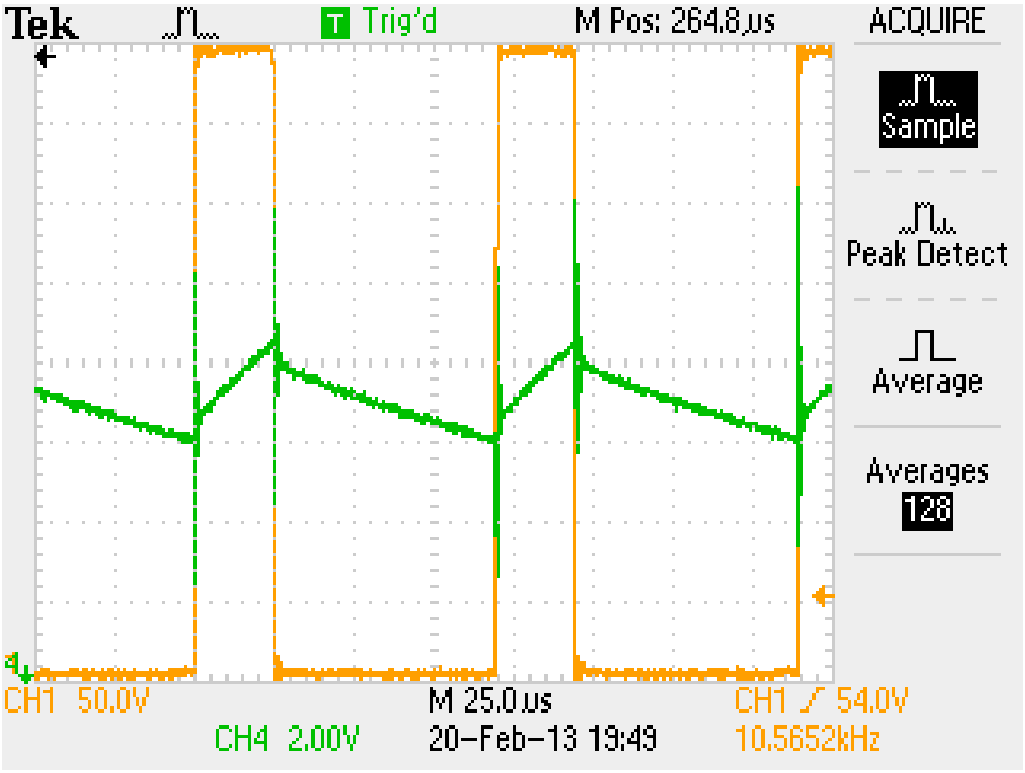

Figure 6.27: Inverter test waveforms for the Case-4: Duty ratio=25 %, f_s=10 kHz, I_{AVE}= 07 A, Legend (Scale): orange – voltage (V/V), green – current (A/V)

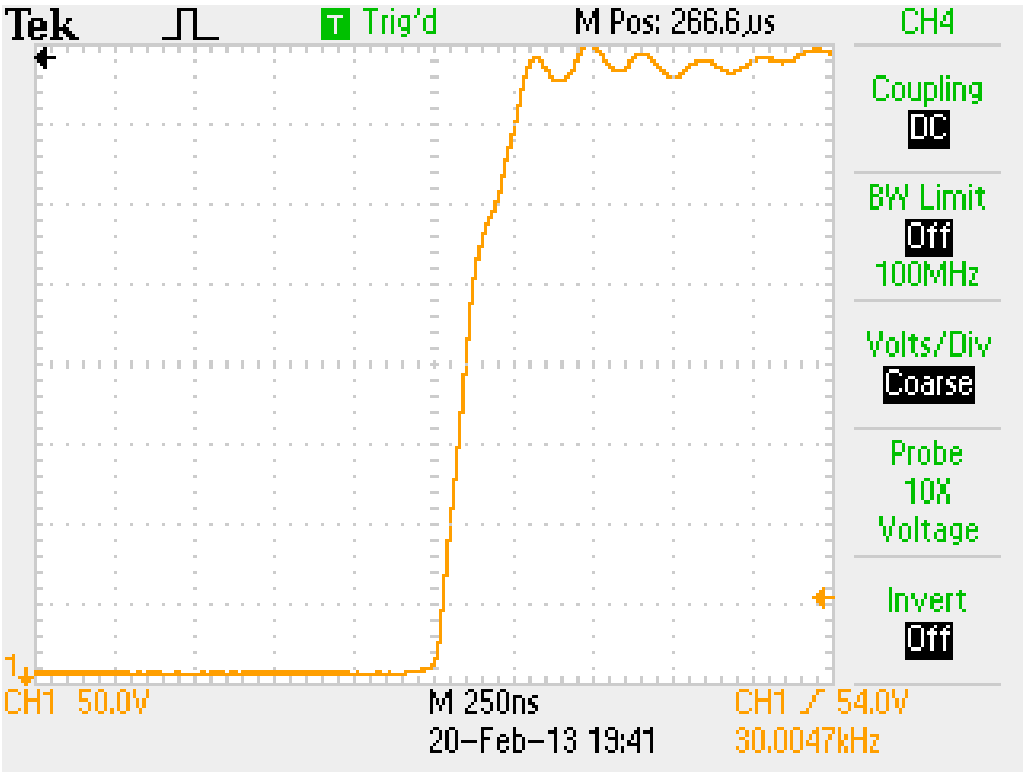

Figure 6.28: Voltage across the switch: Switching OFF transition

The switching ON transition (on the delayed sweep) is captured along with the periodic chopped waveform (on the main sweep) using such a facility on 54621A, 60 Mhz, 200 MSa/s Agilent Digital Storage Oscilloscope [Agilent Technologies(1999)] and is shown in Figure 6.29.

6.5 Conclusions

The hardware developed is tested and experiments are conducted. The system is operated with passive filter and tested for several combinations of load (power) and filter – series and shunt. The results for cases are presented and the post-processed results are presented. There is an improvement in the current waveforms for all the cases is observed. The reduction in the RMS current drawn from the source is considerable in all cases. Based on the experimental results of passive filter implementation the following conclusions can be drawn:

- The harmonic filters are not much effective without the series compensation. Hence the combination of PPF and SPF (in the left-shunt fashion) is necessary to render the PPF more effective. This is more so when the SCR of the utility

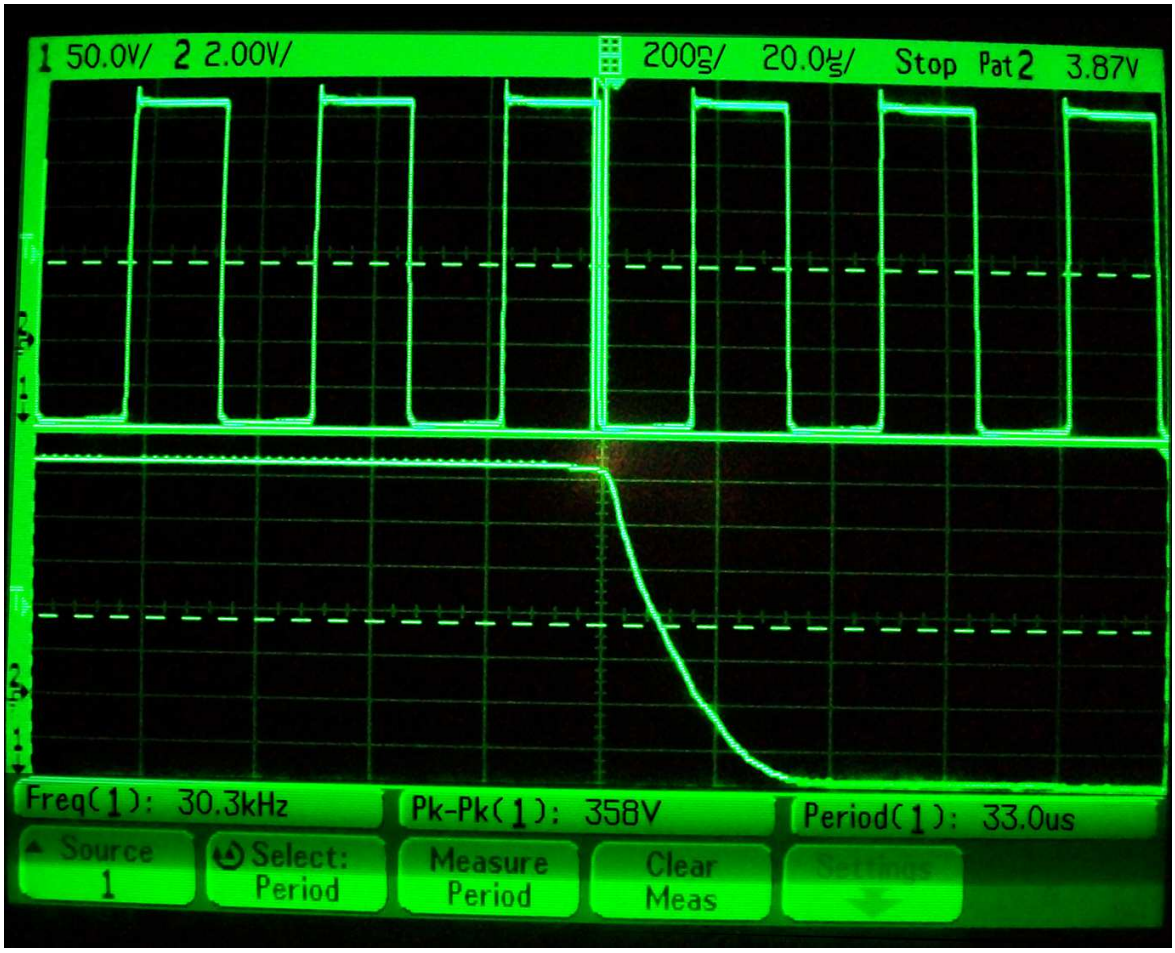

Figure 6.29: Voltage across the switch: Switching ON transition – Main (Top) and Delayed (Bottom) sweeps

at the PCC is good.

- The reactive power compensator is able to absorb considerable amount of reactive power, and thus it is very effective. It also acts as high-pass filter for harmonic currents.

- The active filters must take care of the residual harmonic current and reactive power compensation. The rating of the Active Filters will be very small and hence can be operated at a higher switching frequency.

The three-phase inverter developed is tested up to 600 V and 15 A. The results of operation from the inverter module are presented. The inverter is operated up to 32 kHz at 400 V and 12 A. The clean transient voltage waveforms across the device during switching is a testimony to the quality of the fabrication including the special structure of the DC bus employed. The transition times are of the order of 250 ns.

Chapter 7

Conclusions

7.1 Summary of Contributions

In this thesis it is attempted to determine a topology suitable for improving the Power Quality for a Current-Source type of Nonlinear Load. The options reported in the literature include either one or a combination from the set comprising of – a Commutating Inductor at the input to the rectifier, Parallel Passive Filter – tuned and reactive power compensator, Parallel Active Filter, Series Active Filter, or a Series Passive Filter. However for the case of CSNL a combination that meets the requirements of limiting the distortion of the line current and the voltage at the PCC and that at the input to the rectifier is not reported.

7.1.1 Power-Shield

In this study some favorable options guided by theoretical intuition are considered for exploration on the general topology considered. The guiding principles are as given below:

- The use of only Commutating Inductor will reduce the $\left(\frac{di}{dt}\right)$ and thus gives an impression that the input current distortion can be reduced. It has limited success and the negative side of the solution is that it increases the line notching of the voltage at the rectifier input and hence results in loss of (volt·second) available at the output. It also increases the distortion of the voltage at the input to the

rectifier which may cause difficulties in the control of the rectifier.

- The use of only SPF will result in the harmonic voltage drops across the series element given that the load is a CSNL, and thus has similar effects as that stated above.

- Hence a Parallel Passive Filter is mandatory to tame/convert the Stiff load current waveform to a smoother waveform which may be further improved, by other means – Series Active and/or Passive, and Parallel Active Filter.

- Only PPF, if adopted, may be susceptible to resonance with the source or to sinking the illegitimate currents upstream of the load, and may result in distortion of the voltage input to the rectifier if the SCR of the source is low.

- Thus a series compensator with a passive element is necessary and must be placed to the left of the PPF, i.e., on the upstream side of the PPF, for the same reason as mentioned earlier. This helps in further improving the source current, as well as the quality of voltage at the input to the rectifier.

- A PAF of a very low capacity placed at the PCC with the utility can be considered to supply the residual harmonic and reactive current.

- The Series Active Filter if considered can further improve the performance of the overall system.

On the basis of these guidelines several cases of parameters for the system and the load are considered. An analysis of the simulation results showed that a combination of a passive series compensator and a passive shunt compensator (in right-shunt fashion) is necessary to shape the source current and, to provide a quality voltage at the PCC and at the input to the rectifier. The series passive compensator may be the leakage reactance of the Series Active Compensator/ Filter as well, when such an option is considered. In that case, the passive shunt compensator must be a right-shunt. The PAF and SAF can be called upon to correct for the residues left-over after the effect of the passive compensators. The line commutating inductance of appropriate value is also included which resulted in an optimal improvement in the performance parameters.

This led to the conceptualization of a multifunction device – Power-Shield that can shield the source and the load from each other as far as the unwanted disturbances and pollution are concerned.

7.1.2 Novel compensating quantity extraction algorithms

Also comprising this thesis are two novel, input-locked, synchronized algorithms for the extraction of the compensating quantities. An extensive analysis of the algorithms is presented with rules for selection of the parameters. The algorithms have the features of a PLL and they are input amplitude-locked. They possess very good transient response, tracking capabilities, and steady-state performances in comparison with that class of algorithms. The noise and distortion rejection is very good. The real-time implementations in the dSPACE DS1006 based platform validated their suitability for application in the Active Filters.

7.1.3 Multi criteria based Hysteresis switching principle

A novel hysteresis switching principle utilizing the voltage at the **far-end** (in relation to the injecting converter) of the injection inductor is proposed. The significance of the influence of the **far-end** voltage on the injected current as modulated by that voltage is illustrated. This concept can lead to many techniques. In this thesis two schemes with different switching rules are implemented and compared with the basic hysteresis control. The performance parameters for comparison are defined. The following observations are presented:

- The illustration showed that the **far-end** voltage has significant modulation influence on the injected current.
- It is found that the Scheme-2 as referred has very good performance parameters like: minimum number of switchings per fundamental cycle, smallest fundamental amplitude as well as the constant component in the injected current.

These have advantages with regard to the switching stress on the devices and the EMI problems because of the reduced number of unipolar traverse of the pole voltages. Since

the fundamental component in the injected current is smaller, tracking will be better and faster, because it depends relatively lesser on the supervisory controller.

7.1.4 Hardware Implementation

A single-phase prototype of the system is developed and tested. It comprises of the following components:

- A single-phase thyristor controlled rectifier feeding a separately excited DC motor as an example of a current-stiff load is assembled. Parallel passive filters comprising of capacitor for reactive power compensation and tuned harmonic filters for harmonic compensation are designed, implemented, and tested. The test results and analysis thereof are presented.

- The three-phase inverter developed is tested up to 400 V and 12 A. The results of operation from inverter module are presented. The inverter is operated up to 32 kHz at 400 V and 12 A. The clean transient voltage waveforms across the device during switching is an indication of the quality of the special DC bus fabricated. The transition times are of the order of 250 ns.

- The components required for implementation of the closed loop control – inverters, signal sensing, signal conditioning, and analog and digital interface circuits are developed and test results are presented.

7.1.5 Publications

The work resulted in two journal papers [Gonda and David(2012), Gonda and David(2013)] and three conference papers [Gonda *et al.*(2009)], [Gonda *et al.*(2010)], and [Bhat *et al.*(2010)].

7.2 Scope for future work

On the basis of the extensive literature survey conducted and on the basis of the experience with the topology and the control technique considered, further work may be explored in the following directions.

A Phase-locked loop is a very important component in the implementation of any work related to power systems. Hence there is a scope for an Analog implementation of a good PLL. It can be either as a separate IC or embedded inside a DSC/ μC / FPGA. It must have the feature of generating higher frequency multiplier (in the range of few kilo hertz) to enable generation of synchronous sampling and switching signals. A more complex hysteresis controller can be implemented by a combination of current error, rate of change of error and the **far-end** voltage magnitude informations. The extension of the modeling procedure to larger networks and the procedure for extracting the system matrices, given the network connectivity information may be considered.

Appendix A

Cases and values of parameters used for simulation of Power-Shield

A.1 Parameter values for two sets of tuned filters

Note: TF_h – Tuned Filter of order h and Q – Quality factor of Inductor

A.1.1 Plausible Filter Parameter values

Order (h)	R_h (Ω)	L_h (mH)	C_h (μF)	Q	Remarks
3	5.68	90.5	12.5	15	$R_3 = 1$ MΩ for opening TF_3
5	2	32.85	12.5	25	
7	1	16.92	12.5	40	

A.1.2 Experimental Filter Parameter values

Order (h)	R_h (Ω)	L_h (mH)	C_h (μF)	Q	Remarks
3	1.0964	90.5	12.5	77.61	$R_3 = 1$ MΩ for opening TF_3
5	0.1789	32.85	12.5	288.29	
7	0.5179	16.92	12.5	71.81	

A.2 Values of Parameters – General/ Common

Symbols	Value	Units	Comments
		Load Parameters	
I_O	10	A	Output load current
R_O	3.375	Ω	Effective Resistance at the output of the rectifier
L_O	500	mH	DC Inductor (10 A)
E_O	Load Dependent	V	Back EMF of the DC motor
		Source Parameters	
V_S	230	V	RMS value of Nominal Supply voltage
f_S	50	Hz	Nominal value of Supply frequency
L_S	Variable	mH	Source Inductance
R_S	398	mΩ	Source Resistance
		Left current compensator parameters	
R_1	OPEN/ SHORTED	Ω	OPEN= 1 MΩ / SHORTED = 0.1Ω
L_1	15 or 25	mH	Left Current-Injector Inductor
		Right current compensator parameters	
R_2	OPEN/ SHORTED	Ω	OPEN= 1 MΩ / SHORTED = 0.1Ω
L_2	15	mH	Right Current-Injector Inductor
		Series compensator	
R_B	OPEN/ SHORTED	Ω	Series compensator Bypass Resistor; OPEN= 1 MΩ / SHORTED = 0.1Ω
		Series transformer specifications	
R_4	0.1	Ω	Winding resistance of the Series transformer
L_4	75	mH	Self inductance of the Series transformer
R_6	0.1	Ω	Winding resistance of the Series transformer
L_6	75	mH	Self inductance of the Series transformer
κ	Variable		Mutual Coupling Coefficient, varied to show its effect on filtering
		Series injector and Filter	
v_C	–	V	Dependent on load and source variations
L_v	100	μH	Filter cut-off frequency dependent (Value shown indicates)
R_L	0.1	Ω	SHORTED
C_v	1	μF	Filter cut-off frequency dependent (Value shown indicates OPEN)
R_C	1	MΩ	OPEN (C_V is OPEN)
		Reactive Power Compensator	
C_Q	Variable	μF	Switched Power factor correction Capacitor, depending on the load
R_Q	5 or 50 m or 1 M	Ω	Damping Resistance

A.3 List of Cases considered for simulation with PAF, SPF, and PPF

Cases	Scheme	L_S (H)	E_O(V)	C_Q (μF)	R_B (Ω)	κ
1	2	15e-3	12	75	SHORTED	
2	2	15e-3	110	50	SHORTED	
3	1	15e-3	12	75	SHORTED	
4	Basic	15e-3	12	75	SHORTED	
5	Basic	15e-3	110	50	SHORTED	
6	1	15e-3	110	50	SHORTED	
7	1	711e-6	12	75	OPEN	0.9925
8	2	711e-6	12	75	OPEN	0.9925
9	1	711e-6	110	50	OPEN	0.9925
10	2	711e-6	110	50	OPEN	0.9925
11	Basic	711e-6	12	75	OPEN	0.9925
12	Basic	711e-6	110	50	OPEN	0.9925

A.4 List of Additional Cases considered for simulation with PAF, SPF, and PPF

Table A.1: Parameters for Simulation Studies Guiding Conclusion

Cases	E_O (V)	R_1 (Ω)	L_1 (mH)	Scheme	f_{sw} (kHz)	R_B (Ω)	R_4 (Ω)	L_4 (mH)	R_6 (Ω)	L_6 (mH)	κ	R_L (Ω)	R_Q (Ω)	C_Q (μF)	Remark
1	12	0.1	15	Basic	Free	SHORT	NA	NA	NA	NA	NA	NA	NA	NA	Only PAF
2	110	0.1	15	Basic	Free	SHORT	NA	NA	NA	NA	NA	NA	NA	NA	
3	12	0.1	15	Basic	15	SHORT	NA	NA	NA	NA	NA	NA	NA	NA	
4	12	1 M	15	NA	NA	SHORT	NA	NA	NA	NA	NA	NA	5	75	Only PPF
5	12	1 M	15	NA	NA	OPEN	0.1	75	0.1	75	0.95	0.1	5	75	SPF+PPF
6	12	0.1	25	Basic	Free	OPEN	0.1	75	0.1	75	0.95	0.1	5	75	PAF+PPF
The following cases refer to Power-Shield – incorporating PAF+SPF+PPF and its variants															
7	12	0.1	25	Basic	Free	OPEN	0.1	75	0.1	75	0.95	0.1	5	75	
8	110	0.1	15	Basic	Free	OPEN	0.1	10	1 M	0.075	0.195	1 M	0.05	50	Only L_4 & r_Q
9	70	0.1	25	Scheme-2	25	OPEN	0.1	75	0.1	75	0.95	0.1	0.05	62.5	r_Q
10	162	0.1	25	Scheme-2	15	OPEN	0.1	75	0.1	75	0.95	0.1	5	21.5	..to Case-11
11	162	0.1	25	Scheme-2	15	OPEN	0.1	75	0.1	75	0.95	1 M	5	21.5	..to Case-10
12	145	0.1	25	Scheme-2	15	OPEN	0.1	75	0.1	75	0.95	0.1	5	36	..to Case-13
13	145	0.1	25	Scheme-2	15	OPEN	0.1	75	0.1	75	0.95	0.1	5	50	..to Case-12
14	70	0.1	25	Scheme-1	25	OPEN	0.1	75	0.1	75	0.95	0.1	0.05	62.5	..to Case-9
The following cases refer to Power-Shield – incorporating PAF+SPF+PPF and with Tuned Filter used in Experiment															
15	70	0.1	25	Scheme-2	25	OPEN	0.1	75	0.1	75	0.95	0.1	0.05	62.5	..to Case-9,14
16	145	0.1	25	Scheme-2	25	OPEN	0.1	75	0.1	75	0.95	0.1	5	36	..to Case-12

Note: r_Q to indicate small value of R_Q.

A.5 Simulink Schematic of the Power-Shield

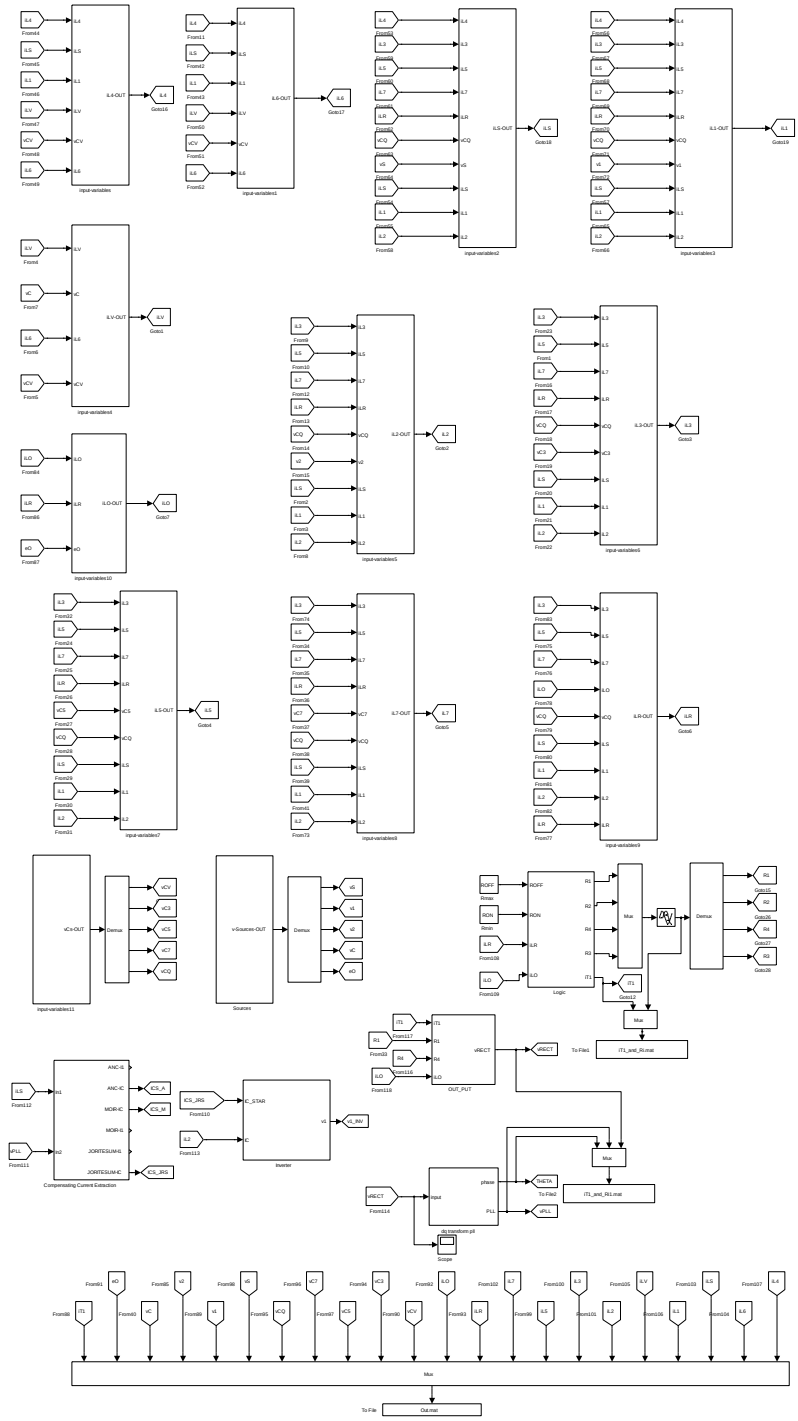

Figure A.1: Simulink Schematic of the Power-Shield

Appendix B

Hardware: Schematics, Circuits, and Pictures

B.1 Digital I/O board

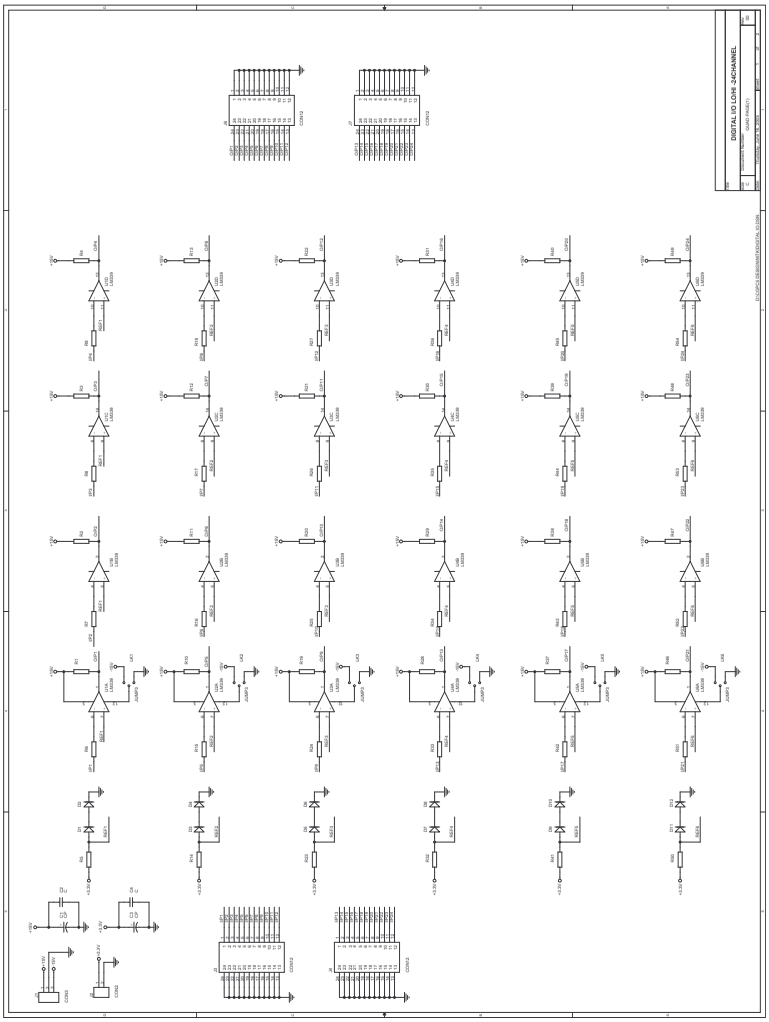

Figure B.1: Digital input-output, level shifter card schematic: LOW to HIGH

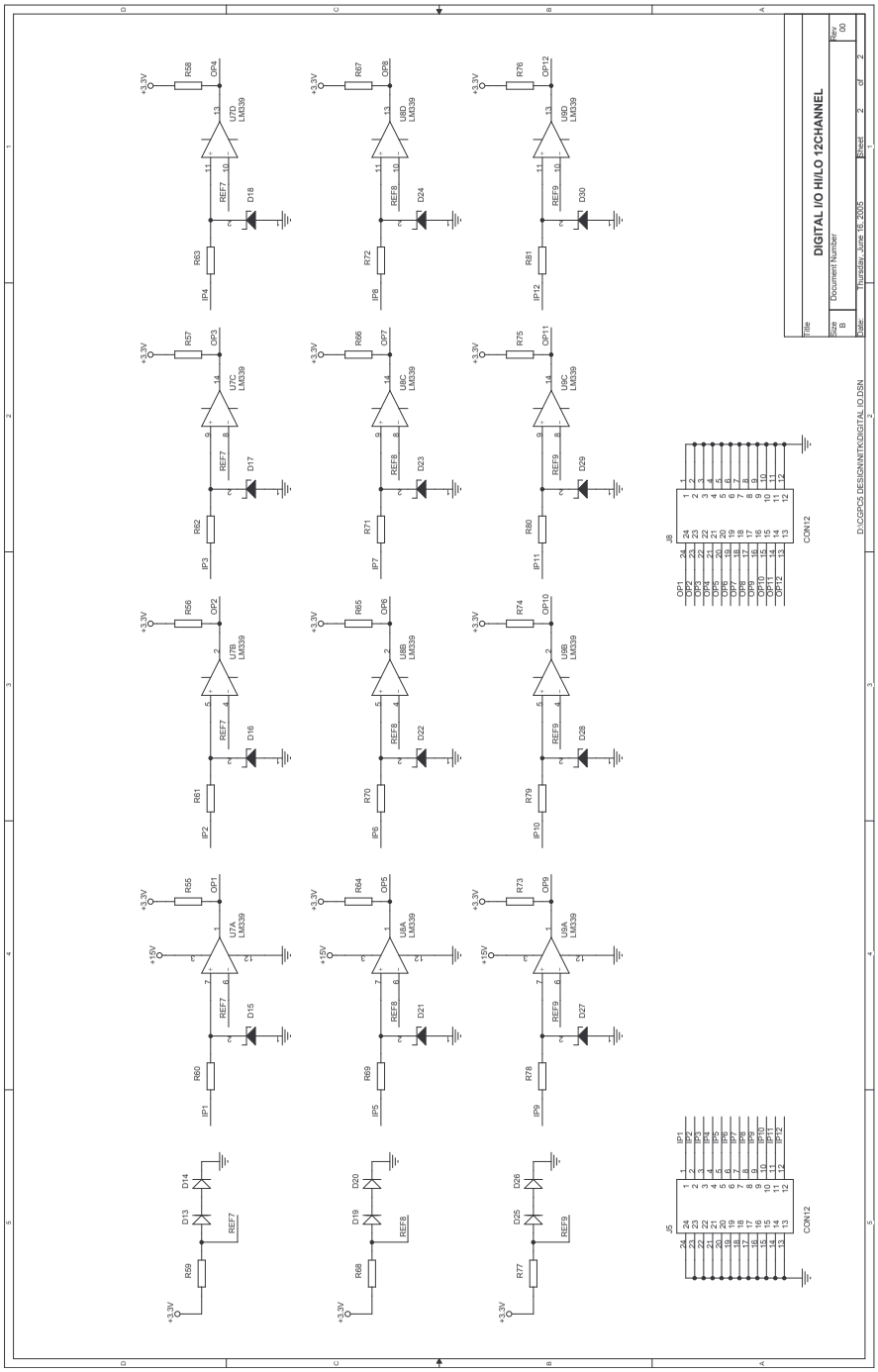

Figure B.2: Digital input-output, level shifter card schematic: HIGH to LOW

B.2 Analog level-shifter and conditioning board

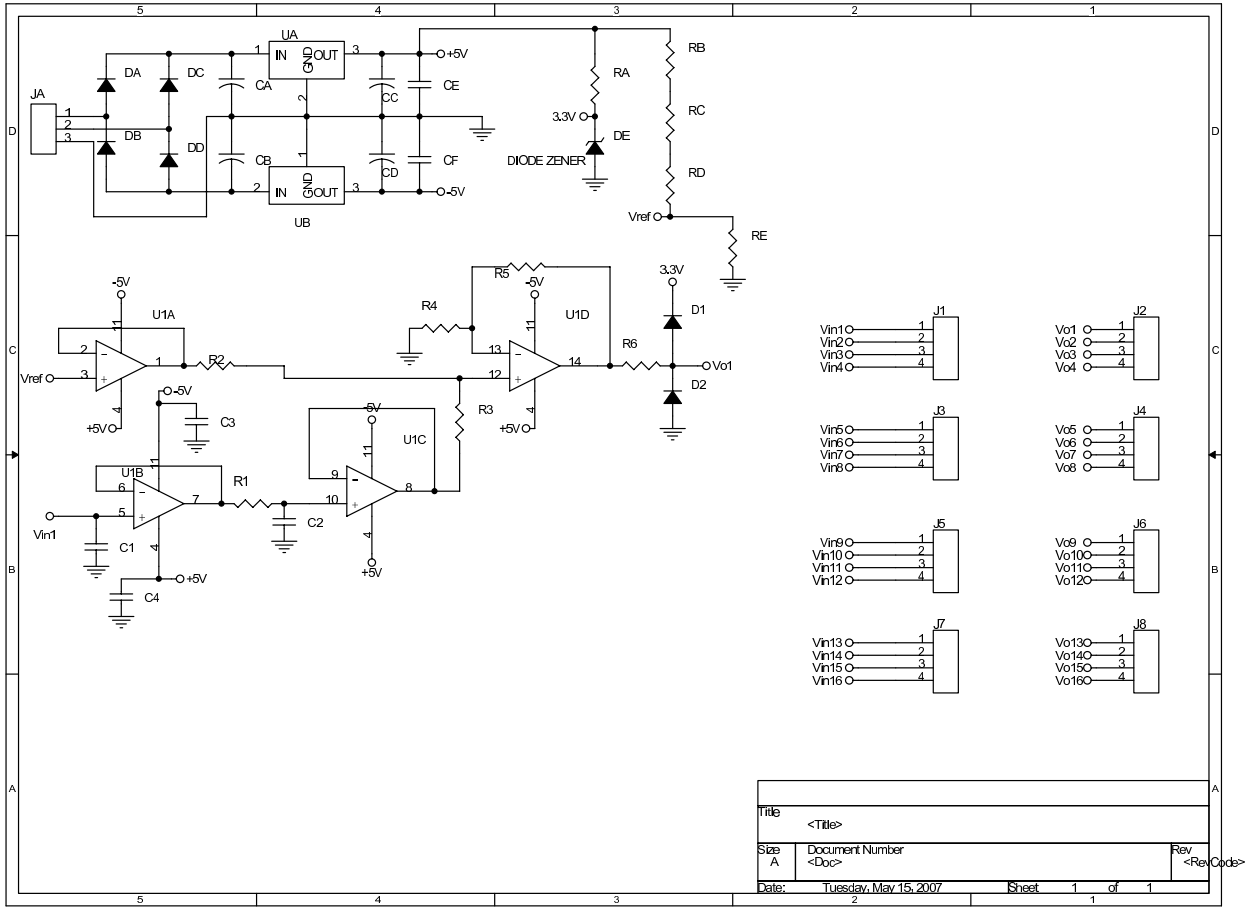

Figure B.3: Schematic of the Analog Level-Shifter

B.2.1 Pictures of DIO and Analog Boards

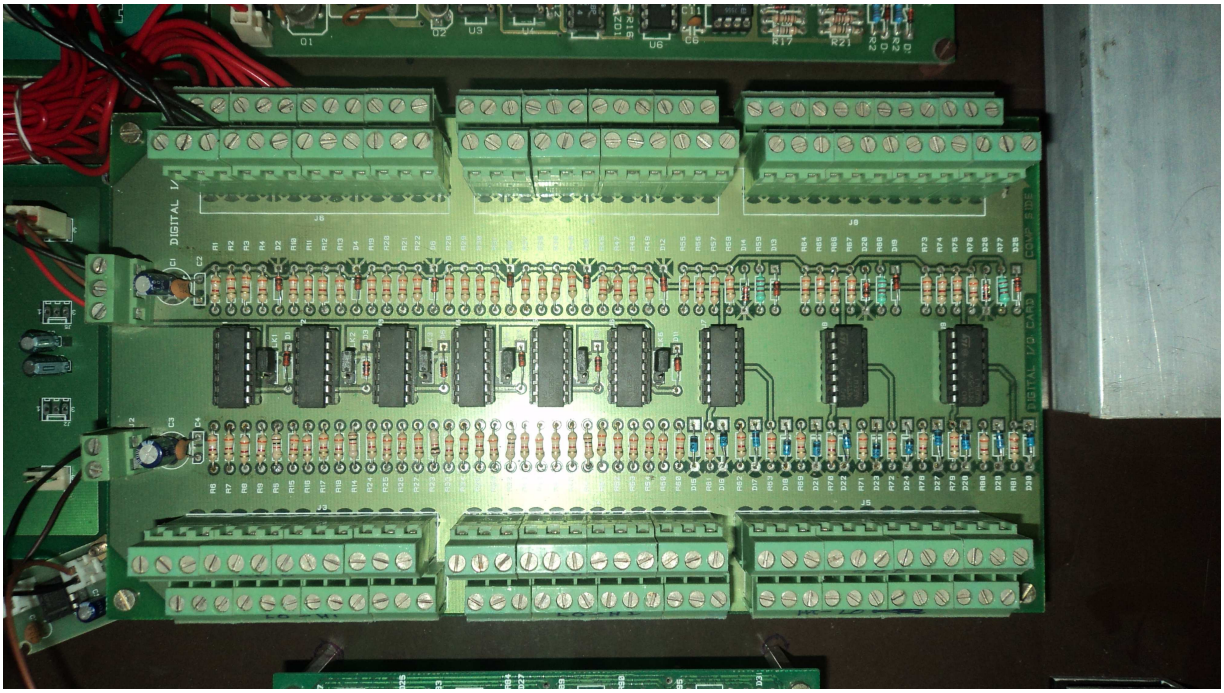

Figure B.4: Digital input-output, level shifter card

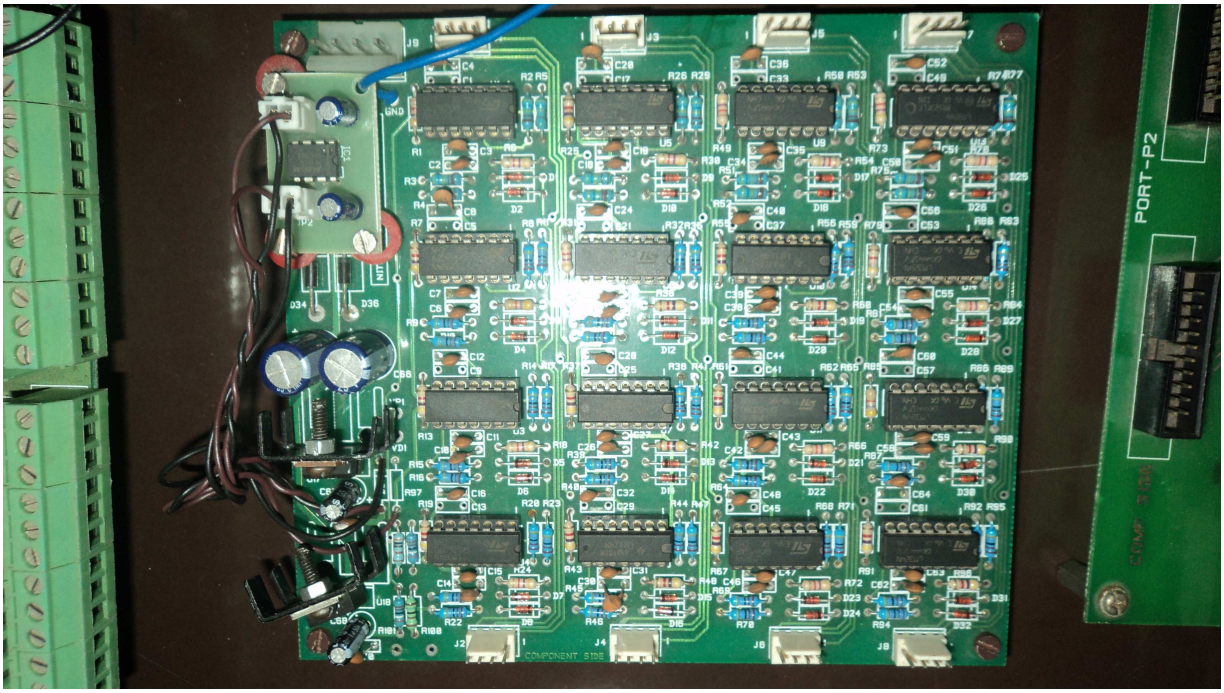

Figure B.5: Analog level shifter card

B.3 Inverter modules

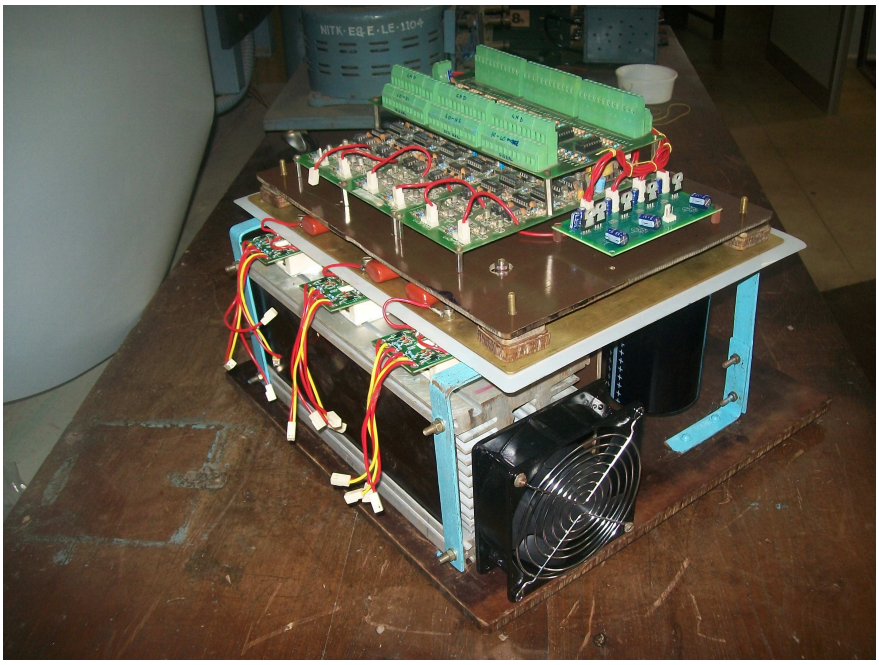

Figure B.6: Three-phase Inverter module: View-1

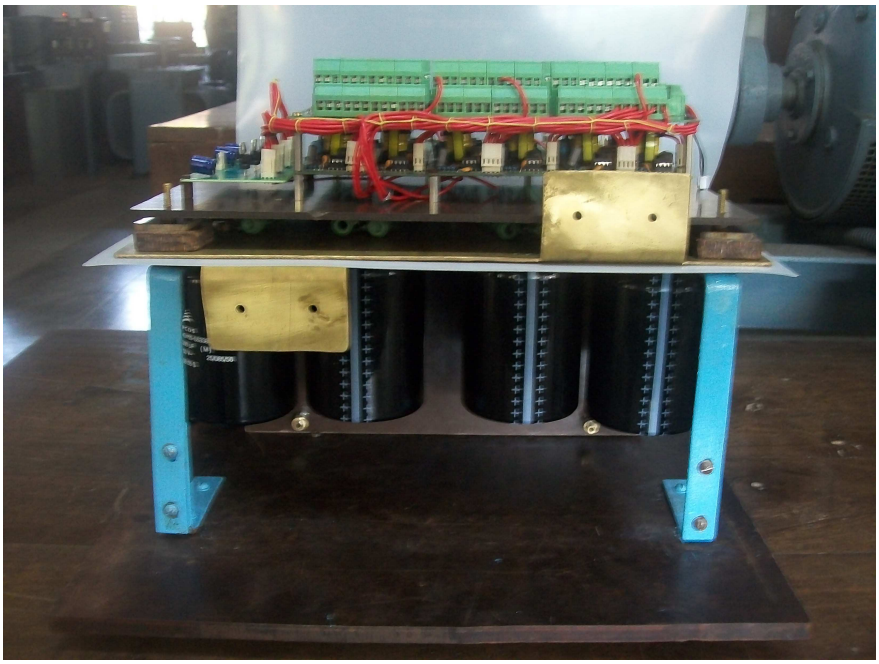

Figure B.7: Three-phase Inverter module: View-2

B.4 Current sensor card: Schematic

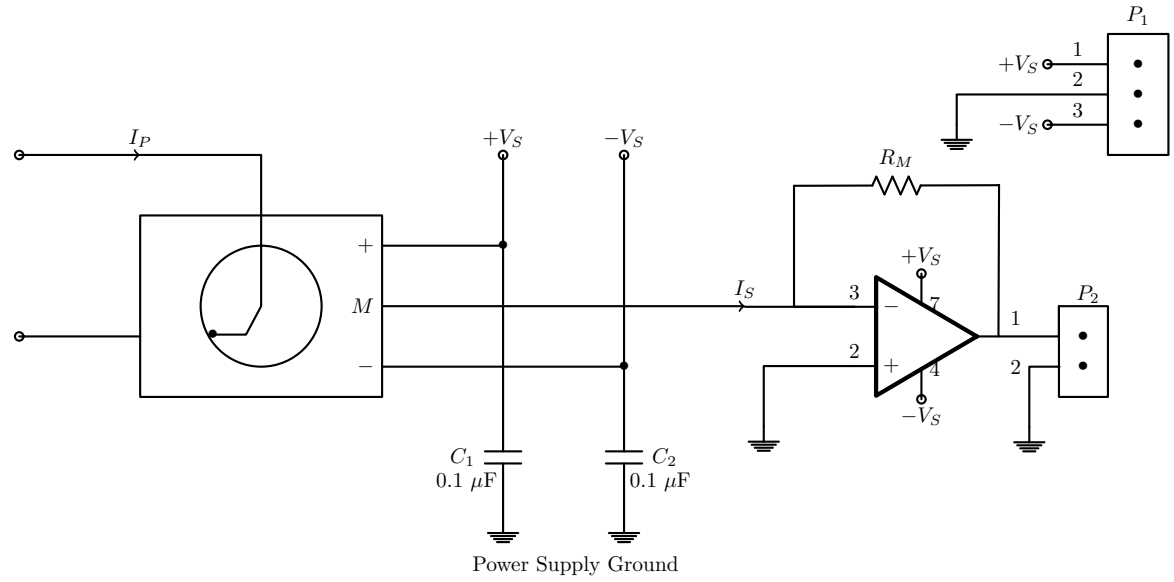

Figure B.8: Current sensor schematic

B.5 Voltage sensor card: Schematic

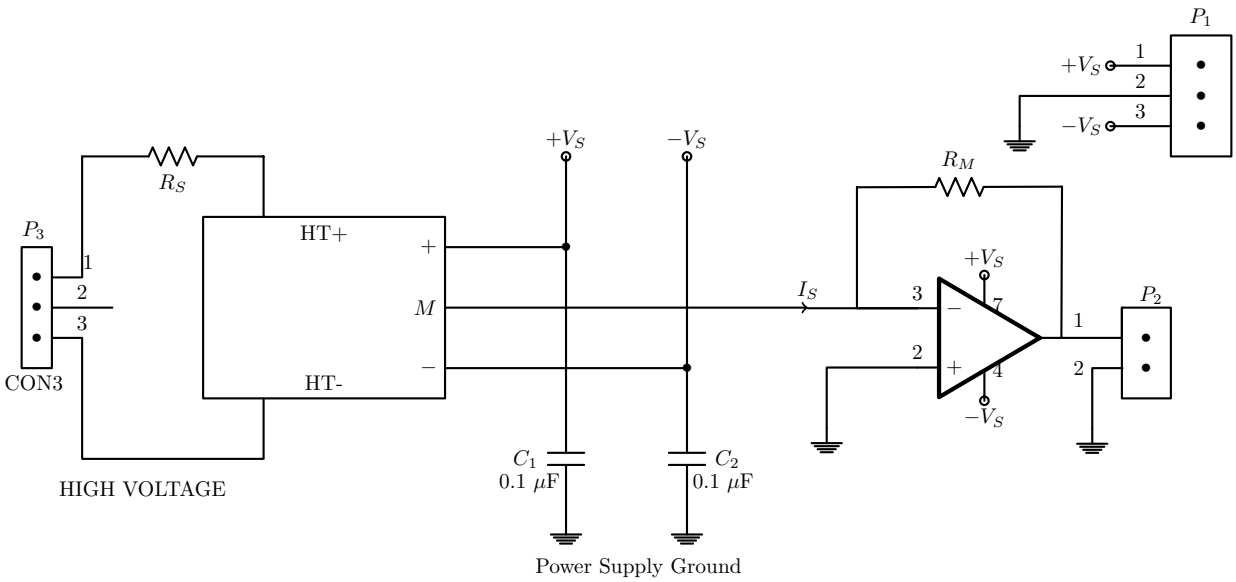

Figure B.9: Voltage sensor schematic

B.6 Voltage sensor card

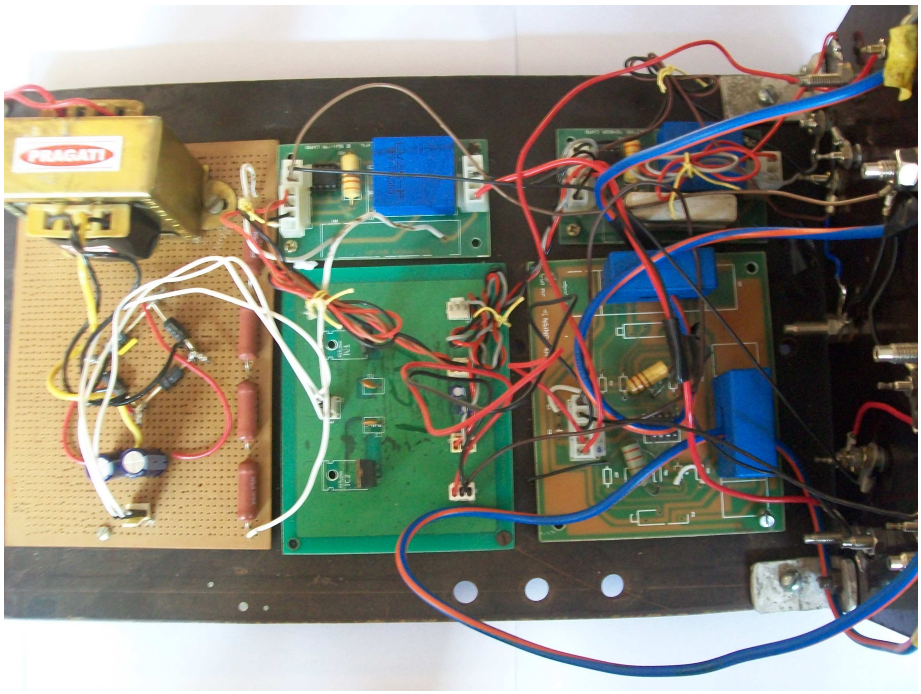

Figure B.10: Voltage and Current sensor card

B.7 Test-zig Schematic

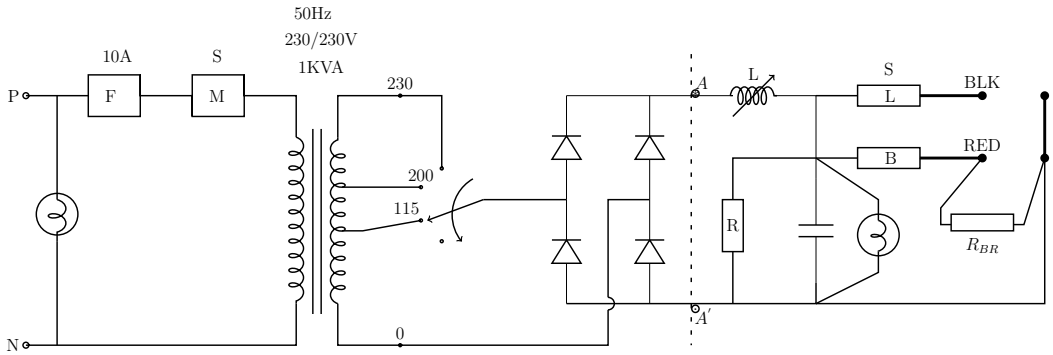

Figure B.11: Test-Zig Circuit Schematic

B.8 Test-zig Setup

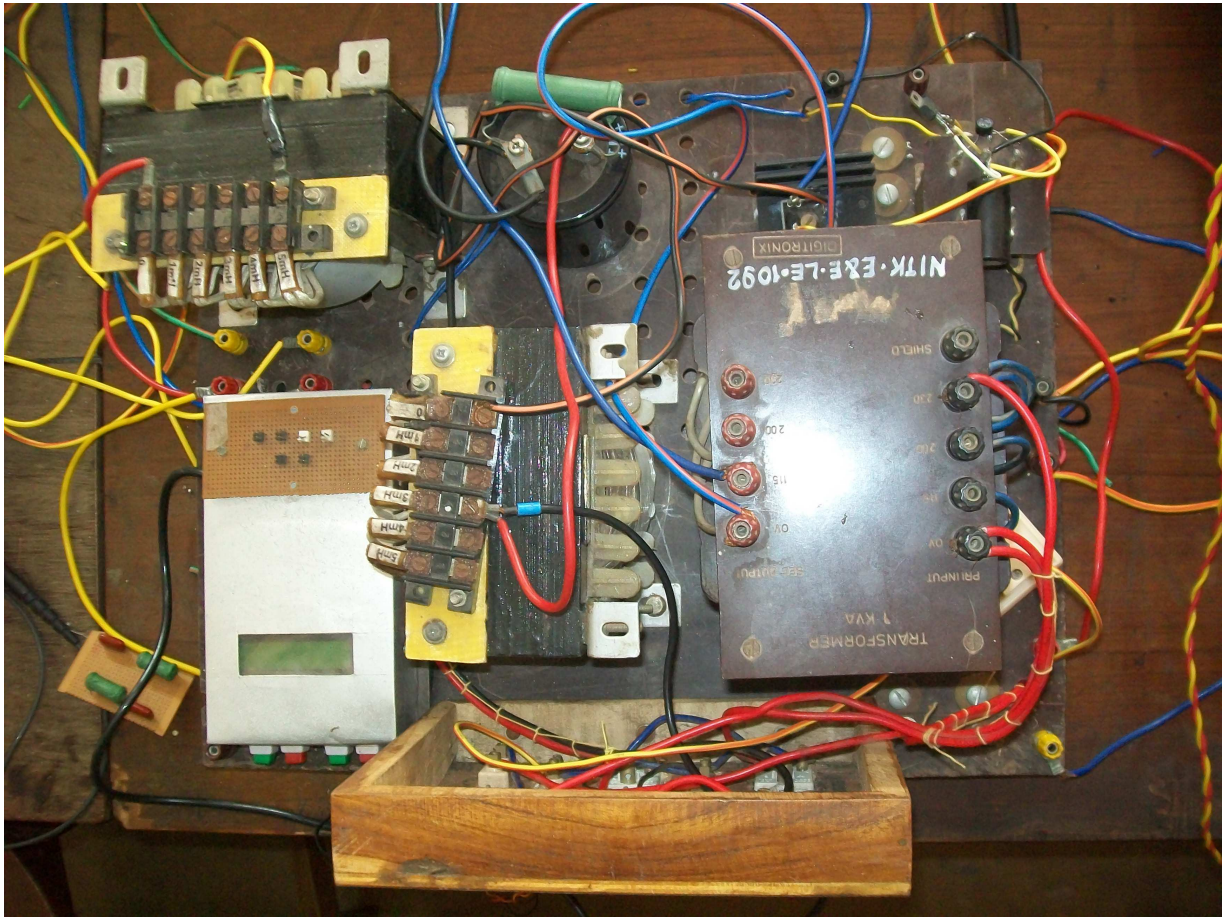

Figure B.12: Test-Zig Setup

B.9 Other accessories

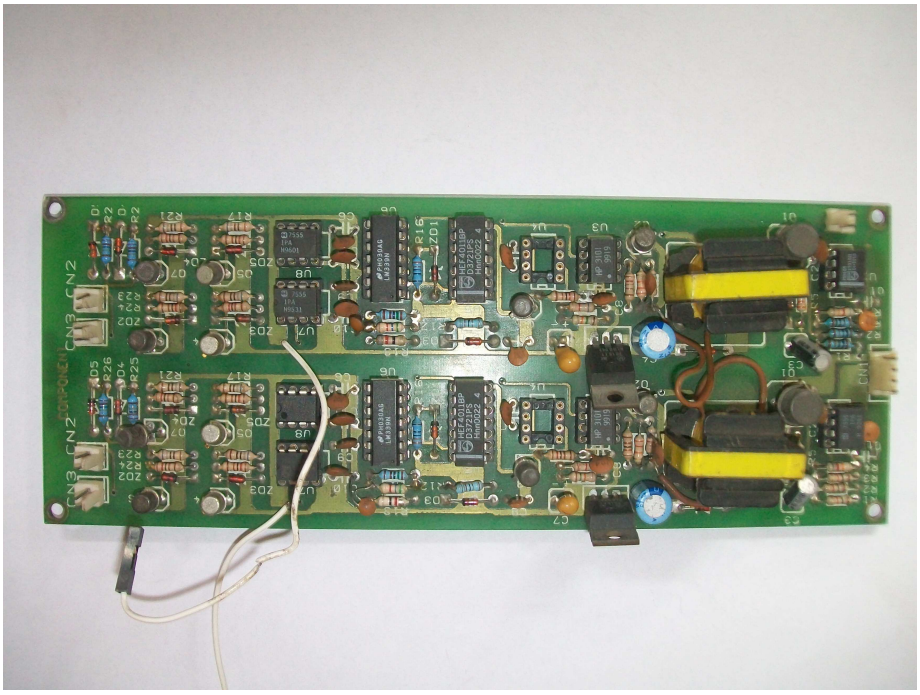

Figure B.13: Gate Drive Card [Courtesy PEG I. I. Sc. Bengaluru]

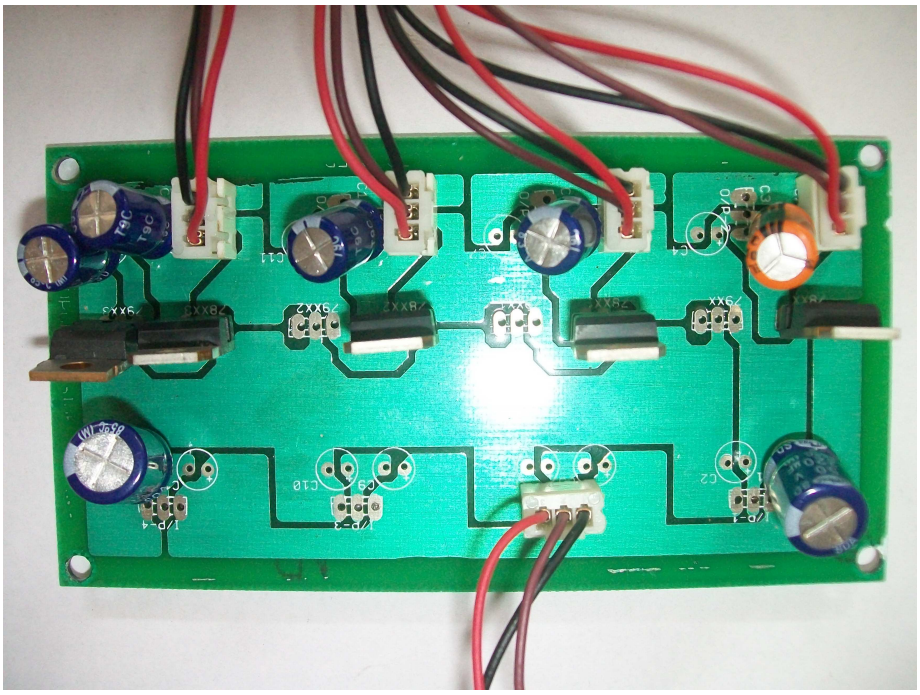

Figure B.14: Power Supply

Appendix C

Experimental setup: Circuits and Pictures

C.1 Passive Filter

C.1.1 Passive Filter: Schematic

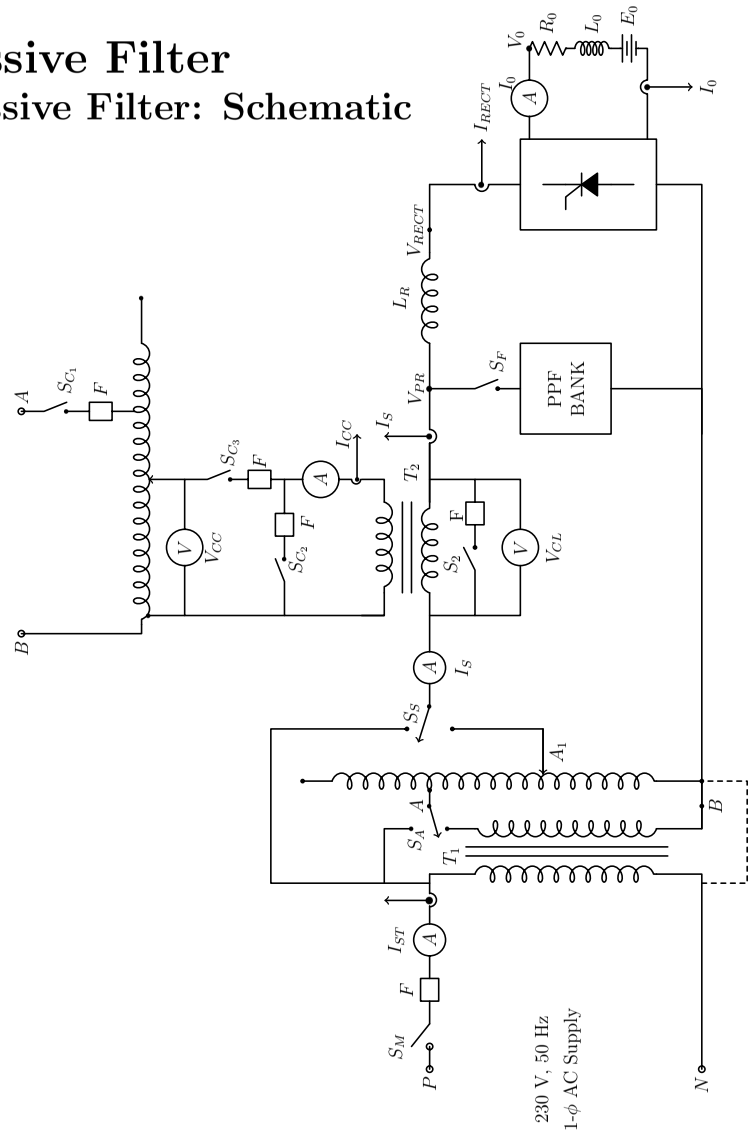

Figure C.1: Circuit Schematic for implementation of the passive filter

C.1.2 Passive Filter: View-1

Figure C.2: View-1 of the passive filter

C.1.3 Passive Filter: View-2

Figure C.3: View-2 of the passive filter

C.2 Inverter Testing

C.2.1 Inverter Testing: Schematic

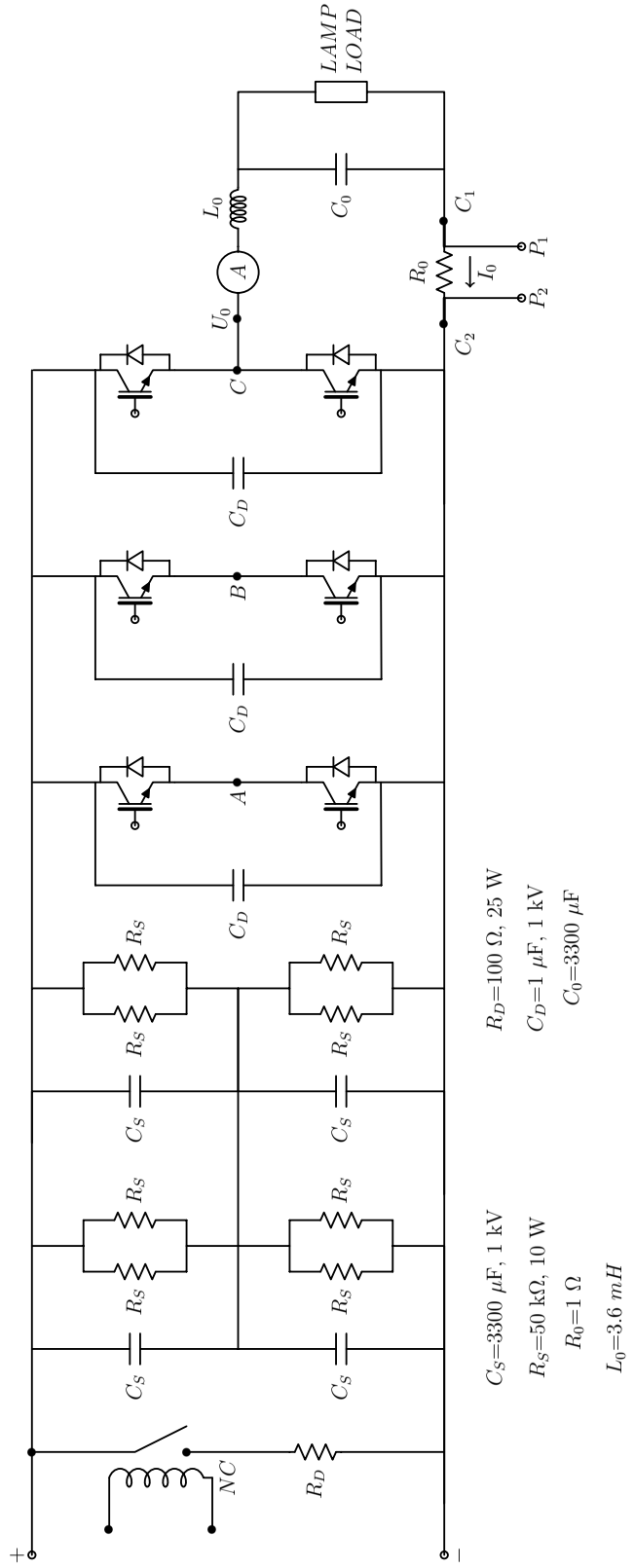

Figure C.4: Circuit Schematic for testing of Inverter module

C.3 Inverter Testing: Experimental setup

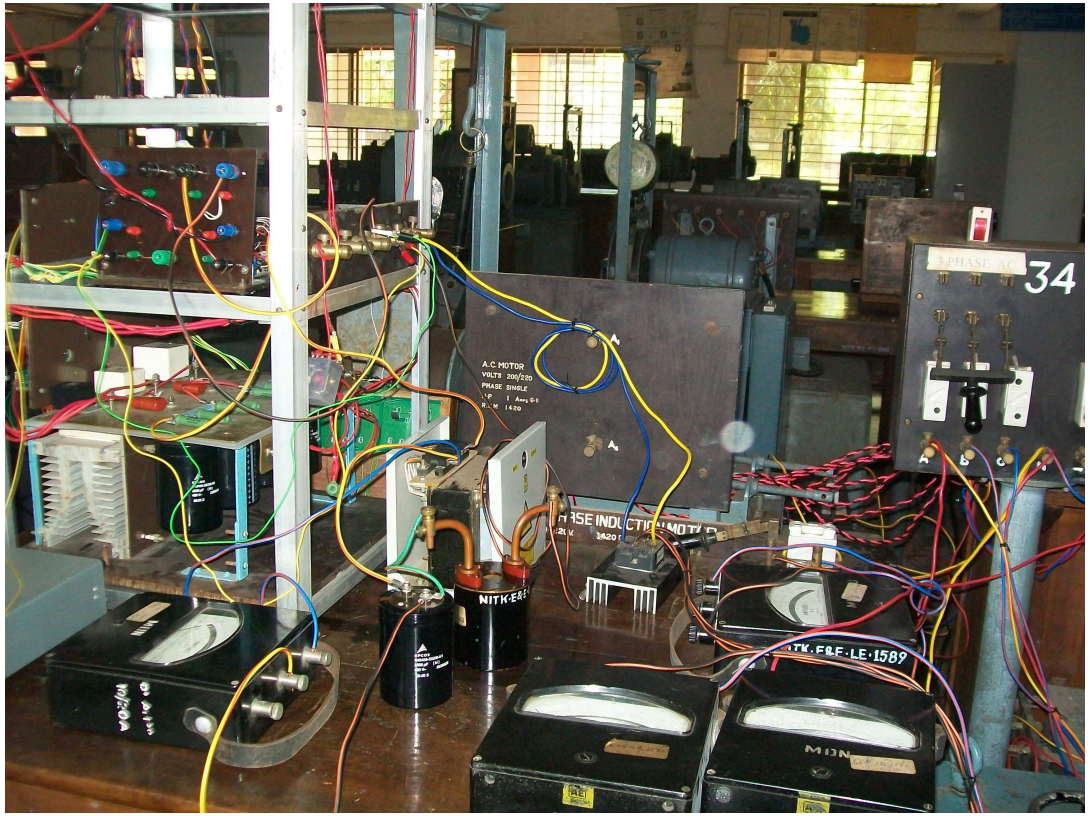

Figure C.5: Experimental setup for Inverter Testing

Appendix D

Determination of System parameters

D.1 DC Machine-Alternator set

D.1.1 Ratings and Specifications

The Specifications and Ratings of the DC machine-Alternator set used for loading the Fully Controlled Single-Phase Rectifier is given in Table D.1.

Table D.1: DC Machine-Alternator Details

DC machine			Synchronous Machine		
Voltage	220	V	Voltage	400	V
Current	51.5	A	Current	12.3	A
Power	10.5	kW	Power	8.5	kVA
			Frequency	50	Hz
Speed	1500	RPM	Speed	1500	RPM
Shunt Field rating	1.6	A	Field rating	1.6	A
	230	V		230	V
			Power factor	0.8	

D.1.2 Measurement of Resistance of the DC Machine Armature with series field

The armature resistance of the DC Motor is measured by passing a constant ripple free current 10 A and measuring the voltage across the armature, while giving a small

movement to the armature to minimize variation due to the effect of brush contact. Several readings are taken and an average value is obtained. It is found that,

R_A	0.44	Ω

D.1.3 Measurement of Inductance of the Armature

The armature inductance is measured by the current build up test for application of a constant voltage. The test is repeated for the case of shunt field winding open and for the case of it kept shorted. A sample current run up curve captured across the $R_R = 1\ \Omega$ standard resistance is shown in Figure D.1.

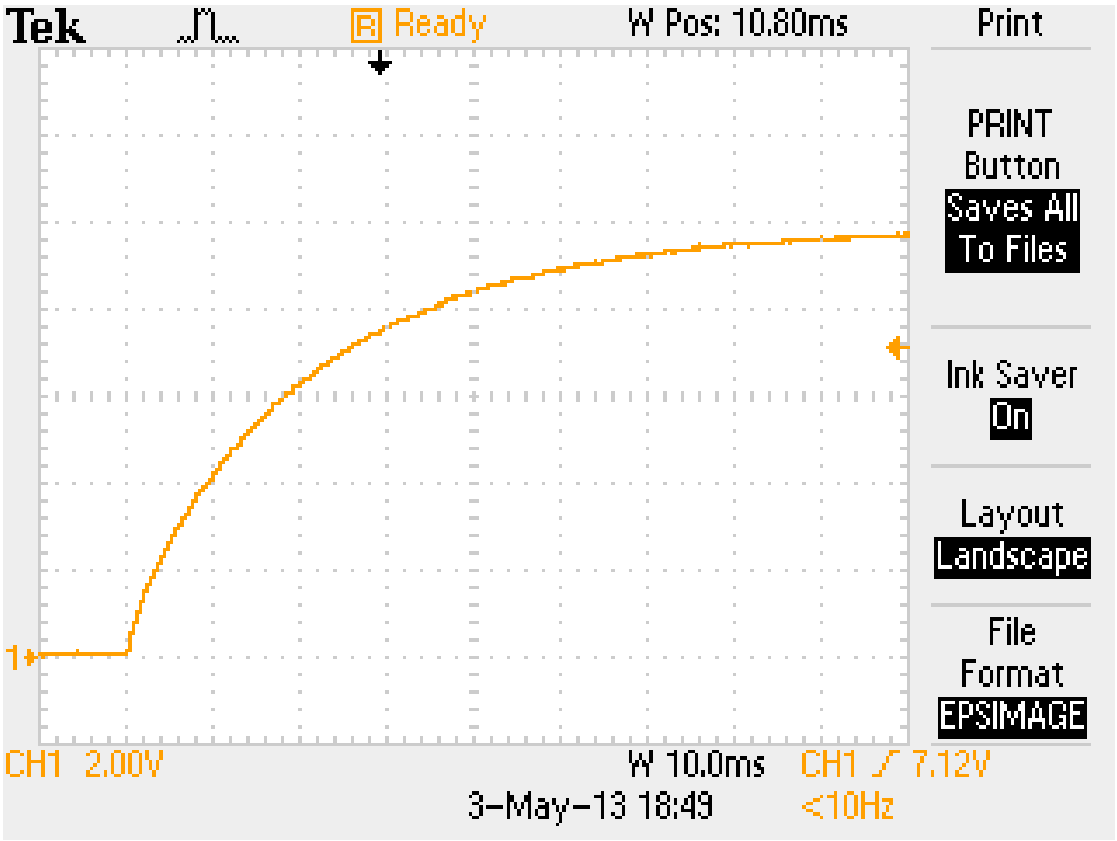

Figure D.1: A sample of the current build-up transient test used to determine the armature inductance of the DC Motor

A slope drawn at a point t_O (the initial portion, in this case) to the exponential build-up (of the current) would intersect the final value at a point t_τ. Then the time constant

of the first order system (armature of the DC motor, in this case) is given by,

$$\tau_A = t_\tau - t_O, \tag{D.1}$$

and is related to the inductance L_A and resistance R_A of the DC motor by,

$$\tau_A = \frac{L_A}{R_R + R_A}. \tag{D.2}$$

The value of τ_A is determined to be,

τ_A	22.5	ms

Then, using D.2, the value of L_A is found to be,

L_A	32.4	mH

D.2 Summary of Utility parameters

The determination/ estimation of the utility parameters is important in such studies as is considered here. However the parameters that can be measured at the PCC will depend upon the circuit conditions – the topology seen into the system from the PCC and the mixture of the loads connected across. The circuit diagram shown in Figure D.2 must serve as an indication of the difficulty involved in the determination of the natural frequencies of the utility system or the equivalent representation of the system seen from PCC. It is a complex problem in system identification and would require a detailed study.

The results that are reported in the literature is related to the Thevenin's equivalent in the form of a $Z_S = R_S + jX_S$, where $X_S = j\omega_s L_s$, a single order series R-L equivalent. But in reality the system is multi-modal and hence this approach is a very gross approximation when harmonics and resonance is to be considered. A survey of the distribution system parameters is carried out to get an estimate of the range of values and is given in Table D.2.

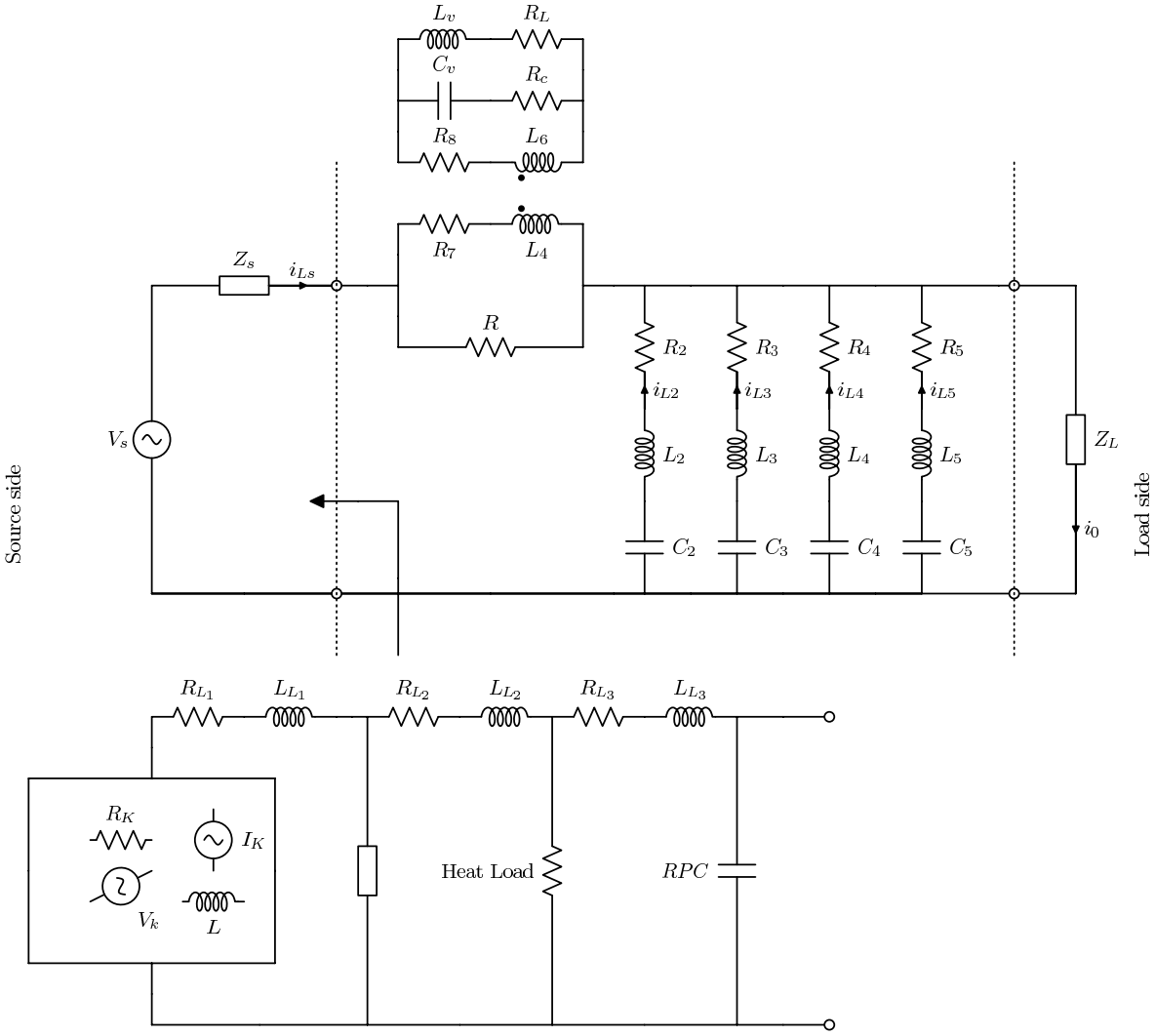

Figure D.2: A representation of the interconnection between the Utility and the load at PCC

Table D.2: A Survey of Distribution System Parameters

Sl. No.	R_S	L_S	$\tau_S = \frac{L_S}{R_S}$	SCR	Voltage drop					References
					IR	IX	IZ	pu	%	
	mΩ	mH	ms	MVA	V	V	V			
1	100	2.000	20		0.707	4.200	4.500	0.0187	1.87	[D.Basic and P.K.Muttik(2000)]
2	250	0.250	01		2.650	0.942	2.833	0.0236	2.36	[Singh *et al.*(2007)]
3	-	0.060							5.20	[Bhattacharya *et al.*(1998)]
4	10	0.150	15		0.106	0.600	0.609	0.0048	0.48	
5	250	2.500	10		1.500	5.655	5.850	0.1463	14.63	[Chandra *et al.*(2000)]
6	-	1.250					0.470	0.0518	0.518	[Bhattacharya *et al.*(1996)]
7	-	2.600					4.500	0.0480	4.800	
8		0.047					12.50	0.0468	4.680	
9	8	0.250	31		0.113	3.487	3.489	0.0092	0.920	
10	0.01	0.250	25				4.455	0.0350	3.500	
The values have the following range										
From	8	0.047	1				0.47		0.479	
To	250	2.6	31				12.5		14.63	

D.3 Determination of Utility parameters

Thus a procedure is envisaged to get an estimate of the system parameters $\overline{Z}_S = R_S + jX_S$ in the laboratory at the PCC where the experimental setup is arranged. It is based on the vector diagram shown in Figure D.3 and the circuit diagram shown in Figure D.4. The open circuit voltage V_O and the voltage V_L across a resistive lamp load at a nominal load current I_L are measured.

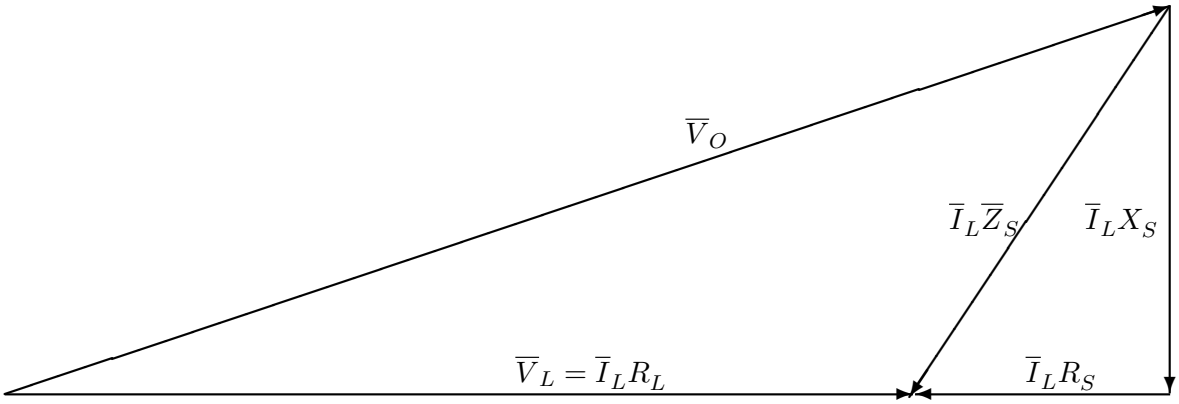

Figure D.3: Vector Diagram relating various quantities at the Utility PCC

From the vector diagram the following relations can be obtained. An assumption is made on the type of the conductor used which determines the relation between the resistance (R_S) and reactance (X_S) at the nominal frequency, like $X_S = \beta R_S$. For a Rabbit conductor $\beta = 0.56$ [Ramamurthy(2009)].

$$R_L = \frac{V_L}{I_L} \tag{D.3}$$

$$\overline{Z}_S = R_S + jX_S \tag{D.4}$$

$$\overline{Z}_T = \frac{\overline{V}_O}{\overline{I}_L} \tag{D.5}$$

$$= (R_L + R_S) + jX_S \tag{D.6}$$

$$|Z_T|^2 = (R_L + R_S)^2 + X_S^2 \qquad \text{or} \tag{D.7}$$

$$R_S = \frac{-R_L + \sqrt{R_L^2 + (1+\beta^2)(|Z_T|^2 - R_L^2)}}{(1+\beta^2)} \tag{D.8}$$

$$X_S = \beta R_S \tag{D.9}$$

Several measurements are taken spread over several days and at different times of the day. The test results and calculations are given in Table D.3

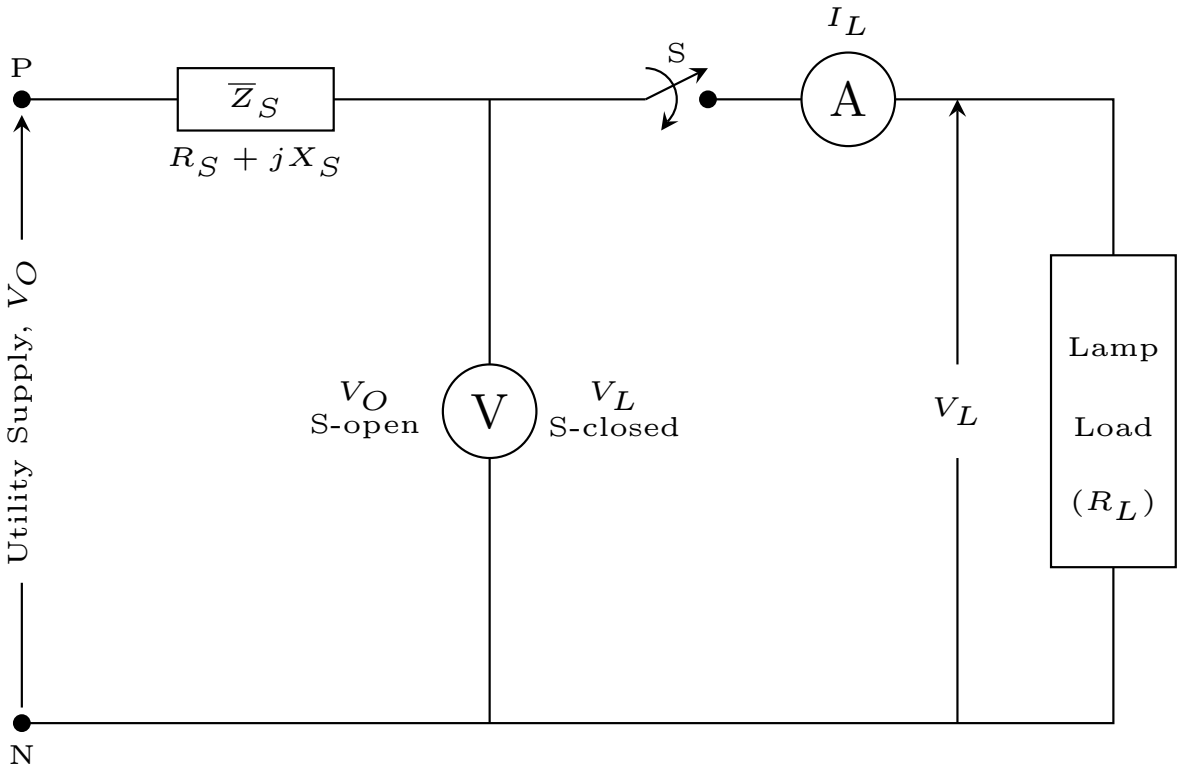

Figure D.4: Schematic for the measurement of power supply circuit parameters

Summary

A value of $R_S = 330$ mΩ and $L_S = 711$ μH is used in the simulation, as a representative value.

Table D.3: A Test Report of Distribution System Parameters

Sl. No.	Date	Time	V_O	V_L	I_L	Z_T	R_L	R_S	X_s	L_S	τ	Z_S	I_{SC}	SCC	SCR	I_{Zs}	pu	%
	2013	Hrs.	V	V	A	Ω	Ω	Ω	Ω	mH	ms	Ω	A	A	kVA	Ω	pu	
1	11-02	10:14	221.25	217.5	9.9	22.348	21.290	0.378	0.212	674	1.783	0.433	511	113	4.52	4.29	0.019	1.864
2	11-02	10:29	222.5	220	9.9	22.475	22.222	0.252	0.141	450	1.783	0.289	770	171	6.85	2.86	0.012	1.244
3	11-02	10:42	223	218	9.5	23.474	22.947	0.524	0.294	935	1.783	0.601	371	83	3.31	5.71	0.025	2.483
4	13-02	14:10	224	220	10	22.400	22.000	0.399	0.223	711	1.783	0.457	490	110	4.39	4.57	0.020	1.988
5	13-02	14:30	222	217	10	22.200	21.700	0.498	0.279	889	1.783	0.571	389	86	3.47	5.71	0.025	2.483
6	13-02	15:30	220	218	8.4	26.190	25.952	0.238	0.133	424	1.783	0.272	807	178	7.10	2.29	0.010	0.995
7	13-02	15:50	224	220	8.5	26.353	25.882	0.469	0.263	837	1.783	0.538	416	93	3.73	4.57	0.020	1.988
8	13-02	16:00	226	222	8.5	26.588	26.118	0.469	0.263	837	1.783	0.538	420	95	3.80	4.57	0.020	1.988
9	14-02	12:19	226	224	8.5	26.588	26.353	0.235	0.132	419	1.783	0.269	839	190	7.59	2.29	0.010	0.995
10	14-02	12:22	232	229	8.6	26.977	26.628	0.348	0.195	621	1.783	0.399	581	135	5.40	3.43	0.015	1.492
11	14-02	19:35	222	219	8.37	26.523	26.165	0.358	0.200	638	1.783	0.410	542	120	4.81	3.43	0.015	1.492
12	14-02	14:00	220	216	10.3	21.359	20.971	0.387	0.217	691	1.783	0.444	496	109	4.36	4.57	0.020	1.988
13	15-02	11:30	220	217	10.35	21.256	20.966	0.289	0.162	516	1.783	0.332	664	146	5.84	3.43	0.015	1.492
14	15-02	12:09	218	214	10.3	21.165	20.777	0.387	0.217	691	1.783	0.444	491	107	4.28	4.57	0.020	1.988
15	15-02	12:25	216	212	10.25	21.073	20.683	0.389	0.218	694	1.783	0.446	484	105	4.18	4.57	0.020	1.988
16	15-02	19:35	225	221	10.5	21.429	21.048	0.380	0.213	678	1.783	0.435	517	116	4.65	4.57	0.020	1.988
17	15-02	20:00	228	224	10.5	21.714	21.333	0.380	0.213	678	1.783	0.435	524	119	4.78	4.57	0.020	1.988
18	15-02	22:30	220	216	10.4	21.154	20.769	0.384	0.215	684	1.783	0.440	500	110	4.40	4.57	0.020	1.988
Note: I_{SC} – Short Circuit Current at PCC; SCC – Short Circuit Capacity at PCC; SCR – Short Circuit Ratio at PCC on 25 kVA base																		

Appendix E

Additional Analysis

E.1 Analysis of Pettigrew's scheme

The scheme is a non-linear system and hence the complete analysis is not considered here. It is not possible to obtain expressions/ formulae relating the parameters of the system (G, Q_F, ω_c) to the design parameters. However under the conditions of small signal variations on the amplitude of the fundamental $C_1(t)$ in $x_I(t)$ a linear model is attempted. Consider for a moment that the system is working under steady-state. The input $D = 0.5$, $x_P(t)$ is steady. Now let there be a small change in the amplitude of $C_1(t)$ from C_1^0, by an amount say Δc_1. Now this change will set-up a new transient. The $a_O(t)$ will change, which results in a change in the error $x_E(t)$, driving a change in $u(t)$ until it settles to a value equal to $\dfrac{1}{C_1^0 + \Delta c_1}$.
Now,

$$u(t) = \frac{G}{\boldsymbol{s}} x_E(t). \tag{E.1}$$

$$= \frac{G}{\boldsymbol{s}} \left(d(t) - a_F(t)\right). \tag{E.2}$$

$$= \frac{G}{\boldsymbol{s}} \left(d(t) - F(\boldsymbol{s}) y(t)\right). \tag{E.3}$$

$$= \frac{G}{\boldsymbol{s}} \left(d(t) - F(\boldsymbol{s}) C_1(t) u(t)\right). \tag{E.4}$$

Now applying small signal analysis on (E.4), with disturbance on input $C_1(t)$ and with $d(t) = D$ we get,

$$u(t) + \Delta u(t) \quad = \frac{G}{\boldsymbol{s}}(D - F(\boldsymbol{s})(C_1^0 + \Delta c_1(t))(u^0 + \Delta u(t))). \tag{E.5}$$

On simplification with cancellation of steady-state terms and with C_1^0 and u^O referring to the steady-state values on C_1 and u respectively we get,

$$\Delta u(t) \quad = \quad -Gu^O \frac{F(\boldsymbol{s})}{\boldsymbol{s}} \Delta c_1(t) - GC_1^0 \frac{F(\boldsymbol{s})}{\boldsymbol{s}} \Delta u(t). \tag{E.6}$$

$$\frac{\Delta u(t)}{\Delta c_1(t)} \quad = \quad \frac{-Gu^O \frac{F(\boldsymbol{s})}{\boldsymbol{s}}}{1 + GC_1^0 \frac{F(\boldsymbol{s})}{\boldsymbol{s}}}. \tag{E.7}$$

$$\frac{\Delta u(t)}{\Delta c_1(t)} \quad = \quad \frac{-Gu^O F(\boldsymbol{s})}{\boldsymbol{s} + GC_1^0 F(\boldsymbol{s}).} \tag{E.8}$$

On substitution for $F(\boldsymbol{s})$ from (3.50)

$$\frac{\Delta u(t)}{\Delta c_1(t)} \quad = \quad \frac{-Gu^O \frac{\omega_c^2}{\boldsymbol{s}^2 + \frac{\omega_c}{Q_F}\boldsymbol{s} + \omega_c^2}}{\boldsymbol{s} + GC_1^0 \frac{\omega_c^2}{\boldsymbol{s}^2 + \frac{\omega_c}{Q_F}\boldsymbol{s} + \omega_c^2}}. \tag{E.9}$$

$$= \quad \frac{-Gu^O \omega_c^2}{\boldsymbol{s}^3 + \frac{\omega_c}{Q_F}\boldsymbol{s}^2 + \omega_c^2 \boldsymbol{s} + GC_1^0 \omega_c^2}. \tag{E.10}$$

Thus the response is depending on the parameters of the system G, ω_c, and Q_F and on the initial state recognized by the values C_1^O and u^O. The response for a step change in $\Delta c_1(t) = \Delta c_1$ – a constant, setting $\boldsymbol{s} = 0$ we get,

$$\frac{\Delta u}{\Delta c_1} \quad = \quad -\frac{Gu^O \omega_c^2}{GC_1^0 \omega_c^2} = -\frac{u^O}{C_1^0}. \tag{E.11}$$

Thus the new steady-state will be,

$$
\begin{aligned}
C_1^* &= \frac{1}{u} && \text{(E.12)}\\
&= \frac{1}{u^O + \Delta u} && \text{(E.13)}\\
&= \frac{1}{u^O + (-\frac{u^O}{C_1^0}\Delta c_1)} && \text{(E.14)}\\
&= \frac{C_1^0}{(1 - \frac{\Delta c_1}{C_1^0})} && \text{(E.15)}\\
&= C_1^0(1 + \frac{\Delta c_1}{C_1^0}) = C_1^0 + \Delta c_1 && \text{(E.16)}
\end{aligned}
$$

which matches with the expected result. If the input $\Delta c_1(t) = \Delta c_1 \sin(\omega_m t)$, then the response is obtained as explained in Figure 3.5, as follows,

$$
\Delta u(t) = \frac{-Gu^O\omega_c^2}{|\boldsymbol{s}^3 + \frac{\omega_c}{Q_F}\boldsymbol{s}^2 + \omega_c^2\boldsymbol{s} + GC_1^0\omega_c^2|_{\boldsymbol{s}=j\omega_m}}\Delta c_1 \sin(\omega_m t - \phi_m) \qquad \text{(E.17)}
$$

where ϕ_m is the phase-shift introduced by the denominator term $D(\boldsymbol{s}) = |\boldsymbol{s}^3 + \frac{\omega_c}{Q_F}\boldsymbol{s}^2 + \omega_c^2\boldsymbol{s} + GC_1^0\omega_c^2|$ at $\boldsymbol{s} = j\omega_m$, which can be obtained from,

$$
\begin{aligned}
D(\boldsymbol{s}) &= \boldsymbol{s}^3 + \frac{\omega_c}{Q_F}\boldsymbol{s}^2 + \omega_c^2\boldsymbol{s} + GC_1^0\omega_c^2 && \text{(E.18)}\\
D(\boldsymbol{s})|_{\boldsymbol{s}=j\omega_m} &= (j\omega_m)^3 + \frac{\omega_c}{Q_F}(j\omega_m)^2 + \omega_c^2(j\omega_m) + GC_1^0\omega_c^2 && \text{(E.19)}\\
&= -j\omega_m^3 - \frac{\omega_c}{Q_F}\omega_m^2 + j\omega_c^2\omega_m + GC_1^0\omega_c^2 && \text{(E.20)}\\
&= (GC_1^0\omega_c^2 - \frac{\omega_c}{Q_F}\omega_m^2) + j(\omega_c^2\omega_m - \omega_m^3). && \text{(E.21)}
\end{aligned}
$$

Now, the magnitude and phase of $D(\boldsymbol{s})$, are given by;

$$
|D(\boldsymbol{s})| = \sqrt{(GC_1^0\omega_c^2 - \frac{\omega_c}{Q_F}\omega_m^2)^2 + (\omega_c^2\omega_m - \omega_m^3)^2} \qquad \text{(E.22)}
$$

angle

$$
\phi_m = \tan^{-1}(\frac{(\omega_c^2\omega_m - \omega_m^3)}{(GC_1^0\omega_c^2 - \frac{\omega_c}{Q_F}\omega_m^2)}) \qquad \text{(E.23)}
$$

E.2 Derivation of formula for tuned Passive-Filter Design

The fundamental current through the h^{th} harmonic tuned filters are governed by the relation,

$$\overline{I}_{1h} = \frac{\overline{V}_1}{\overline{X}_{1L_h} + \overline{X}_{1C_h}} \tag{E.24}$$

where a high quality factor (Q_h) is assumed and the subscripts indicate the impedance offered by the h^{th} harmonic tuned filters to the fundamental input. The $\overline{X}_{1L_h} = j\omega_1 L_h$ and $\overline{X}_{1C_h} = \dfrac{1}{j\omega_1 C_h}$. This leads to,

$$\overline{I}_{1h} = \frac{\overline{V_1}}{j\omega_1 L_h + \dfrac{1}{j\omega_1 C_h}} \tag{E.25}$$

$$j\overline{I}_{1h} = \frac{\overline{V_1}}{\omega_1 L_h - \dfrac{1}{\omega_1 C_h}}. \tag{E.26}$$

The reactances of L_h and C_h at the h^{th} harmonic frequencies are related by,

$$h\omega_1 L_h = \frac{1}{h\omega_1 C_h} \tag{E.27}$$

$$\omega_1^2 L_h C_h = \frac{1}{h^2} \tag{E.28}$$

Since the current at fundamental is leading the voltage $\overline{V_1} = V_1\angle 0$ by $\pi/2$ rad, then $\overline{I}_{1h} = jI_{1h}$. Thus we have,

$$-I_{1h} = \frac{V_1}{\omega_1 L_h - \dfrac{1}{\omega_1 C_h}} \tag{E.29}$$

$$= \frac{\omega_1 C_h V_1}{\omega_1^2 L_h C_h - 1} \tag{E.30}$$

Using (E.28),

$$C_h = \frac{I_{1h}}{\omega_1 V_1}\frac{h^2-1}{h^2} \tag{E.31}$$

$$C_h = \frac{1}{\omega_1 V_1}\frac{h^2-1}{h^2} \tag{E.32}$$

where (E.32) is obtained with $I_{1h} = 1$ A for the current study. Knowing V_1, ω_1 and h, C_h may be calculated from (E.32). It may be observed that the dependency of C_h on h diminishes as h increases, C_h is a weak function of h. The desired value of L_h may be calculated from (E.28) as,

$$L_h = \frac{1}{C_h h^2 \omega_1^2}. \tag{E.33}$$

It may be observed that L_h is a strong function of h. Given the quality factor (Q_h) for the inductor L_h, resistance R_h may be calculated as,

$$R_h = \frac{h\omega_1 L_h}{Q_h}. \tag{E.34}$$

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LIST OF PUBLICATIONS BASED ON THE THESIS

Journals:

1. J. M. Gonda, S. David, "Real-time implementation of a novel vector locked-loop for Synchronous extraction of Harmonics in Power Systems", *Vol. 12/2012 - Edition: 1, pp: 87-94, Journal of Electrical Engineering, University Politehnica Timisoara, Romania.* **(SCOPUS indexed)**

   DOI:http://www.jee.ro/covers/editions.php?act=art&art=WE1302803899W4da735bb9dd42

2. J. M. Gonda, S. David, "Real-time implementation of an amplitude-locked loop: a validation on the dSPACE DS1006- based platform", Vol. 21, Issue 3, 2013, pp: 699-713, *TÜBİTAK - Turkish Journal of Electrical Engineering and Computer Sciences*, The Scientific and Technological Research Council of Turkey.

   (SCI and SCOPUS indexed)

   DOI: http://journals.tubitak.gov.tr/elektrik/issues/elk-13-21-3/elk-21-3-6-1104-22.pdf

Conferences:

1. J. M. Gonda, V. A. Adithya, and S. David, "Performance analysis of compensation current extraction techniques for, 3Φ 3-wire shunt active power filter under unbalanced supply," in *Proc. IEEE International Conference on Power Systems (ICPWS 2009),* IIT-Kharagpur, India, Dec. 2009.

   DOI: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5442679

2. Jora M. Gonda, Ritesh A. Bhat, and Sumam David S., "Adapting Pettigrew's Amplitude-locked loop for Fast and Synchronized Extraction of Fundamental and Harmonics," *In Proceedings of the 2010, Third International Conference on Power Electronics and Intelligent Transportation System (PEITS 2010), Shenzhen, China, during 20-21 November 2010, pp-341-344*, IEEE, ISBN: 978-1-4244-9162-9 (Print).

3. Ritesh A. Bhat, Jora M. Gonda, and Sumam David S., "A Novel Vector-Locked Loop Scheme for Synchronized Extraction of Harmonics," *In Proceedings of*

5th International Conference on Information and Automation for Sustainability (ICIAFS 2010), Colombo, Sri lanka, December 17-19, 2010, pp: 447-452.

DOI: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5715703

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B. E.	K. R. E. C. Surathkal	1986	80.3%	7^{th} Rank
P.U.C. Science	Anjuman Science College, Bhatkal	1982	74.66%	
S.S.L.C.	Janata Vidyala Shirali, Bhatkal	1980	76.66%	

PROFESSIONAL EXPERIENCE

Head	Dept. of E&E	N.I.T.K. Surathkal	02-09-2013	02-09-2015
Assoc. Professor	Dept. of E&E	N.I.T.K. Surathkal	01-01-2006	till date
Asst. Professor	Dept. of E&E	N.I.T.K. Surathkal	31-12-1997	31-12-2005
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Number of publications	Journals	:	2
	Conferences	:	4
Number of projects guided	Undergraduate	:	30
	Graduate	:	21

Area in which Projects Guided: Power Electronics and Drives, Power Systems, Signal Processing.

Industry/ Organisation Interacted: I. I. Sc. Bengaluru; Schneider Electric Bengaluru; Dell India Limited, Bengaluru; Robert Bosch, Bengaluru; I. S. I. Bengaluru; K. M. C. Mangaluru; Texas Instruments (India).

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