

ELECTRICAL STUDIES ON II-VI COMPOUND SEMICONDUCTORS FOR DEVICE APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree

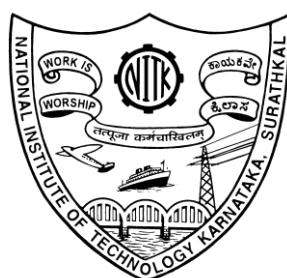
of

DOCTOR OF PHILISOPHY

Submitted

by

SHASHIDHARA



DEPARTMENT OF PHYSICS

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA,

SURATHKAL, MANGALORE – 575025

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DECLARATION

I hereby *declare* that the Research Thesis entitled “**Electrical Studies on II-VI Compound Semiconductors for Device Applications**” which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirements for the award of the Degree of **Doctor of Philosophy in Physics** is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

Mr. Shashidhara

(Reg. No.100626PH10F04)

Department of Physics

Place: NITK, Surathkal

Date:

CERTIFICATE

This is to *certify* that the Research Thesis entitled “**Electrical Studies on II-VI Compound Semiconductors for Device Applications**” submitted by **Shashidhara** (Register Number: **100626PH10F04**) as the record of the research work carried out by him, is accepted as the Research Thesis submission in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

Prof. G. K. Shivakumar
Research Guide

Prof. Kasturi V. Bangera
Research Guide

Chairman-DRPC

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ABSTRACT

II-VI compounds are vital materials for high performance optoelectronic devices such as photovoltaic, light detecting, light emitting diodes and laser diodes in the blue-green to ultraviolet spectral range. The direct band gap ranging over entire visible region and high absorption coefficient of these materials are main features that make them very attractive for such applications. Studies carried out so far on these materials have provided valuable insight into both fundamental and application aspects. In thin film form, these compounds are of interests for optoelectronic applications. However, the improvement in the efficiency of these devices was rather slow, due to the difficulty in doping and lack of control over the defects. These compounds are known to exhibit high electrical resistivity with low intrinsic carrier concentration and low carrier mobility in the thin film form. In addition, the self-compensation effects involving defects restrict the conductivity of the films. An effective utilization of these compound semiconducting thin films can only be possible by improving the carrier density and/or mobility of the carriers. Detailed investigations are needed to achieve these improvements.

In this thesis, an attempt was made to understand the electrical transport properties in some of the technologically important II-VI compound heterojunctions. As a first step, a detailed study including structural, compositional, and electrical characterizations were carried out on CdTe, CdSe, ZnTe, and ZnSe films grown by vacuum evaporation. Further, the effect of substrate temperature on the properties of these compounds was assessed. It was found that as the substrate temperature increased above room temperature, the composition and crystalline quality improved and hence, the electrical conductivity. Among the four compounds studied, CdTe had high resistivity; therefore, more attention was paid to improve its electrical conductivity through doping with indium and by adding excess Te. The CdTe films were further annealed in air and vacuum to study the effect of annealing on electrical properties of the films. Indium doped films showed n type conductivity and tellurium rich films showed p-type conductivity. The CdTe films showed improvement in electrical conductivity with increasing dopant concentration.

Further, four different combinations of heterojunctions (p-CdTe/n-ZnSe, n-CdSe/p-ZnTe, n-CdTe/p-Si, and p-CdTe/n-Si) were fabricated using the condition obtained in the first step. The heterojunctions were evaluated using current-voltage (I-V) and capacitance-voltage (C-V) characterizations. To identify the dominant conduction mechanism in the heterojunctions, I-V curves were fitted to various models. Series resistance and leakage current were found to affect the characteristics of the junctions. Further, C-V measurements showed that the interfaces had large defect density and contributed to the measured capacitance along with space charges.

The results of all the above mentioned studies are presented and analyzed in the present thesis. The doping studies were successful to certain extent, but did not result in drastic improvement in the device characteristics. However, the studies gave a good insight into the behavior of these compounds, which will help in improving the device suitability of the compound semiconductor thin films. Further research is required to improve electrical properties of the films by minimizing the defects, which control the film characteristics, by suitable passivation steps.

CONTENTS

Declaration

Certificate

Acknowledgements

Abstract

Contents i

List of figures v

List of tables ix

Nomenclature xi

Chapter 1 Introduction

1.1 General introduction 1

1.2 II-VI compounds 2

1.3 Background of the work 5

1.4 Scope of the thesis 7

1.5 Objectives 8

1.6 Thesis outline 8

Chapter 2 Experimental techniques

2.1 Thin film preparation 11

2.2 Characterization of thin films 14

2.2.1 X-ray diffraction (XRD) 14

2.2.2 Scanning electron microscopy 15

2.2.3 Optical characterizations of thin films 16

2.2.4 Electrical characterization of thin films 17

2.3 Characterization of heterojunctions 19

Chapter 3 Preparation and characterization of compound thin films

3.1 Introduction 23

3.2 Influence of substrate temperature on growth of II-VI compounds 24

3.3 CdTe thin films 26

3.3.1 Elemental composition 27

3.3.2 Crystal structure 27

3.3.3 Optical properties	29
3.3.4 Electrical properties	29
3.4 CdSe thin films	31
3.4.1 Elemental composition	31
3.4.2 Crystal structure	32
3.4.3 Electrical properties	33
3.5 ZnTe thin films	34
3.5.1 Elemental composition	35
3.5.2 Crystal structure	36
3.5.3 Electrical properties	36
3.6 ZnSe thin films	37
3.6.1 Elemental composition	38
3.6.2 Crystal structure	38
3.6.3 Electrical properties	40
3.7 Discussion	40
3.8 Conclusions	42
Chapter 4 Optimization of CdTe films	
4.1 Post deposition processing	45
4.2 Doping	48
4.2.1 In doped CdTe films	50
4.2.2 Effect of annealing on In doped CdTe	52
4.2.3 Te Doped CdTe	53
4.3 Conclusions	54
Chapter 5 Fabrication and evaluation of heterojunctions	
5.1 Introduction	55
5.2 Fabrications of heterojunctions	56
5.3 Evaluation of heterojunctions	57
5.4 n-ZnSe/p-CdTe heterojunctions	59
5.5 n-CdSe/p-ZnTe heterojunctions	62
5.6 CdTe/Si heterojunctions	68
5.7 Conclusions	81

Chapter 6	Conclusions and scope for further work	
6.1	Introduction	83
6.2	Conclusions	83
6.2.1	Preparation of II-VI compound thin films	83
6.2.2	Processing and doping of CdTe	84
6.2.3	Heterojunctions of II-VI compounds	84
6.3	Scope for the future work	86
References		87
Publications		103
Bio-data		105

LIST OF FIGURES

Fig. 1.1: (a) Wurtzite structure and (b) the zincblende (sphalerite) structure of II-VI compounds

Fig. 2.1: (a) Image of vacuum coating unit used in present work and (b) Schematic diagram of vacuum deposition unit

Fig. 2.2: Schematic of Bragg-Brentano geometry (θ - 2θ)

Fig. 2.3: A typical EDAX plot of a compound in the range of 0-10 keV, Note: there is good separation between Zn K_{α} =8.63 and K_{β} whereas L lines are not so well resolved at Zn L_{α} = 1.012

Fig. 2.4: The contact configuration used for electrical characterizations (a) two-contact and (b) four-contact (Van der Pauw) configurations.

Fig. 2.5: Schematic diagram showing hot probe technique used for determination of conductivity type

Fig. 2.6: Schematic diagram of Hall Effect sample in Van der Pauw configuration

Fig. 2.7: Schematic representation of heterojunction prepared in sandwich structure

Fig. 3.3.1: EDAX spectrum of as grown CdTe thin films deposited at $T_s = 300$ K

Fig. 3.3.2: XRD pattern of as grown CdTe thin films on quartz substrate at room temperature

Fig. 3.3.3: The Tauc plot of CdTe film deposited at $T_s = 300$ K

Fig. 3.3.4: Temperature dependence of resistance for CdTe thin films on quartz substrate at different substrate temperature

Fig. 3.4.1: EDAX spectrum of as grown CdSe thin films deposited at $T_s = 300$ K

Fig. 3.4.2: XRD pattern of as grown CdSe thin films on quartz substrate (a) at room temperature and (b) at 453 K.

Fig. 3.4.3: Temperature dependence of resistance for CdSe thin films deposited at $T_s = 300$ K

Fig. 3.5.1: EDAX spectrum of as grown ZnTe thin films deposited at $T_s = 300$ K

Fig. 3.5.2: XRD pattern of as grown ZnTe thin films deposited at room temperature

Fig. 3.5.3: A representative plot of temperature dependence of resistance for ZnTe thin films deposited at $T_s = 300$ K

Fig. 3.6.1: EDAX spectrum of as grown ZnSe thin films deposited at $T_s = 300$ K

Fig. 3.6.2: XRD pattern of as grown ZnSe thin films on quartz substrate at room temperature

Fig. 3.6.3: A representative plot of temperature dependence of resistance for ZnSe thin films on quartz substrate at $T_s = 473$ K

Fig. 4.1: Variation of resistance as a function of temperature of CdTe thin films annealed (a) in air and (b) vacuum

Fig. 4.2: XRD patterns of CdTe and In doped CdTe

Fig. 4.3: Variation of resistance of In doped CdTe with temperature.

Fig. 5.1: A schematic showing three possible band alignments at hetero-interface

Fig. 5.4.1: (a) I-V characteristic (b) $\ln I$ vs. V and (c) I vs. V^2 curve of n-ZnSe/ p-CdTe heterojunction

Fig. 5.4.2: (a) Junction capacitance and (b) C^{-2} as function of voltage of n-ZnSe/p-CdTe heterojunction

Fig. 5.4.3: Band profile of p-CdTe/n-ZnSe heterojunction

Fig. 5.5.1.: (a) I-V curve of n-CdSe/ p-ZnTe diode (b) the variation of $\ln I$ with voltage, (c) temperature dependence of I-V and (d) Richardson's plot.

Fig. 5.5.2: Forward I-V curve fitted using model given in [Dongaonkar 2014]

Fig. 5.5.3: Variation of junction resistance with bias voltage

Fig. 5.5.4: (a) Plot $\log I$ vs. $\log V$ and (b) variation of current with temperature

Fig. 5.5.5: Junction capacitance of CdSe/ ZnTe heterojunction: (a) C^{-2} as function of voltage, (b) capacitance, (c) differential capacitance as function of frequency and (d) conductance as function angular frequency.

Fig. 5.6.1: Representation of band diagram of (a) n-CdTe/p-Si and (b) p-CdTe/n-Si heterojunctions

Fig. 5.6.2: Schottky-Mott plot of n-CdTe/p-Si heterojunction with different In wt% in n-CdTe

Fig. 5.6.3: Schottky-Mott plot of p-CdTe/n-Si heterojunction with different Te wt% in p-CdTe

Fig. 5.6.4: Mott–Schottky plot of a fictitious device with uniform carrier density N_a . The solid line represents the ideal case in the CV analysis. The dashed line represents the non-ideal case with factors affecting the capacitance at different voltages [Li et al. 2012].

Fig. 5.6.5: Frequency dependency of C-V curve for n-CdTe/p-Si heterojunction with In content (a) 2.5 wt%, (b) 1.875 wt%, (c) 1.25 wt% and (d) 0.625 wt%

Fig. 5.6.6: Frequency dependency of C-V curve for p-CdTe/n-Si heterojunction with Te content (a) 2.5 wt%, (b) 1.875 wt% and (c) 1.25 wt%

Fig. 5.6.7: Capacitance as a function of frequency for (a) n-CdTe/p-Si heterojunctions for different In content and (b) p-CdTe/n-Si heterojunction with different Te content.

Fig. 5.6.8: I-V characteristics of (a) as-deposited and (b) annealed (at 300° C for 2 hours) n-CdTe/p-Si heterojunctions with different In content

Fig. 5.6.9: Series resistance reduction with different In content for annealed (at 300° C for 2 hours) sample of n-CdTe/p-Si heterojunctions

Fig. 5.6.10: Junction resistance as a function of bias voltage for annealed (at 300° C for 2 hours) samples of n-CdTe/p-Si heterojunctions with different In content

Fig. 5.6.11: I-V characteristics of annealed (at 300° C for 2 hours) p-CdTe/n-Si heterojunctions with different Te content

Fig. 5.6.12: Junction resistance as a function of bias voltage for annealed (at 300° C for 2 hours) samples of p-CdTe/n-Si heterojunctions with different Te content

LIST OF TABLES

Table 1.1: The energy band gap, crystal structure, and ionicity of II–VI compound semiconductors

Table 1.2: Some of the parameters of technologically important combination of II-VI forming heterojunction [Fahrenbruch et al. 1974]

Table 3.3.1: Atomic ratio of elemental composition of CdTe films as function of substrate temperature.

Table 3.3.2: Activation energy of CdTe films as function of substrate temperature

Table 3.4.1: Atomic ratio of elemental composition of CdSe films as function of substrate temperature

Table 3.5.1: Atomic ratio of elemental composition of ZnTe films as function of substrate temperature

Table 3.6.1: Atomic ratio of elemental composition of ZnSe films as function of substrate temperature.

Table 4.1: Composition of CdTe annealed at 573 K in air and vacuum for 2 hrs

Table 4.2: Activation energy of CdTe films deposited at different substrate temperature and annealed for 2 hours.

Table 4.3: Resistivity and thermal activation energy of electrical conduction of In doped CdTe

Table 4.4: Effect of annealing on activation energy and carrier concentration of In doped CdTe

Table 4.5: Resistivity and electrical conduction activation energy of excess Te in CdTe

Table 5.5.1.: Extracted diode parameters using equivalent circuit model

Table 5.6.1: Carrier density, built-in potential, and depletion layer width in n-CdTe/p-Si heterojunction for different In wt% (annealed at 300 °C for 2 hours)

Table 5.6.2: Carrier density, built-in potential, and depletion layer width in p-CdTe/n-Si heterojunction for different excess Te wt% (annealed at 300 °C for 2 hours)

NOMENCLATURES

ABBREVIATIONS

Ag	Silver
Cd	Cadmium
CdS	Cadmium Sulfide
CdSe	Cadmium selenide
CdTe	Cadmium Telluride
C-f	Capacitance-frequency
C-V	Capacitance- Voltage
CVD	Chemical vapor deposition
DC	Direct current
EDAX	Energy dispersive analysis of X-rays
FE-SEM	Field Emission Scanning Electron Microscope
Ge	Germanium
HF	Hydro fluoric acid
In	Indium
IR	Infrared
I-V	Current-Voltage
MBE	Molecular beam epitaxy
MOCVD	Metal-organic chemical vapor deposition
n-	n-type
NIR	Near Infrared
p-	p-type
PID	Proportional-integral-derivative controller
PVD	Physical vapor deposition
RCA	Radio Corporation of America
RF	Radio frequency
SCLC	Space charge limited current
Se	Selenium
SEM	Scanning electron microscope

Si	Silicon
Sn	Tin
Te	Tellurium
TED	Thermionic-emission-diffusion model
Te _i	Tellurium interstitials
UV	Ultra violet
V _{Cd}	Cadmium vacancy
Vis	Visible
XRD	X-ray diffraction
Zn	Zinc
ZnSe	Zinc Selenide
ZnTe	Zinc Telluride

SYMBOLS & UNITS

ε	Relative permittivity
ν	frequency
ϕ_b	Barrier height
ΔE_c	Conduction band offset
ΔE_v	Valance band offset
ε_0	Vacuum permittivity
"	Inch
°C	Degree Celsius
2θ	Bragg angle
A	Amperes
Å	Angstrom
A^{**}	Effective Richardson son constant
a, c	Lattice parameters
at%	Atomic percentage
cm	Centimeter
Cu K _α	Characteristic X-Ray emission from electron transition to K shell of Copper

E_a	Activation energy of electrical conduction
E_g	Energy band gap
E_t	Activation energy of traps
eV	Electron volt
h	Planks constant
Hz	Hertz
K	Kelvin
k	Boltzmann constant
L_α	X-ray emission from electron transition to L shell
MHz	Mega Hertz
mV	Millivolt
N_c	Effective density of state in the conduction band
nm	Nanometres
N_t	Trap density
q	Electron charge in coulomb
R	Resistance
R_j	Junction resistance
R_{sh}	Shunt resistance
T	Temperature
T_b	Boiling point
T_m	Melting point
T_s	Substrate temperature
V	Volts
V_b	Built in potential
W	Depletion region width
$wt\%$	Weight percentage
μ	Carrier mobility
μm	Micrometers
σ	Conductivity in Siemens/cm
Ω	Resistance unit ohms
ρ	Resistivity in ohm-cm

CHAPTER 1

INTRODUCTION

1.1 GENERAL INTRODUCTION

A p-n junction is a fundamental building block in most of the electronic devices around us such as light emitting diodes (LED), lasers, solar cells, and integrated chips in computers and mobiles. It either is an interface between two similar materials (homojunctions) or between two dissimilar semiconductors (heterojunctions). The homojunctions contributed to fundamental device concepts and it is the core of many silicon-based devices. The introduction of heterojunction concept in device structure has improved the performance of semiconductor devices tremendously e.g., in heterostructure bipolar transistors [Kroemer 1957, 1982, Dumke et al. 1972]. Further, it led to a wealth of new device concepts and structures such as resonant tunnel diodes [Tsu and Esaki 1973, Chang et al. 1974], double heterostructure lasers [Alferov 2001], superlattice infrared detectors [Smith et al. 1983, Smith and Mailhot 1987], which would not have been achievable with homojunctions. One of the main features of a heterojunction is the discontinuity in energy levels at hetero-interface creating conduction and valence band offsets. The band offset is a critical parameter, which dictates the performance and even feasibility of the device applicability for a given material systems. It gives a new degree of freedom in the device designing and allows one to optimize carrier injection or separation, carrier confinement and barrier height depending on the combination of materials.

The development of many technologies is intimately associated with the availability of suitable materials and ability to produce and manipulate materials to yield specific properties. Advancement in the understanding of the interrelationship between processing, structure, properties, and performance of materials is often the forerunner to the stepwise progression of a technology. In our contemporary era, sophisticated electronic devices rely on many semiconductor materials, which may be elemental (IV group elements) or compound (III-V, II-VI, IV-VI etc.) and most recently organic compounds. Among the semiconductor materials, Si and III-V

compounds such as GaAs are the most used materials in device applications. This is due to the understanding and ability to control their properties gained from the extensive studies carried out. On the other hand, large amount of effort has been focused on II-VI compounds but less success was achieved because of peculiar nature of defects with this class of materials. Thus, to achieve successful device application, one need to understand and surmount the difficulties in these materials or in words of Dr. Sekimoto (eminent Japanese businessperson and scientist) - "*Who dominates materials dominates technology*". This thesis explores some of the II-VI compounds, namely CdTe, CdSe, ZnTe, and ZnSe, for device applicability through electrical studies.

1. 2 II-VI COMPOUNDS

Binary compounds of group IIB and group VIA elements are commonly referred to as II-VI compounds. Except for telluride and selenide of mercury, all other compounds possess a direct band gap, which makes them highly efficient materials for optoelectronic applications. The energy band gaps of these compounds are spanned over entire range of visible spectrum, from infrared (1.45 eV for CdTe) to ultraviolet (3.66 eV for ZnS). The lattice parameter and energy band gap of these compounds are listed in Table 1.1. The binary compounds are highly miscible into one another, so that nearly any desired value of band gap or other property can be achieved through alloying [Adachi 2009]. Hence, they have a potential for a variety of applications especially in the areas of light emitting and light detecting devices, photovoltaic conversion, x-ray and gamma ray detection, etc.

Almost all the II-VI compounds crystallize in such a way that each atom of one element is located at the centre of a regular tetrahedron, the apices of which are occupied by atoms of the other element. The two possible structures can be formed from such tetrahedral: the sphalerite (cubic-zincblende) and wurtzite (hexagonal) type as shown in Fig. 1.1. In sphalerite structure, the atoms of one element are located at the sites of an FCC lattice, while the atoms of the second element occupy centre of four out of eight small cubes. Both these structures have coordination number of four for each atom and both differ only in stacking of atoms. In sphalerite, atoms stack one

above other, taking lattice sites “a-b-c-a-b-c-” whereas in wurtzite it is “a-b-a-b-” staking.

Table 1.1: The energy band gap, crystal structure, and ionicity of II–VI compound semiconductors

Compound	E_g (eV)	Structure	Lattice parameter (\AA)	Phillips's ionicity f_i
ZnO	3.44	Wurtzite	$a = 3.25, c = 5.21$	0.616
ZnS	3.91,	Wurtzite,	$a = 3.82, c = 6.26$	0.623
	3.84	Zincblende	$a = 5.41$	
CdS	2.58	Wurtzite	$a = 4.14$	0.685
HgS	2.10	Zincblende*	$a = 5.86$	0.790
ZnSe	2.80	Zincblende	$a = 5.67$	0.630
CdSe	1.84	Wurtzite	$a = 4.29, c = 7.01$	0.699
HgSe	-0.1	Zincblende	$a = 6.09$	0.680
ZnTe	2.39	Zincblende	$a = 6.10$	0.609
CdTe	1.60	Zincblende	$a = 6.48$	0.717
HgTe	-0.1	Zincblende	$a = 6.45$	0.650

*metastable phase

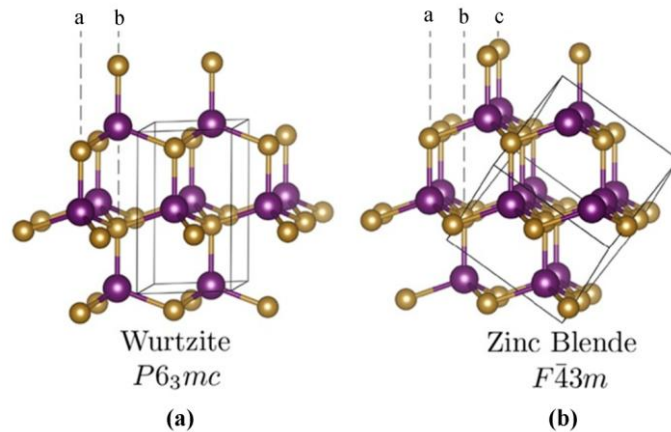


Fig. 1.1: (a) Wurtzite structure and (b) the zincblende (sphalerite) structure of II-VI compounds

In these tetrahedral coordinated II-VI compounds, the bonding takes place by sp^3 hybridization as in pure covalently bonded elemental semiconductors [Christensen et al. 1987]. However, the chemical bonding in these compounds is partly ionic and

partly covalent. This is due to high ionization energy of the metals (II group atoms) and hence does not give up electron but share them with neighboring non-metals (VI group atoms). Since, the non-metals in II-VI compounds have strong electronegativity than metal atoms; the electron cloud between atoms participating in the bonding is pulled towards non-metals and away from metals. Whereas, in case of metal atoms with strong electropositive nature, it donates two outer *s* orbital electrons to non-metal atom that fills outer *p* shell and that makes both atoms doubly charged. Such materials will have pure ionic bonds with octahedral coordinates and Phillips's ionicity value will be more than 0.9. The upper limit for tetrahedral coordination in Phillips's ionicity scale is 0.785, which is threshold for octahedral coordination [Christensen et al. 1987]. It can be noted in Table 1.1, that except for HgS all other compound has ionicity value lower than 0.785.

The electrical properties in these compounds are governed by defects. Due to ionic nature, the defects are electrically active in these compounds and type of conductivity is associated with departure of composition from the stoichiometry. CdSe, ZnSe, ZnS, and CdS exhibit only n-type conduction, while ZnTe has only p-type conduction. CdTe is the only compound which can be easily doped to have both n and p type conduction. The consideration of relative atomic size of metallic and non-metallic component indicate that if metallic component is larger, the compound will have n-type conduction, whereas if non-metallic component is larger in size then p-type conduction is favored [Desnica 1998]. In addition, these materials are well known to have typical behavior such as self-compensation, which hinders efficient doping in these materials. However, the rich optical properties in visible region such as direct band gap and high absorption coefficients make these compounds interesting candidates for optoelectronic applications.

Wide variety of growth methods were employed to grow samples of II-VI compounds ranging from high quality single crystal to poly crystalline thin films to study different aspects of these materials. The different crystal growth methods include vapor phase single crystal growth, melt growth, etc. [Piper and Polich 1961, Ray 1969]. The employed thin film growth methods are molecular beam epitaxy (MBE) [Smith and Pickhardt 1975, Million 1986], metal-organic chemical vapor

deposition (MOCVD) [Dean 1984], metal-organic vapor phase epitaxy [Mullin et al. 1985 Bhargava 1988], hot wall method [Lopez-Otero 1978, Humenberger et al. 1982], close spaced vapor transport [Zapata-Torres et al. 2000, Hu et al. 2007], vacuum evaporation [Sebastian 1992, Romeo et al. 2000, Rusu and Rusu 2000, Rao et al. 2009], etc. The thin film form of the compounds is of significant interest in solar cell and photoconducting device applications due to high absorption coefficient, minority charge-carrier lifetime, and hence requires less quantity of material. In addition, due to variations in the deposition process, a range of unusual properties such as size effects (including quantum size effects), crystalline orientation, and multilayer aspects can be obtained which are not possible with bulk materials. Further, vacuum evaporation is of interest owing to low temperature processing compared to most of the above mentioned methods, and hence the possibility of using flexible substrate and reduces cost without compromising the quality of the films [Heisler et al. 2013, Kranz et al. 2013].

1.3 BACKGROUND OF THE WORK

II-VI compounds and their role as semiconductors have a long evolutionary history. There exist a vast literature concerning the abundant practical experience and valuable device technologies that have emerged in the development of these compounds. Excellent reviews on the topic edited by Ray [1969] and Jain [1993] provide knowledgebase to understand materials science of these compounds and their technological development. Triboulet and Siffert [2010] provided extensive review regarding the technological development, physics of defects and nanostructure of CdTe and related compounds.

II-VI compounds have been extensively exploited for photovoltaic applications. Fahrenbruch [1977] and Chu and Chu [1995] have compiled reviews on different combination of II-VI compound heterojunctions and their photovoltaic conversion properties. Among II-VI compounds, CdTe is the most suitable material for absorber role as it has near optimum band gap for highest efficiency photovoltaic conversion. The reviews also list out other requirements for efficient energy conversion in heterojunction devices. They are,

- (i) Large band gap difference of two compounds forming the junction for transmission of wider spectrum of light
- (ii) Small lattice mismatch and less difference in linear thermal expansion coefficient to minimize density of interfacial recombination states,
- (iii) Minimum electron affinity difference between two components to avoid band spike, which may interfere in photo generated charge transport.

The optoelectronic application relevant values derived from those reviews are given in Table 1.2.

Table 1.2: Some of the parameters of technologically important combination of II-VI forming heterojunction [Fahrenbruch et al. 1974]

Heterojunctions	Smaller band gap (eV)	ΔE_g (eV)	Carrier injected	Lattice mismatch (%)	Energy spike (eV)
n-ZnSe/p-CdTe	1.44	1.23	electron	12.5	0.19
n-CdSe/p-ZnTe	1.70	0.56	electron	0.5	none
n-CdS/p-CdTe	1.44	0.98	hole	9.7	none
n-CdTe/p-ZnTe	1.44	0.82	hole	5.8	0.04

The most efficient CdTe solar cell with CdS as window layer is limited by optical loss at window layer [Mohamed 2013]. Consequently, replacing a CdS layer with wider band gap materials as the window layer is expected to enhance the efficiency of PV cells [Aranovich et al. 1978, Potlog et al. 2011, Spalatu et al. 2011]. Hence, p-CdTe/n-ZnSe should have higher theoretical conversion efficiency. On the other hand, a couple of simulation works suggest that CdSe/ZnTe junctions can be used in tandem to the high efficiency CdTe or copper indium gallium diselenide (CIGS) cells [Mahawela et al. 2005, Xiao et al. 2010]. This may further extend the efficiency of CdTe cells. The efficiency of the devices based on II-VI compounds particularly in CdTe is mainly affected by its poor conductivity. This is due to carrier concentration reduced by compensation and recombination centres.

The band offset or barrier height at interface is a very important parameter in heterojunctions. There are many empirical methods to predict the offset at the interface, for example, electron affinity rule, common anion rule, Harrison atomic orbital model etc. The electron affinity rule developed by Anderson [1962] is one of the first and most widely used method as it is simple to apply; it is based on electron affinity difference of the materials forming junction. However, most of the theoretical predictions on the band offsets are not reliable in most of the practical situations and hence, the band offset values must be determined by experimental methods. Many methods have been developed to experimentally measure the band offset such as x-ray photoelectron spectroscopy [Yu et al. 1991], photoemission spectroscopy [Nelson 1995], electrical transport measurements [Morris et al. 1993], capacitance-voltage measurements [Kroemer et al. 1980], etc. Among these techniques, electrical transport measurements and capacitance-voltage are simple to set up.

The current transport across the interface in heterojunction may be controlled by many mechanisms depending on the device structure and geometry. A number of models to explain conduction mechanism have been developed like Schottky's diffusion model, Bethe's thermionic emission model, combination of both thermionic emission-diffusion model [Chang 1965, Crowell and Sze 1966], etc. The analysis of transport measurements using these models are useful tools to assess the junction quality [McMahon et al. 2005, Macabebe et al. 2008, Hu et al. 2009].

1.4 SCOPE OF THE THESIS

The thesis mainly focuses on the evaluation of heterojunctions formed from II-VI compounds through electrical characterizations. In order to understand the final device performance, thin films of the compounds have to be studied thoroughly correlating the structural and compositional properties with the electrical properties. The electrical properties are severely affected by the defects created because of the deviation in stoichiometry. In case of excess metal atoms, donor type of defects arise that may be either from vacancy of non-metal atoms or interstitials of metal atoms. Similarly, acceptor types of defects are formed when non-metal components are excess in the film. It is very difficult to differentiate between types of defect that act

as donor or acceptors, in particular. Therefore, in this thesis, the observed electrical properties of the films are correlated with the excess or deficiency of one of the component forming II-VI compound. The composition in these compounds can be controlled by substrate temperature and hence, its effect on electrical properties studied. Using the parameters obtained from initial studies on individual compound films, the heterojunctions of the films are formed, and evaluated for device applications.

1.5 OBJECTIVES

1. To grow II-VI compound thin films i.e. CdTe, CdSe, ZnTe, and ZnSe
2. To investigate the effect of growth parameters on compound thin films grown on different substrates by PVD method
3. To study the effect of post deposition heat treatment on the films
4. To evaluate the films by optical and electrical characterizations for solar photovoltaic and photo detector applications
5. To form heterojunctions with these compounds
6. To evaluate junction parameters by current-voltage and capacitance-voltage measurements at different temperatures under dark and illuminated conditions

1.6 THESIS OUTLINE

The work contained in this thesis is concerned with various topics including growth, processing, and characterization of thin films of II-VI compounds and heterojunction involving these compounds. It is divided into chapters based on topics as follows.

Chapter 1 gives a brief overview of II-VI compounds for possible applications. It also includes scope and objectives of the thesis followed by a summary of all the chapters.

Chapter 2 describes the experimental techniques used in present work giving details of deposition technique used for growing thin films of II-VI compounds and for fabrication of heterojunctions, post deposition heat treatment conditions used, and the characterization techniques used to analyze the structure and elemental compositions. Further, it also gives the details of electrical characterization such as electrical

resistivity, carrier concentration, etc. of the thin films and for evaluating the heterojunctions of these compounds.

Chapter 3 contemplates the growth of CdTe, CdSe, ZnTe, and ZnSe thin films using thermal evaporation technique. The chapter introduces the general feature of the as-grown films of these compounds with emphasis on crystal structure and stoichiometry. Particular attention was paid to the substrate temperature as it plays critical role in controlling stoichiometry and crystallinity of these films. The chapter also considers the electrical properties such as resistivity, conductivity type, and thermal activation energy of dark conductivity correlating the results to the composition and structure of the films.

Chapter 4 considers the post deposition process such as heat treatment and doping of CdTe, in particular. The result of heat treatment on CdTe films were analyzed using composition and electrical characterizations. Further, effect of indium doping and excess tellurium on electrical conductivity of CdTe films was studied. The insights obtained from chapter 3 and 4 were used in the following chapter in order to study device applicability of these compounds.

Chapter 5 describes the electrical properties of n-ZnSe/p-CdTe, n-CdSe/p-ZnTe, p-Si/n-CdTe, and n-Si/p-CdTe heterojunctions. The parameters controlling the carrier transport mechanism in the heterojunction diode were assessed through dark current-voltage characteristics and temperature dependence of reverse saturation current. The defect structures in the bulk as well as at the interfaces were elucidated using admittance and capacitance-voltage characteristics of the junction at different frequencies and bias voltages. The results of current-voltage and capacitance-voltage characteristics were evaluated, as it is crucial to determine the device performance.

Finally, chapter 6 summarizes the inferences obtained from chapter 3 to 5 with concluding remarks and scope for the future work.

CHAPTER 2

EXPERIMENTAL TECHNIQUES

Overview

This chapter describes the experimental techniques used in the present work giving details of deposition technique used for growing thin films of II-VI compounds and for the fabrication of heterojunctions, post deposition heat treatments conditions used, and the characterization techniques used to analyze the structure and elemental compositions. Further, it also gives the details of electrical characterization techniques used for electrical resistivity, carrier concentration measurements of the thin films and for evaluating the heterojunctions of these compounds.

2.1 THIN FILM PREPARATION

Most of the electronic and optical applications of the semiconductors need to have a finite thickness and that is achieved by growing them atom by atom from one or more source on the surface of the substrate. Wide variety of deposition techniques such as molecular beam epitaxy (MBE), hot wall flash evaporation, close space vapor transport, close space sublimation, sputter deposition, vacuum evaporation, metal-organic chemical vapor deposition (MOCVD), screen print deposition, spray pyrolysis, and electrochemical deposition have been employed to grow thin films of II-VI compounds. Most of these techniques are variants of basic vapor deposition method, which have been developed in efforts to balance the advantage and disadvantage of various approaches based on required film purity, rate of growth, temperature constraints, need of conformal or non-conformal deposition, etc. The high quality films are often epitaxial films grown under conditions of low supersaturation and thermodynamic equilibrium. However, these processes are time consuming, involves high temperature, limited to rather small area, requires sophisticated instrumentations and hence, highly expensive. For applications such as photovoltaic cells or electroluminescent display, one requires thin film depositions on large area substrates. In addition, to reduce the cost of fabrication, it is usually

necessary to work at high supersaturation to achieve higher processing rates at the expense of film quality. Further, in recent years, to reduce the cost of final device and in search of new possible applications, there are extensive studies on the use of flexible substrates, which require reduction of processing temperature [Heisler et al. 2013, Kranz et al. 2013]. Vacuum evaporation is one of the suitable techniques, which in case of II-VI, has lower processing temperatures (below 473 K). In addition, vacuum evaporation has several advantages such as the material to be evaporated boils or sublimates at reduced temperature and reduction of contamination in deposit. Also, due to straight-line path at pressure less than 10^{-4} mbar, it is possible to use shadow mask between source and substrate to obtain sharp pattern on substrate surface. Hence, vacuum evaporation is a simple fabrication method to study various kinds of semiconductor and heterojunction devices without the need of any lithographic technique to define device patterns.

In the present study, a 12” vacuum deposition unit (Hind High Vac Model No.: 12AD) with a glass bell jar (Fig. 2.1) was used for depositing II-VI compounds as well as for fabrication of heterojunctions. The base plate of the vacuum chamber was connected through a manual high vacuum valve to a 4” water cooled oil vapor diffusion pump backed by a double stage rotary pump (with pumping capacity 200 l/min). The system pressure was monitored using a penning and two pirani gauges and minimum base pressure attained was 8×10^{-6} mbar. A separate but similar deposition unit (Hind High Vac Model No.: 12AD) dedicated for metallization was used for metal contact depositions. The vacuum chambers were equipped with PID controlled substrate heater with a chromel-alumel (K type) thermocouple attached to the surfaces of it where the substrates are placed (facing downwards). For each compound material, a separate molybdenum boat (100A) was used. Power to the evaporation source was provided by a thyristor controlled 1 kW (100A, 10V) transformer and current input regulated by a variac control.

CdTe, CdSe, ZnTe, and ZnSe powder of purity 99.999% (Alfa Aesar and Sigma Aldrich) were used as source materials for deposition of their thin films and as well as for heterojunctions. Silver wire of purity 99.999% (Alfa Aesar) was used for metal contact deposition. Quartz substrates were used for growing individual films as well

as to grow CdSe/ZnTe and CdTe/ZnSe heterojunctions. p-Si (1-10 Ω -cm) and n-Si (1-10 Ω -cm) were used as substrates for n-CdTe/p-Si and p-CdTe/n-Si heterojunctions, respectively. The quartz substrates were cleaned by immersing it in acetone, isopropyl alcohol and distilled water for 15 minutes each in an ultrasonic bath. The Si wafers were cleaned using RCA procedure and after that, to remove native oxide layer on Si surface, wafers were dipped for 2 minutes in diluted hydrofluoric acid (HF) with a concentration of 1 % in distilled water. In case of CdTe, the films were doped with different wt% of indium (In), to achieve better conductivity. For this purpose fine powder of In of purity 99.999% (Alfa Aesar) was mixed with CdTe powder.

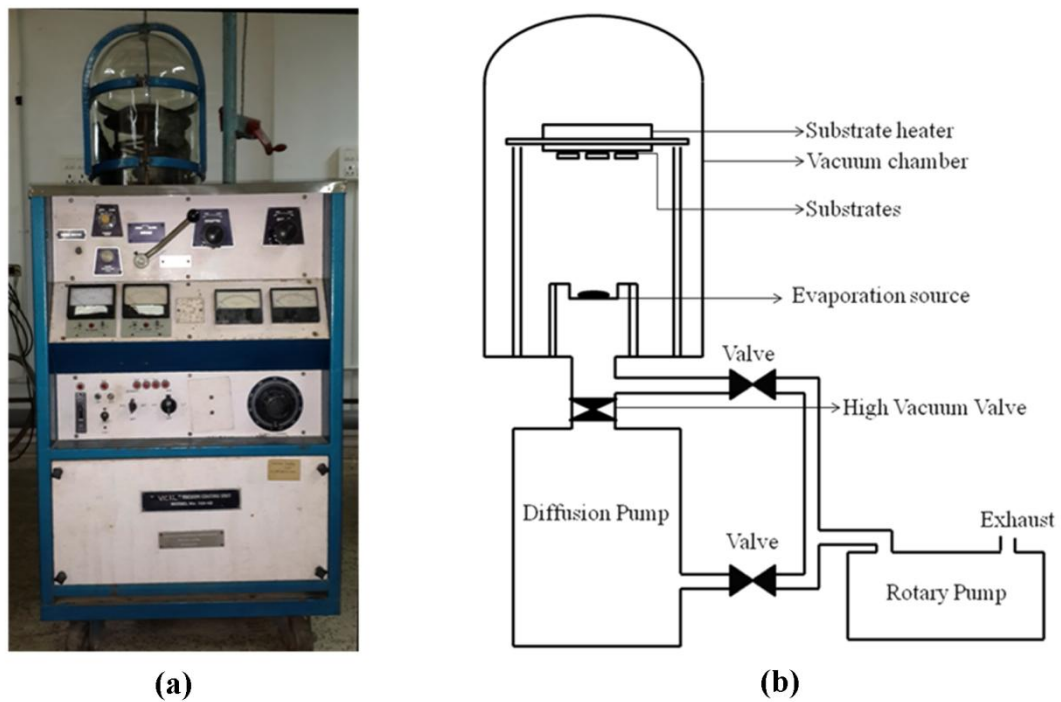


Fig. 2.1: (a) Image of vacuum coating unit used in present work and (b) Schematic diagram of vacuum deposition unit

The deposition condition inside the vacuum chamber was maintained almost same throughout the work except for the substrate temperature. All the possible deposition parameters were set to optimum conditions, as reported in previous works carried out using this deposition system [Rao et al. 2009, 2013]. The vacuum level during the evaporation was in the range of 9×10^{-6} - 2×10^{-5} mbar, deposition rate was maintained ≈ 30 nm/min and source to substrate distance was ≈ 10 cm. However, the substrate

temperature was varied from 300 K to 553 K at a step of 50 K. After the deposition some of the samples were further heat treated in air using PID controlled muffle furnace (dimension 4'× 4'× 9'). In some cases, the samples were annealed in vacuum. For this purpose, they were placed in a vacuum unit equipped with substrate heater.

2.2 CHARACTERIZATION OF THIN FILMS

2.2.1 X-ray diffraction (XRD)

The x-ray reflection from the atomic lattice was used to investigate the crystal structure and crystalline quality of the films deposited at different substrate temperatures. A Rigaku miniflex-600 tabletop X-ray diffractometer was used for this purpose. It has a 600 W Cu-K α characteristic X-ray ($\lambda = 1.54 \text{ \AA}$) generator. The diffractometer working in Bragg-Brentano geometry (θ - 2θ) with vertical goniometer (radius of goniometer circle = 150 mm) shown in Fig 2.2 and consisted of optics such as divergence slit, scattering slit, receiving slit, K β foil filter, monochromator (Graphite), soller slit. The instrumentation has a capability of scanning range from -3 to 145° (2θ) with scanning speed of 0.01-100°/min (2θ) at a minimum step width of 0.005 (2θ). In the present case, a scan rate of 2°/min and 600 W Cu-K α was used as it provided well enough diffracted intensity. The inter planar distance (d) in crystallites of the thin films produces typical diffraction pattern at certain 2θ angles, which is governed by Braggs law $2d \sin \theta = \lambda$. The d values are well documented by Joint Committee on Powder Diffraction Standards-International Center for diffraction Data (JCPDS-ICDD) over the years and they are given in card format. The obtained XRD patterns were matched with these standard data to confirm the crystal structure. The average grain size of the crystals of the polycrystalline films were determined using Scherrer formula ($D=0.9\lambda/\Delta\theta \cdot \cos\theta$), where D is size of the grain in nm, λ is wavelength of x-ray used, $\Delta\theta$ is the FWHM of the intensity peak in radiant and θ is the position of the peak maximum.

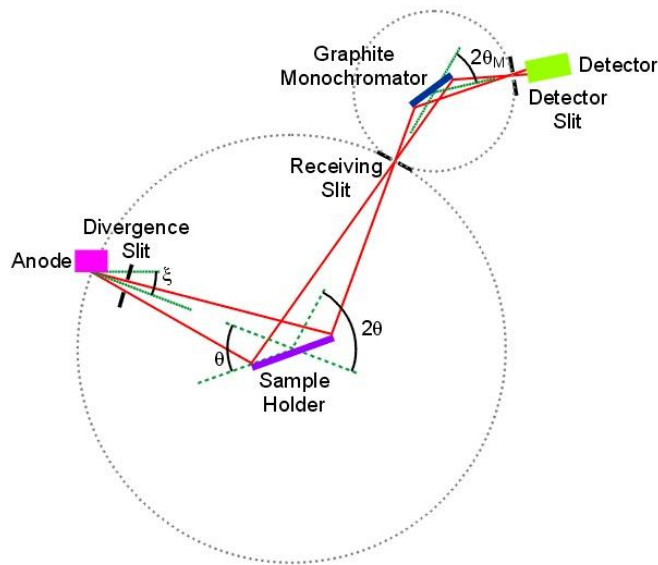


Fig 2.2: Schematic of Bragg-Brentano geometry (θ - 2θ)

2.2.2 Scanning electron microscopy

The surface morphology of the thin films were imaged using secondary electrons detector in either in a JEOL JSM-6380LA scanning electron microscope (SEM) or in a Carl-Zeiss Supra 40VP field emission scanning electron microscope (FE-SEM). The FESEM was capable of 1 nm resolution at 20kVA. A typical accelerating voltage of 10-20 kV was used and a working distance of about 12 mm was maintained. Since, the samples were of high resistance and were deposited on non-conducting substrates, a very thin layer of gold (approximate thickness 5nm) was deposited by dc sputtering. The conductivity from the surface to the conductive sample holder was established with either carbon tape or conductive silver paste.

The elemental compositions of the films were determined using energy dispersive x-ray analysis (EDAX) with a silicon drift detector attached to SEM. The energy of x-ray generated due to the interaction of electron with the material is characteristic of the material that produces it and hence, can be used for identification of elemental composition. However, the quantitative analysis of composition is very complex problem, as analysis often needs calibration. Many factors determine the accuracy as it depends on atomic number of the sample in comparison to the standard, x-ray absorption coefficient and fluorescence factors of the samples. The atomic number

determines the x-ray generation efficiency, the absorption coefficient concerns with reduction in intensity due to absorption with-in the material and higher energy x-ray can excite atoms that emit characteristic x-rays (fluorescence). A typical EDAX plot given in Fig. 2.3 ranges in energy between 0 and 10 keV. This energy range comprises characteristic peaks from K shell for atomic number 4 to 31; L shell peaks for atomic number 22 to 79 and M shell peaks for atomic number 56 onwards. In some cases, it is possible to observe peaks from more than one shell in this 0-10 keV range. In such cases, it is desirable to inspect region between 10 and 20 keV, as higher energy (K shell) peaks are better resolved than the lower energy (L and M) peaks (Fig. 2.3).

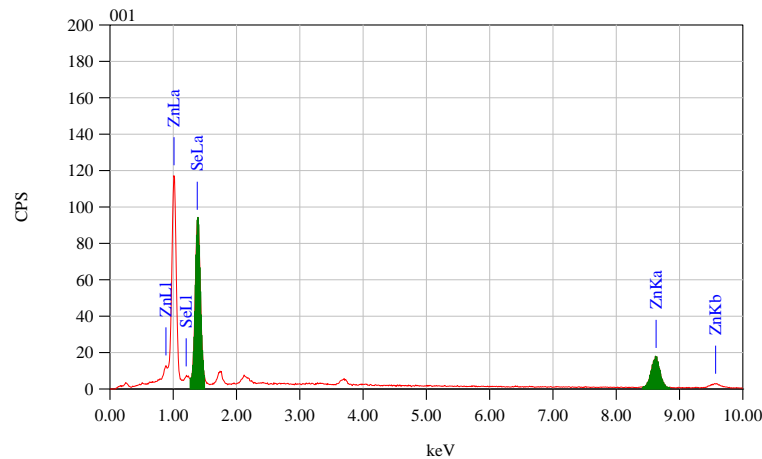


Fig. 2.3: A typical EDAX plot of a compound in the range of 0-10 keV, Note: there is good separation between Zn K_{α} = 8.63 and K_{β} whereas L lines are not so well resolved at Zn L_{α} = 1.012

2.2.3 Optical characterizations of thin films

The transmittance spectra of the thin films were recorded between 500 nm to 2000 nm using a Shimadzu UV 3600 spectrometer. It is one of the simplest methods to determine the band gap of the semiconductor thin films. The energy band gap was determined using Tauc method assuming a direct transition.

2.2.4 Electrical characterization of thin films

Electrical properties such as sheet resistance, resistivity, and carrier concentration of thin films were measured using Keithley 2000 multimeter and Keithley 2400 source-measure unit. For this purpose, the samples of known dimensions with two different contact configurations, i.e. two contact and four contact (Van der pauw) on its surface were used (Fig. 2.4). In two contact configuration, two silver contact pads of $1\text{ cm} \times 1\text{ cm}$ separated by a distance 1 mm were deposited on the surface of thin films of area $2.5\text{ cm} \times 2.5\text{ cm}$ of known thickness. For Van der Pauw configuration, four metal contacts of dimension $1\text{ mm} \times 1\text{ mm}$ were deposited at four corners of sample with $0.5\text{ cm} \times 0.5\text{ cm}$ area.

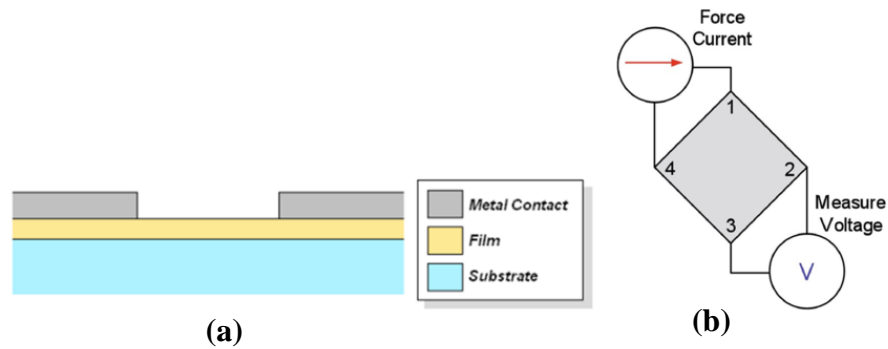


Fig. 2.4: The contact configurations used for electrical characterizations (a) two-contact and (b) four-contact (Van der Pauw)

The contacts in Van der Pauw configuration are numbered in anticlockwise as shown in Fig. 2.4(b). Although this method can be applied at any arbitrary shape, the measurement is simple and straight forward if the sample has a line of symmetry. The resistivity in such symmetrical sample can be determined by allowing current I_{14} through terminal 1 and 4 and measuring voltage V_{23} across terminal 2 and 3. From these I_{14} and V_{23} , one of the two characteristic resistances R_B as demonstrated by Van der Pauw [1958] and similarly, other characteristic resistance R_A can be determined by carrying out measurement in alternative combination terminals i.e., I_{12} and V_{43} . The sheet resistance R_S is related to R_A and R_B as follows,

$$\exp\left(\frac{-\pi R_A}{R_S}\right) + \exp\left(\frac{-\pi R_b}{R_S}\right) = 1 \quad (2.1)$$

Due to symmetry, R_A must be equal to R_B , applying this in Eq. 2.1 and solving it numerically gives R_S . The R_S is related to resistivity as $\rho = R_S t$, where t is thickness of the film.

Even though there are many techniques to determine the conductivity type in the semiconductors, in present case, two of the most common techniques i.e. thermoelectric probe (hot probe) technique and Hall Effect were used. In hot probe method, based on Seebeck effect, the sign of thermo emf generated between hot and cold probe (Fig. 2.5) was used to determine the conductivity type. A soldering gun was used to heat one terminal and other end was at room temperature. The hot end was connected to the positive terminal and cold end to the negative terminal of the voltmeter. Due to thermal gradient, the carriers in the semiconductor diffuse from hot end to cold end causing an opposing potential to develop between two terminals, which can be measured in voltmeter. A positive potential develops for n-type materials and negative for p-type materials.

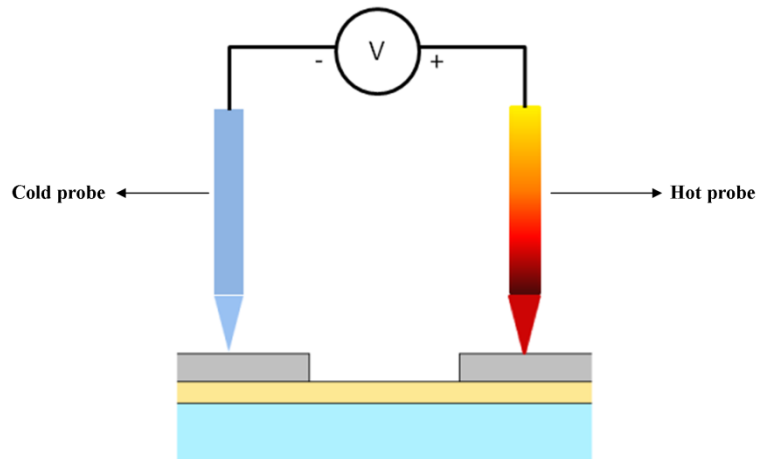


Fig. 2.5: Schematic diagram showing hot probe technique used for determination of conductivity type

The charge carrier type in semiconductor materials can also be determined using Hall Effect by the polarity of the developed Hall voltage. In addition, Hall Effect measurements are widely used to determine the carrier concentration in the samples.

For the Hall Effect measurements of thin film samples, Van der Pauw configuration as shown in Fig. 2.6 was used. The current I_{13} was applied on opposite terminals from 1 through 3 and voltage V_{24} was measured across terminals 2 and 4 (Fig. 2.6) both in presence and absence of the magnetic field perpendicular to sample surface (i.e., to current direction). Using the current and voltage values, the change in resistance ΔR in presence and absence of the magnetic field can be determined, which can be used to calculate Hall coefficient R_H ,

$$R_H = \frac{t}{B} \Delta R \quad (2.2)$$

where t is thickness of the sample and B is the applied magnetic field. The charge carrier concentration can be determined as follows,

$$n = \frac{1}{R_H q} \quad (2.3)$$

where q is electronic charge.

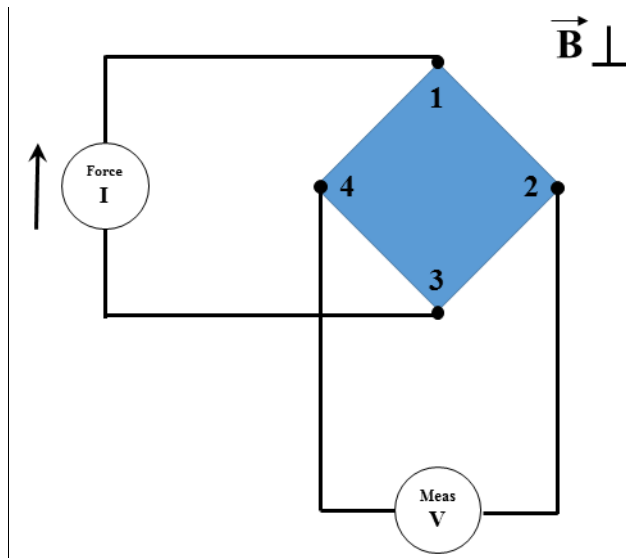


Fig. 2.6: Schematic diagram of Hall Effect sample in Van der Pauw configuration

2.3 CHARACTERIZATION OF HETEROJUNCTIONS

The heterojunctions of CdSe/ZnTe, CdTe/ZnSe, and CdTe/Si were fabricated to study device applicability of these heterojunctions. In order to fabricate the junctions, the semiconductor layers and metal contacts of particular shape or pattern were

deposited through various shadow masks for each layer. The structure of one of the heterojunction fabricated for electrical characterization is shown in Fig. 2.7. Similarly, other heterojunctions were fabricated by replacing CdSe and ZnTe with ZnSe and CdTe, respectively. In both cases, silver was used as contact materials. However, in case of CdTe/Si heterojunctions, aluminum was used as contact for Si, indium as contact material for n-type CdTe and silver for p-type CdTe.

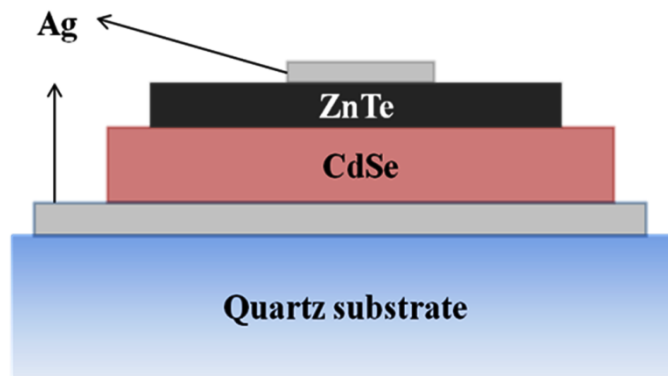


Fig. 2.7: Schematic representation of heterojunction prepared in sandwich structure

The heterojunctions were evaluated by employing current-voltage measurements in dark using Keithley 2400 source-measure unit. The conduction mechanism in heterojunctions can be elucidated by fitting it to suitable diode equations (detailed description is given in chapter 5). In order to determine the barrier height at semiconductor interface, current-voltage was measured at different temperatures varying from 300 K to 373 K in a step of 5 K. Since, in practical devices, series resistance affects the current at high forward bias and parallel (shunt) resistance plays a key role at low forward and reverse bias depending on device preparations. Hence, they are considered in device evaluation.

Depletion region width and barrier height at hetero-interfaces and the apparent carrier density in space charge region (SCR) were determined through capacitance-voltage (C-V) measurements. Assuming the junction to be a plate capacitor with the apparent profiling depth $x = \epsilon_0 \epsilon_r A/C$, where the vacuum permittivity ϵ_0 , the relative permittivity ϵ_r of the material and the area of the junction A, the characteristic parameters of the junctions were extracted at a constant temperature of 300 K. The

junction capacitance measurements of heterojunctions were performed with an Agilent E4980A precision LCR meter at a frequency of 300 kHz with an oscillating voltage of 50mV superimposed on bias voltages. Bias applied to the junction was varied from negative voltage to positive voltage depending on heterojunctions being studied (details in chapter 5).

CHAPTER 3

PREPARATION AND CHARACTERIZATION OF COMPOUND THIN FILMS

Overview

This chapter describes the growth of CdTe, CdSe, ZnTe, and ZnSe thin films using thermal evaporation technique. The chapter introduces the general feature of the as-grown films of these compounds with emphasis on crystal structure and stoichiometry. Effect of substrate temperature on the stoichiometry and crystallinity of these films has been studied. The electrical properties such as resistivity, conductivity type, and thermal activation energy of dark conductivity of these compounds have been determined with respect to the growth conditions.

3.1 INTRODUCTION

The main objective of this chapter is to understand the effect of growth parameter on the properties of four important II-VI compound thin films (i.e., CdTe, CdSe, ZnTe, and ZnSe) grown by thermal evaporation. This is because the properties of the vacuum-deposited films depend on the growth process and it can be tuned to achieve required property for applications. The insight obtained here would be useful to account for the transport mechanism in heterojunctions of these materials evaluated in the chapter 5 of the thesis. Among the many parameters such as evaporation rate, vacuum level, nature, and condition of substrate in vacuum deposition, substrate temperature (T_s), T_s is the most critical parameter determining the structure and properties of the films. In most of the cases, T_s determines the degree of the crystallinity and morphology and hence, in turn many other structure related properties such as charge carrier mobility [Okamoto and Ugai 1973], photoconductivity of vacuum deposited ZnTe [Rao et al. 2010], and ZnSe [Rao et al. 2011].

In addition, T_s also determines the composition of the films if compounds dissociates during evaporation. It has been well understood that II-VI compounds dissociate during evaporation as evidenced by the initial evaporation experiments on

CdS, CdSe and ZnSe [Somorjai and Jepsen 1964a, 1964b, Kirk and Raven 1976]. Due to the difference in volatility of constituent elements of these compounds, the grown films may deviate from stoichiometry. The deviation in composition determines defect density in thin films of the compounds. Owing to the ionic nature of bonding in these compounds, the defects are electrically active. Hence, minor deviation in composition of these compounds can lead to significant effect on their electronic properties [Desnica 1998b]. For instance, earlier studies correlating the growth and electrical properties of ZnSe, CdTe, and CdSe films have shown that as-deposited films had very high resistivity even after doping [Aranovich et al. 1978, Sebastian and Sivaramakrishnan 1990, Sebastian 1992]. They reported that self-compensation from the excess non-metallic component in the films is hindering the efficient doping. Further, it has been shown that annealing in the presence of metallic component vapors or adding excess of metallic component during evaporation can favor effective doping in these films [Aranovich et al. 1978, Belas et al. 2007]. In recent studies, it is being debated whether metallic vacancy is an efficient acceptor in CdTe films or the films should be Cd rich to give better efficiency [Ma et al. 2013, Chin et al. 2015]. In addition, degrees of freedom in crystal structure of these compounds depending on composition and growth conditions can have major effects on properties of the films [Shalimova and Dmitriev 1972]. Hence, to achieve optimum characteristics of the compound thin films, it is very important to understand the effect of deposition conditions on the structure, surface morphology, and optoelectronic properties.

3.2 INFLUENCE OF SUBSTRATE TEMPERATURE ON GROWTH OF II-VI COMPOUNDS

II-VI compounds are of AB type, where A is metallic component and B is non-metallic components. They are known to dissociate in the course of evaporation into their constituent elements i.e., into A and B₂ in vapor phase [Somorjai 1961, Wösten 1961, Wösten and Geers 1962, Goldfinger and Jeunehomme 1963, Höschl and Koňák 1965, Brebrick 1969]. The constituent elements have different volatility and therefore have different vapor pressure [Ignatowicz 1976]. In such cases, the films deviate from the stoichiometry or may have different composition than that of the source materials. The condensation process is complex in presence of two interacting different vapors

phases than that of single-phase vapor. In such cases, the critical value of vapor pressure and growth temperature of compounds for progressive condensation is different from that of individual component. In order to achieve stoichiometric film, the constituent element vapors must arrive and/or adsorbed at proper ratio or need to have similar sticking coefficient and react to form a compound. Otherwise, the film may have either rich or deficient of one component.

Previous experiments have shown that either by controlling the vapor pressure of constituent elements of a compound or by tuning T_s , it is possible to attain required composition [Karl-Georg 1960, Freller and Günther 1982]. In the former case of controlling vapor pressure, at a given constant T_s , constituent elements were taken in separate crucibles and their temperatures are varied to attain suitable vapor pressure near substrate surface. In latter case, at a given vapor pressure, the T_s is varied to tune the sticking coefficient of constituent elements. Similarly, many empirical rules have been put forward in order to relate the structure of the films to substrate temperature. One of them is that developed by Movchan and Demchishin [1969] according to which three structural zones are possible as a function of reduced temperature T_s/T_m , where T_s is the substrate temperature and T_m is melting point of the material being deposited. Each of these zones has its own characteristic structure and physical properties, ranging from tapered crystals with domed tops separated by void boundaries at $T_s/T_m < 0.3$, to columnar grains with dense well-defined boundaries between $(0.3 < T_s/T_m < 0.5)$ and equiaxed grains for $T_s/T_m > 0.5$. Another empirical relation between substrate temperature and boiling point of material being deposited was identified after studying wide range of materials including II-VI materials [Vincett et al. 1977]. According to this, vacuum-deposited films exhibit optimized structure and composition at $T_s \approx 0.3T_b$ (where T_b is normal boiling point of the respective material). This relation was established based on the assumption that two opposing processes, one of which is condensation while other is re-evaporation, which are taking place near growing surface during thin film deposition control optimum T_s . That implies, if T_s/T_b is less than 0.3 then the films may have mixed phases with a fraction of well order crystalline phase of stoichiometric compound and other fraction of disordered non-stoichiometric phase (often excess of one with higher

sticking coefficient). As substrate temperature increased, i.e., T_s/T_b gets closer to 0.3, the disordered phase re-evaporates since it has higher vapor pressure at that temperature in comparison to the compound (stable crystal phase) formed, which has very less vapor pressure above its surface [Montrimas and Petretis 1973, Vincett et al. 1975]. Therefore, these compounds can be deposited in a controlled manner using vacuum evaporation. T_s is perhaps the most critical and easily controllable parameter responsible for determining the structure and properties of vacuum-deposited films.

The following sections describe the structure, composition, electrical properties of the vacuum deposited CdTe, CdSe, ZnTe, and ZnSe films. The properties of the films were studied as a function of substrate temperature by keeping other parameters such as growth rate (30 nm/min), vacuum level (10^{-5} mbar), and distance between source and substrate (10 cm) constant.

3.3 CdTe THIN FILMS

The growth of CdTe thin films has been studied extensively for its application as absorber material in solar cell and for photo-detector applications. A wide variety of deposition techniques have been employed to grow polycrystalline films for solar cell application such as close spaced sublimation [Bonnet 2000], electro-deposition [Basol 1988] rf-sputtering [Shao et al. 1996] and thermal evaporation [Takamoto et al. 1997, Mahesha et al. 2009]. Highly sophisticated deposition techniques were also used to grow single crystal CdTe films for photo-detector applications such as IR [Fiederle et al. 2007, Rogalski 2012] X-ray and gamma ray detector applications [Niraula et al. 2006, Belas et al. 2007]. Except for the rf-sputtering and vacuum evaporation, all other techniques have relatively very high processing temperature and are expensive. Hence, use of vacuum evaporation technique will reduce the cost due to low substrate temperature (around 473 K); also, the possibility of using flexible substrate is an added advantage [Heisler et al. 2013, Kranz et al. 2013].

In this study, CdTe films were deposited on cleaned quartz substrate. The substrates were cleaned with acetone, isopropyl alcohol and distilled water in ultrasonicator. High pure CdTe (99.999%) powder was taken in a molybdenum (Mo) boat and it was evaporated at a residual pressure of 10^{-5} mbar. The crystal structure

and elemental composition of the films deposited at different substrate temperature were studied. The electrical properties such as resistivity and conductivity type of the films were analyzed using silver as ohmic contact.

3.3.1 Elemental composition

The chemical composition of the films was determined using EDAX (Fig 3.3.1) and it revealed that the films deposited at $T_s = 300$ K were Te rich with Cd to Te ratio (in at%) ~ 0.89 . This can be attributed to, as described in section 3.2, the difference in vapor pressure of the constituent elements Cd and Te. The substrate temperature was varied from 373 to 523 K to study its effect on the elemental composition of the CdTe films. It can be noted from the Table 3.3.1 that the stoichiometry improves with increasing substrate temperature and elemental ratio reaches unity as T_s approaches to 523 K. At $T_s = 523$ K, the CdTe compound has much lower vapor pressure in comparison with its constituent elements Cd and Te. Thus, CdTe compounds are stable and continue to grow on the substrate while excess Cd and Te have high vapor pressure and hence, re-evaporate.

3.3.2 Crystal structure

The XRD analysis of the CdTe film grown at $T_s = 300$ K (Fig 3.3.2) revealed that the film was polycrystalline in nature with a strong peak at 23.74° . This peak corresponds to (111) plane of sphalerite phase of CdTe. The CdTe films can grow in stable sphalerite and in metastable wurtzite phases depending on growth conditions and composition. Few of the reported cases [Holt and Abdalla 1975] had both mixed phases. In the XRD pattern of CdTe films, since peaks corresponding to wurtzite phase were not detected, it can be concluded that the films were purely consisting of sphalerite phase. The crystalline quality of the films was found to increase with increasing T_s . As seen in section 3.3.1, with increasing T_s , the elemental constituent which is in excess (also expected to be in amorphous phase), may re-evaporate and lead to an improvement in crystallinity. In addition, increase in T_s increases the surface diffusion leading to larger grains.

Table 3.3.1: Atomic ratio of elemental composition of CdTe films as function of substrate temperature.

Substrate temperature (K)	Atomic ratio (at %)
373	0.89
423	0.92
473	0.96
523	1.00

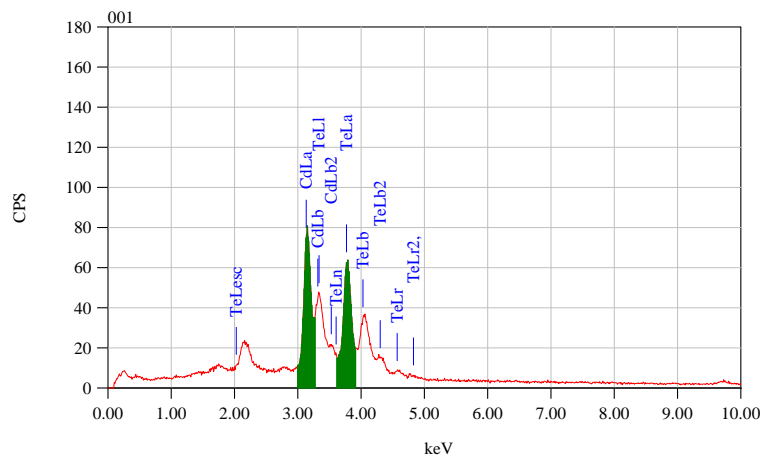


Fig. 3.3.1: EDAX spectrum of as grown CdTe thin films deposited at $T_s = 300$ K

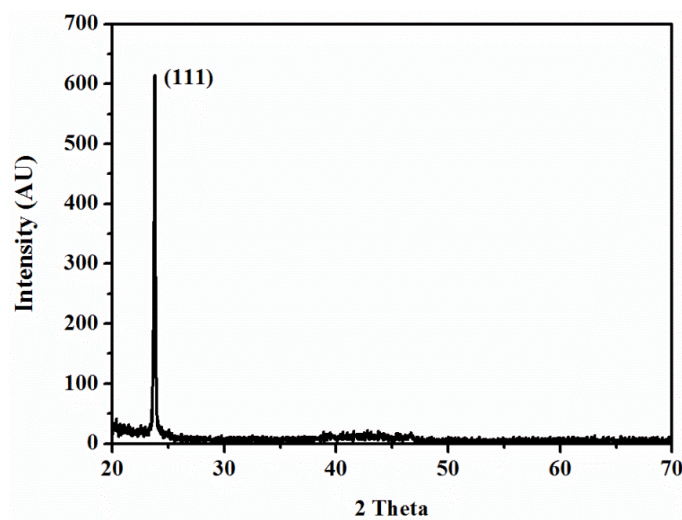


Fig. 3.3.2: XRD pattern of as grown CdTe thin films on quartz substrate at room temperature

3.3.3 Optical properties

Optical properties of the films were studied from transmittance measurements in the Vis-NIR wavelength range from 500 nm to 2000 nm. Assuming the direct transition in CdTe films, the energy band gap of ≈ 1.5 eV was obtained from the tauc plot (Fig. 3.3.3). The energy band gap for the films deposited at different T_s did not vary significantly. The sharp absorption edges confirm the quality of the films.

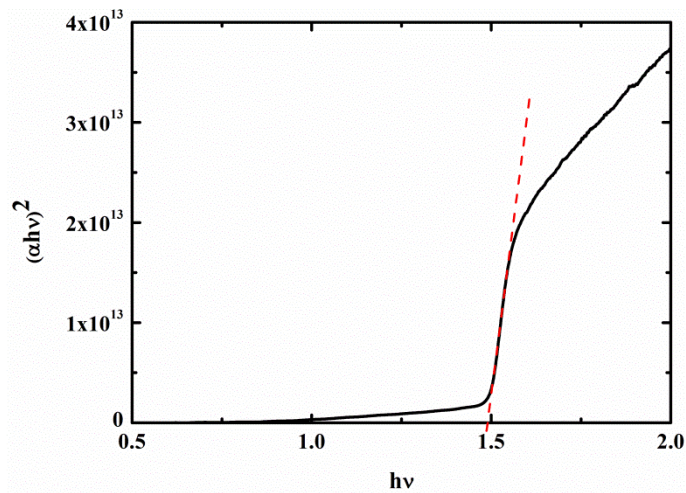


Fig. 3.3.3: The Tauc plot of CdTe film deposited at $T_s = 300$ K

3.3.4 Electrical properties

The electrical properties of CdTe are very sensitive to composition and crystallinity of the films. The majority carrier type in CdTe films deposited at different T_s was determined using hot-probe method. From the polarity of the potential between hot and cold probe, it was determined that the majority carriers in all films were holes. This can be attributed to the composition of the films; films grown at substrate temperature below 523 K were Te rich (section 3.3.1). The films grown at T_s above 523 K are expected to be Cd rich and show n-type conductivity [Dawar et al. 1983, Heisler et al. 2013]. The p-type conductivity in the undoped films arises due to the Cd vacancies, which create acceptor-like impurity level at forbidden gap (at 130-210 meV above the valence maxima) [Wei and Zhang 2002]. Furthermore, in Te rich films, there is a possibility of Te occupying interstitial

position that creates acceptor-type level in forbidden gap (570 meV above the valence maxima).

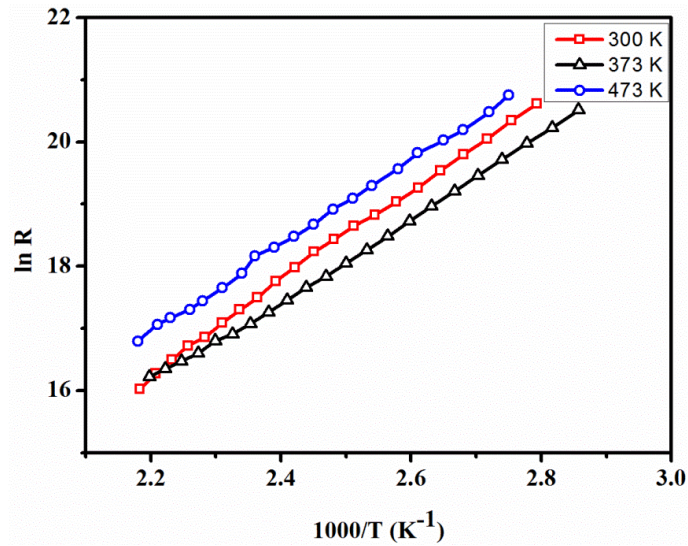


Fig. 3.3.4: Temperature dependence of resistance for CdTe thin films on quartz substrate at different substrate temperature

Table 3.3.2: Activation energy of CdTe films as function of substrate temperature

Substrate temperature (K)	Activation energy (eV)
300	0.66
373	0.56
423	0.66
473	0.59
523	0.77

The electrical resistivity of the films was measured in coplanar configuration with two silver contacts of 1cm x 1cm dimension separated by 1mm distance. All the as-grown films have high electrical resistivity $>10^6 \Omega\text{-cm}$ with corresponding carrier concentration of the order 10^{13} cm^{-3} . The thermal activation energy (Fig. 3.3.4) was determined from temperature dependence of resistivity and it was found to be in the range of 0.56 eV - 0.77 eV for all the films (Table 3.3.2). The reason for such high resistance and activation energy may be the non-stoichiometry that creates self-

compensating defect complexes and related deep trap level in forbidden band gap. In case of stoichiometric films, due to reduction in acceptor like defects the carrier density may have reduced.

3.4 CdSe THIN FILMS

Due to its excellent optoelectronic properties, the growth CdSe thin films and nano structure films have been studied for photo-detector [Pejova et al. 2003] and photovoltaic [Mahawela et al. 2005, Xiao et al. 2010] applications. The vapor pressure studies over CdSe during evaporation has shown that it dissociates in to Cd and Se₂ [Wösten 1961] and Se₂ has higher vapor pressure. Hence, the condensed phase on substrate surface is non-stoichiometric. The CdSe films deposited on a substrate at room temperature found to have Se inclusions [Shreekanthan et al. 2003]. These Se inclusions in CdSe films affect the electrical conductivity of the films. Two possible reasons for the high resistivity of such films may be the amorphous phase of Se hindering the transport and self-compensation from donor-acceptor like defects [Tubota 1963]. As described above, the composition of II-VI compound can be controlled by tuning the T_s. Also, due to the difficulties in doping p-type of CdSe and possibility of excellent lattice matched type-II heterojunction with p-ZnTe [Phillips et al. 1992, Yu et al. 1992, Wang et al. 1993], it is necessary for CdSe thin films to have good n-type conductivity.

Therefore, in this study growth of vacuum evaporated CdSe films with emphasis to the effect of T_s on its properties was analyzed. Under similar conditions as used for CdTe films, CdSe films were deposited. High pure (99.999%) CdSe powder was taken to evaporate it from Mo boat in a residual ambient pressure of 10⁻⁵ mbar. Silver was found to form low resistive ohmic contact with CdSe thin films and it was used as contact material for electrical characterization of CdSe films.

3.4.1 Elemental composition

The elemental compositions of the CdSe films deposited at different T_s were analyzed using EDAX. Fig 3.4.1 shows EDAX spectrum of the film deposited at T_s = 300 K and the analysis of data revealed that the film was Se rich with Cd to Se ratio

of ~ 0.85 (in at %). Due to low sticking coefficient and thermal non-equilibrium between substrate and Cd adatoms at $T_s = 300$ K, Cd may be re-emitted to vapor state as described in section 3.2. In addition, higher vapor pressure of Se_2 in comparison to Cd also leads to non-stoichiometric films. Increasing substrate temperature was found to improve the stoichiometry as in Table 3.4.1. Stoichiometric composition was obtained at 453 K. Further increase in substrate temperature, the films became Cd rich, which may be due to re-evaporation of excess Se from growth surface.

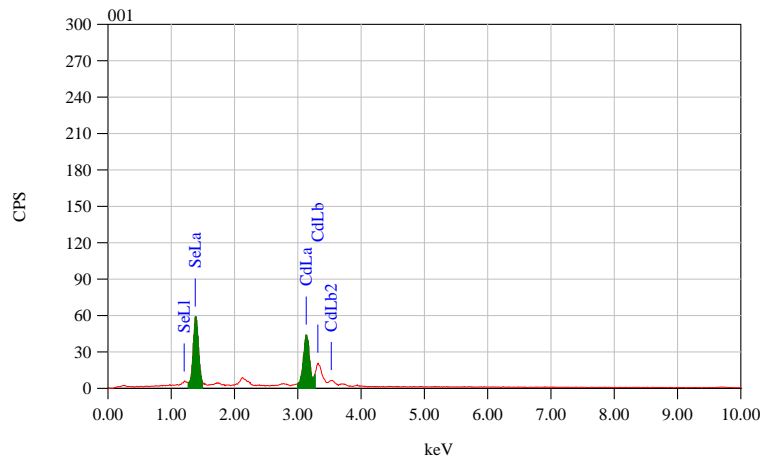


Fig. 3.4.1: EDAX spectrum of as-grown CdSe thin films deposited at $T_s = 300$ K

Table 3.4.1: Atomic ratio of elemental composition of CdSe films as function of substrate temperature

Substrate temperature (K)	Atomic ratio (at %)
373	0.85
423	0.87
453	1.00
473	1.19

3.4.2 Crystal structure

The crystal structure of the CdSe films deposited at different T_s was evaluated using XRD. The XRD pattern in Fig 3.4.2 reveals that the films have stable hexagonal phase with a prominent peak of (002) orientation. The films deposited at room temperature shows low intensity peaks (Fig. 3.4.2a) of other planes (110), (103),

and (112) whose intensity has improved (Fig. 3.4.2b) as substrate temperature increased. This indicates improvement in crystal quality. Like other II-VI compounds, CdSe also has polytypic nature, but metastable cubic phase was not observed in any of the deposited films.

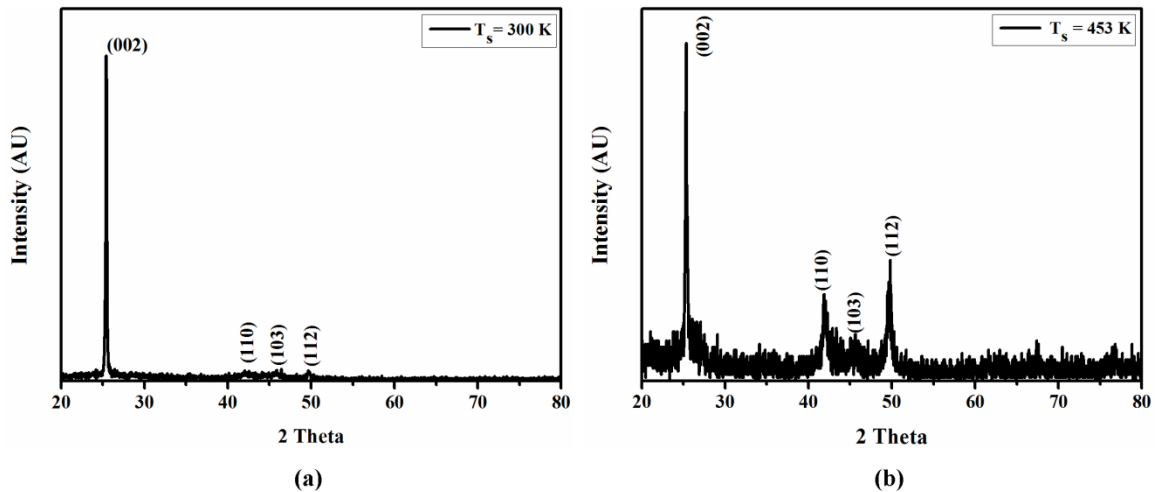


Fig. 3.4.2: XRD pattern of as-grown CdSe thin films on quartz substrate (a) at room temperature and (b) at 453 K

3.4.3 Electrical properties

The majority carrier type in all CdSe films deposited at T_s from 300 to 473 K was n irrespective of the composition of the films. The composition and crystal quality were found to affect the electrical property. The electrical resistivity of the films was measured in coplanar configuration with two silver contacts of 1cm x 1cm dimension separated by 1mm distance. The CdSe films deposited at $T_s = 300$ K had electrical resistivity of $\sim 10^4$ Ω -cm, whereas, the films deposited at $T_s = 473$ K had resistivity of $\sim 2.2 \times 10^2$ Ω -cm. However, the films with stoichiometric composition had higher resistivity. This may be due to the reduction in vacancies or point defects, which contribute to the charge carrier density. Further, the films with excess Se imply that the similar quantity of acceptor-like Cd vacancies, which may trap electrons and hence, reduce the free charge carriers. From the variation of resistance with temperature (Fig. 3.4.3), the thermal activation energy of electrical conduction was determined and it was found to vary from 0.5 to 0.7 eV for the films grown at different T_s .

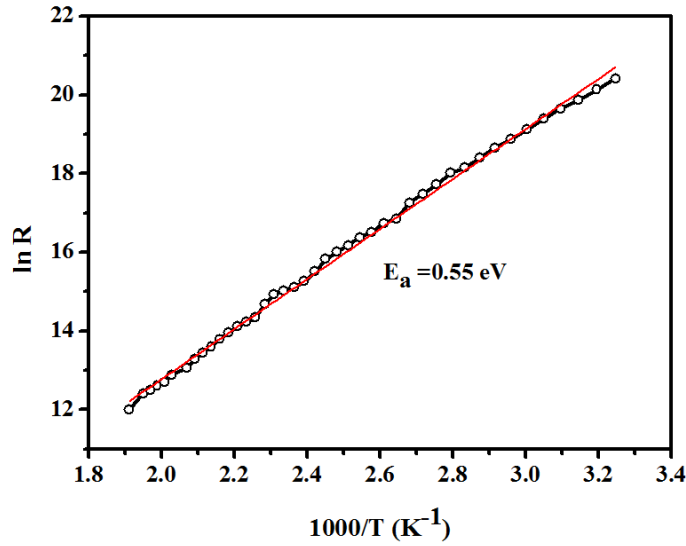


Fig. 3.4.3: Temperature dependence of resistance for CdSe thin films deposited at $T_s = 300$ K

3.5 ZnTe THIN FILMS

The interest on ZnTe thin films in the present work is due to their capability to make excellent pn heterojunction with CdSe. Among II-VI compounds, only ZnTe shows good p-type conductivity. However, it is very difficult to get n-type conductivity in ZnTe by doping with donor-like impurities either on Zn lattice position (III group elements) or on Te lattice position (VII group elements). Further, in recent years, ZnTe films have been extensively studied for its application as back contact interface layer in CdTe based solar cells due to small valence band offset with CdTe and it can be doped highly p-type ($\sim 10^{18} - 10^{19} \text{ cm}^{-3}$) to reduce contact resistance [Wu et al. 2007]. Like other II-VI compounds, ZnTe also dissociates into Zn and Te_2 during evaporation in vacuum [Goldfinger and Jeunehomme 1963, Brebrick 1969]. Hence, resultant vapor will be non-stoichiometric leading to Te rich films [Rao et al. 2009]. It is known from the previous work that for device application of ZnTe, the composition and crystallinity of the film have to be properly tuned. As described above, T_s is one of the key parameters to optimize the properties for the required device applications. Thus, growth of ZnTe at different T_s was studied. For this purpose, high purity (99.999%) ZnTe powders were evaporated from Mo boat.

3.5.1 Elemental composition

The elemental composition of ZnTe films deposited at $T_s = 300$ K is non-stoichiometric with excess Te. The elemental composition of as-grown films deposited at $T_s = 300$ K determined from the EDAX spectrum (Fig 3.5.1) was Te rich with Zn to Te ratio (in at %) ~ 0.78 . The elemental composition can be varied by altering growth conditions, in particular, by varying T_s . In the earlier study [Rao et al. 2009], it was shown that at $T_s = 553$ K, stoichiometric ZnTe can be obtained, similar to that given in Table 3.5.1. In ZnTe, Zn being more volatile and having less sticking coefficient leads to Te rich films. As T_s increased, sticking coefficient of Zn increases and atomic ratio tends towards unity (Table 3.5.1).

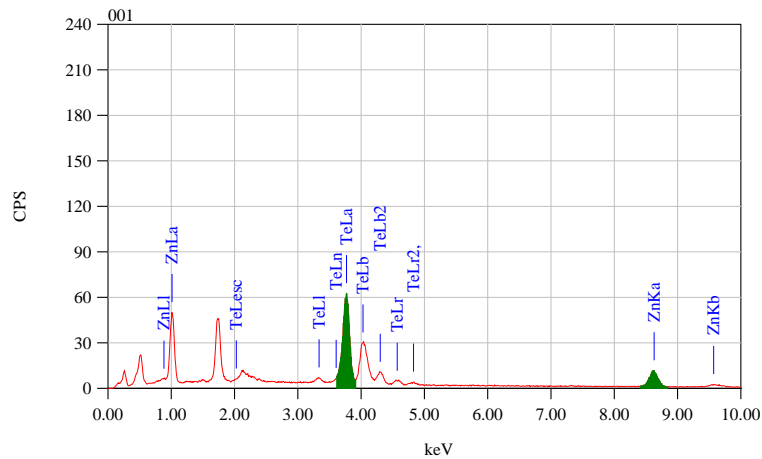


Fig. 3.5.1: EDAX spectrum of as-grown ZnTe thin films deposited at $T_s = 300$ K

Table 3.5.1: Atomic ratio of elemental composition of ZnTe films as function of substrate temperature

Substrate temperature (K)	Atomic ratio (at %)
373	0.88
423	0.90
473	0.94
523	0.97
553	1.00

3.5.2 Crystal structure

ZnTe thin films most commonly found in sphalerite (cubic) phase. Excess of non-metallic components favor cubic phase. In some cases, depending on growth conditions and in presence of excess Zn, rare hexagonal phase can also form. As-grown ZnTe films were characterized using XRD to confirm the crystal structure. Fig. 3.5.2 shows the XRD pattern of the film. This is the characteristic of ZnTe thin films with preferred (111) orientation and also agrees with previous reported data [Rao et al. 2009]. The XRD pattern did not show any peak corresponding to hexagonal phase. Upon varying the substrate temperature, diffraction pattern did not show drastic variations. However, the intensity of various peaks increased, indicating improvement in crystallinity with increasing T_s .

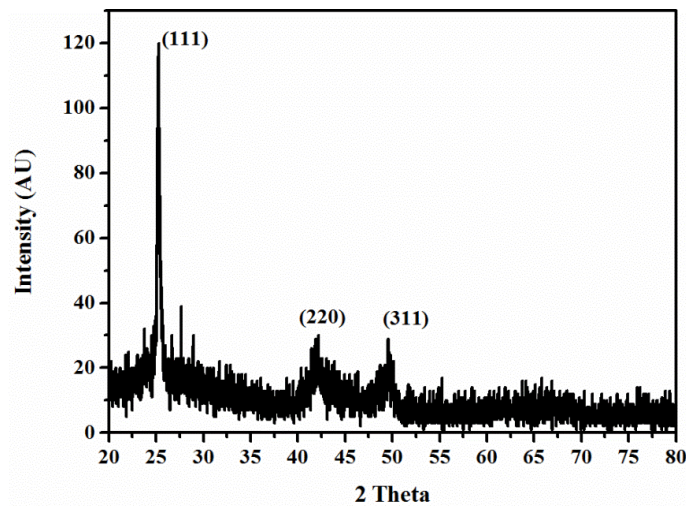


Fig. 3.5.2: XRD pattern of as-grown ZnTe thin films deposited at room temperature

3.5.3 Electrical properties

The electrical resistivity of the films was measured in coplanar configuration with two silver contact pads of sides 1cm x 1cm dimension separated by 1mm distance. Using hot probe method, the majority carrier type was determined and it was p-type. As seen earlier in section 3.5.1, ZnTe films grown at lower T_s had excess Te. That implies that a similar amount of Zn vacancies are present, which creates acceptor level in the band gap and hence of p-type conductivity. These films had black grayish color and a low resistivity of $\sim 0.49 \Omega\text{-cm}$; which also confirm presence of excess Te

in films. As substrate temperature is increased, due to improvement in composition closer to stoichiometric films, the resistivity of the films increased to $10^4 \Omega\text{-cm}$ and color of the films turned to brick red. The thermal activation energy of electrical conduction was determined from the variation of resistance with temperature (Fig 3.5.3) and found to vary from 0.17 eV to 0.9 eV for the ZnTe films deposited at T_s from 300 K to 553 K. This increase in activation energy can be attributed to the reduction of Zn vacancy level in films due to improve in stoichiometry as T_s increased.

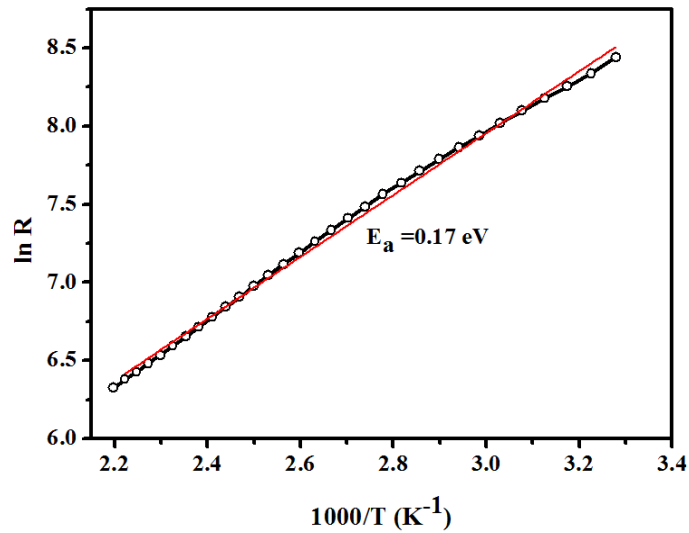


Fig. 3.5.3: A representative plot of temperature dependence of resistance for ZnTe thin films deposited at $T_s = 300 \text{ K}$

3.6 ZnSe THIN FILMS

ZnSe is a wide band gap ($E_g = 2.67 \text{ eV}$) semiconductor and it has been extensively studied for its blue-green laser and light emitting diode applications [Pessa and Ahn 1993]. Vacuum evaporated ZnSe films have been studied for their application as photo-detector and effect of growth parameter on its photoconductivity properties [Rao et al. 2011]. Since ZnSe is having wider band gap than CdS, it can be a suitable replacement in CdTe and CIGS solar cell as a buffer layer [Fahrenbruch 1977]. For this application, ZnSe film requires good n-type conductivity. Though vacuum deposited ZnSe films have high electrical resistivity, it is also shown that a combination of dopant co-evaporation and post-annealing in Zn vapor can drastically

reduce the resistivity [Aranovich et al. 1978]. Thus, the purpose of studying the growth of ZnSe films in the present work is to understand the effect of growth parameter on its electrical properties. A known quantity of high purity (99.999%) ZnSe powder was used for depositing thin films on quartz substrate. Mo boat was used for heating resistively in a vacuum of 10^{-5} mbar.

3.6.1 Elemental composition

Based on previous studies on ZnSe thin films, deposition conditions were chosen i.e. a growth rate of 30 nm/min and substrate temperature 300 K - 473 K [Rao et al. 2011]. According to that, stoichiometric ZnSe films can be grown at a T_s of 423 K. Variation of elemental composition as a function of T_s is given in Table 3.6.1. The elemental composition of ZnSe films deposited at $T_s = 300$ K was determined from analysis of EDAX plot (Fig. 3.6.1) and film was found to be Se rich with Zn to Se ratio (in at %) ~ 0.89 . Similar to ZnTe case, at lower T_s , Zn has low sticking coefficient than that of the Se. At T_s above 423 K, the films were Zn rich.

3.6.2 Crystal structure

Like CdTe and ZnTe, thin films of ZnSe also grow in stable sphalerite phase. In addition, it also shares the feature of growing in metastable hexagonal phase in Zn rich conditions provided other deposition conditions are favorable. To verify this, the ZnSe films were characterized using XRD. Fig. 3.6.2 shows diffraction pattern of ZnSe film deposited at $T_s = 300$ K. It exactly matches with JCPDS file 37-1463 confirming that the grown film has cubic phase. Lattice parameter of ZnSe film, $a = 5.61\text{\AA}$ was calculated from the obtained diffraction pattern. Besides, diffraction pattern did not show any peak corresponding to hexagonal phase. Therefore, it can be concluded that the grown films had pure cubic phase or minimum metastable phase. ZnSe films grown at higher T_s found to have improved crystalline quality without altering the pattern. The crystallite size was also found to depend on the growth rate and it varied from 55 nm to 10 nm as the rate increased from 20 to 200 nm/min [Rao et al. 2013]

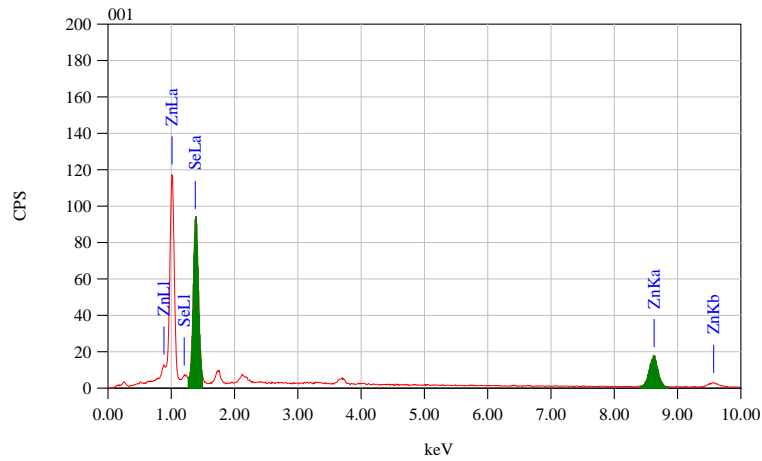


Fig. 3.6.1: EDAX spectrum of as-grown ZnSe thin films deposited at $T_s = 300$ K

Table 3.6.1: Atomic ratio of elemental composition of ZnSe films as function of substrate temperature.

Substrate temperature (K)	Atomic ratio (at %)
373	0.95
423	1.00
473	1.07
523	1.13

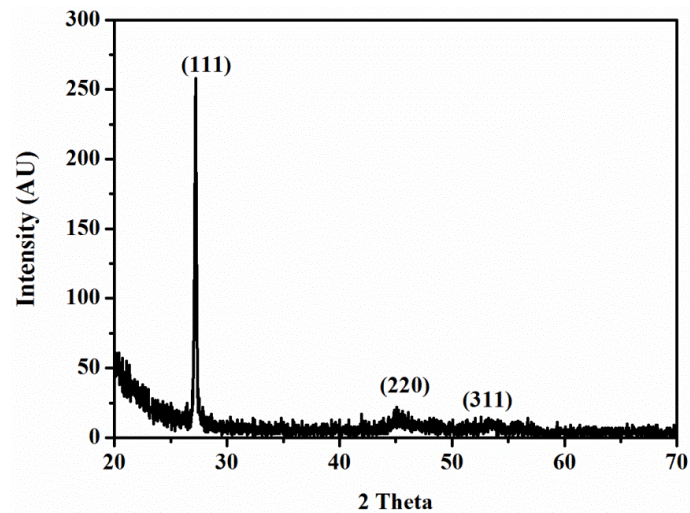


Fig. 3.6.2: XRD pattern of as-grown ZnSe thin films on quartz substrate at room temperature

3.6.3 Electrical properties

The ZnSe films deposited at substrate temperature 300 K and 473 K were n-type as determined with hot-probe method. The electrical resistivity of the films was measured in coplanar configuration with two silver contacts of 1cm x 1cm dimension separated by 1mm distance. The film deposited at 300 K had high resistivity ($10^4 \Omega\text{-cm}$) in comparison to the film deposited at 473 K ($10^2 \Omega\text{-cm}$). The possible reason for this may be the variation in composition of the film and crystallinity with T_s as seen in section 3.6.1 and 3.6.2. High resistance film had excess Se, which compensates the electrons, whereas low resistance ones had excess Zn contributing extra charge carriers. These trends of ZnSe films conform with previous reported data, according to which charge carrier concentration also increases from $4 \times 10^{14} \text{ cm}^{-3}$ to $14 \times 10^{14} \text{ cm}^{-3}$ with increasing T_s [Rao et al. 2013]. Fig. 3.6.3 shows the temperature dependence of the electrical resistivity for the film deposited at $T_s = 473 \text{ K}$. The activation energy for electrical conduction also decreased from 0.6 eV to 0.2 eV for films deposited at 300 K and 473 K, respectively.

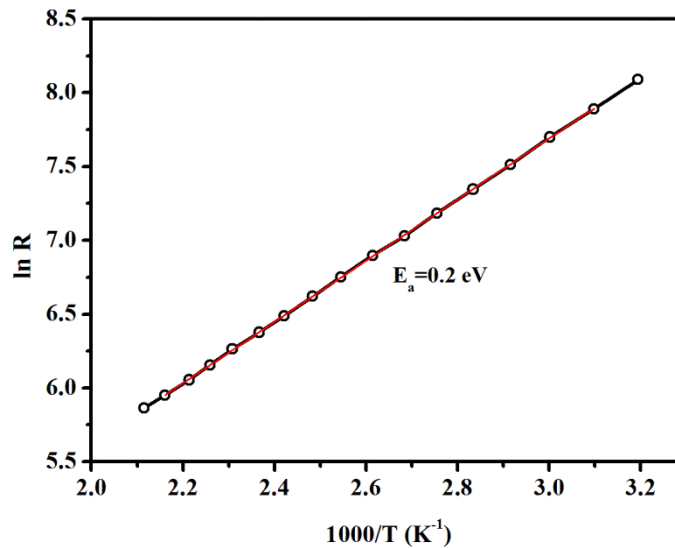


Fig. 3.6.3: A representative plot of temperature dependence of resistance for ZnSe thin films on quartz substrate at $T_s = 473 \text{ K}$

3.7 DISCUSSION

Although all the four compounds, CdTe, CdSe, ZnTe, and ZnSe dissociate during evaporation, they do form compound on substrate surface. The vapor pressure studies

using mass spectroscopy and other indirect methods have shown that constituents of the compounds in vapor state will be separate as metallic component and diatomic non-metallic molecular component [Goldfinger and Jeunehomme 1963]. Unlike ZnO, where binding energy of O₂ is higher than that of Zn and ½ O₂, these diatomic and higher weight molecules have lower binding energy than II-VI compound. Hence, if sufficient T_s is provided, these adatoms on substrate surface readily form II-VI compounds and at lower T_s, non-crystalline mixture (or inclusions) of the molecular species can be condensed [Shreekanthan et al. 2003]. As T_s is increased, these non-crystalline mixture of molecules may re-evaporate letting the formation of ordered compounds with favorable crystallite phase [Vincett et al. 1977].

This interpretation for the observed stoichiometry at a suitable T_s for each of the four compounds can also be given in an alternative approach based on phase diagram [Heisler et al. 2013]. Based on phase diagram of CdTe, melting point of CdTe is 1092 °C and that of Cd and Te is 594 K and 723 K, respectively. These temperatures are from CdTe phase diagram at 1 bar pressure, whereas the deposition process of compounds takes place in vacuum, i.e., at much lower pressure and liquid phase is absent; materials directly sublime to gas phase. At lower pressure, the evaporation temperature of the materials also reduces, for instance, at a pressure of 10⁻⁶ mbar, the sublimation temperatures of Cd and Te are 373 K and 463 K, respectively [Heisler et al. 2013]. Because of this, if T_s is above 463 K, only stoichiometric CdTe will be deposited and elementary Cd and Te₂ will sublime from the substrate. With vacuum level, these temperature values may vary a little; same explanation will apply to the other compounds for observed stoichiometric deposition at certain temperatures.

Similar idea can be applied for structural ordering at sufficiently high T_s for respective compounds. High T_s, along with re-evaporation of excess elemental atoms, provide adatoms enough energy to diffuse laterally to form coarse grains, whereas at low T_s, the growth is diffusion limited and hence leads to large number of fine grains [Chopra 1969, Chan and Hill 1976, Dhere et al. 1977, Uthanna and Reddy 1983]. Since the predominant scattering mechanism at the studied temperatures is mainly grain boundary scattering, the grain boundary width may considerably affect the electron transport in these films.

The four compounds, CdTe, CdSe, ZnTe, and ZnSe are known to exhibit polymorph and can exist in both sphalerite (cubic) and wurtzite (hexagonal phase) depending on growth conditions. The crystal structure of these films are also found to depend on relative concentration of constituent elements [Däweritz 1971, Shalimova and Dmitriev 1972]. For example, in case of CdTe with excess Te, the films grow in cubic phase, but excess Cd in films favor hexagonal phase. However, percentage of hexagonal phase depends on many other factors such as growth temperature, ambience, and vacuum. Similar arguments hold for ZnSe and ZnTe, whereas CdSe shows opposite behavior. CdSe films deposited at low T_s with excess Se favors hexagonal phase [Däweritz and Dornics 1973]. A possible explanation for such a behavior of these compounds is crystallographic axial ratio of these compounds, whether it is larger or smaller than ideal $c/a = \sqrt{8/3}$. CdTe, ZnSe and ZnTe have larger axial ratio than the ideal value, while CdSe has a smaller value [Däweritz and Dornics 1973].

The observed electrical properties such as resistivity and carrier concentration in all the four compounds are very sensitive to the stoichiometry and crystallinity. As crystallinity improves the conductivity improves, but slight deviation in composition can have significant effect on electrical properties [Ma et al. 2013 Chin et al. 2015]. This nature of II-VI compounds can be attributed to the ionic nature of the chemical bonding of the compounds. Slightest deviation creates either acceptor-like (vacancy of metallic element or interstitial occupation of non-metallic element) or donor-like (vacancy of non-metallic element or interstitial occupation of metallic element) defects. The electrically active defects in II-VI act as unintentional dopants, hence can be used without needing impurity atoms [Ahmad et al. 2014, Chin et al. 2015]. However, this leads to very low carrier concentration in these compounds to be applicable in devices. Also, this makes the doping difficult by compensation through easily forming structural disorders [Desnica 1998a]. The doping and post deposition treatments of the compounds are described in next chapter.

3.8 CONCLUSIONS

The four technologically important II-VI compounds, CdTe, CdSe, ZnTe, and ZnSe have been grown using vacuum evaporation. The effect of growth parameter, in

particular substrate temperature on its crystal structure, stoichiometry, and electrical properties were studied.

The elemental composition was found to be non-stoichiometric when deposited on a substrate at room temperature. The elemental ratio between II group element and VI group element for CdTe, CdSe, ZnTe, and ZnSe were 0.89, 0.85, 0.78, and 0.95, respectively. Increasing substrate temperature improved the elemental ratio towards unity and stoichiometric composition was attained for CdTe, CdSe, ZnTe, and ZnSe at substrate temperature 523 K, 453 K, 553 K, and 423K, respectively. As stoichiometry improved, the crystallinity also enhanced due to the re-evaporation of disordered and excess elemental component at elevated substrate temperature. The analysis of XRD patterns showed that all four compounds had stable phase i.e. CdTe ZnTe and ZnSe had cubic (sphalerite) phase and CdSe had hexagonal (wurtzite) phase.

All four samples had poor conductivity when deposited on a substrate at room temperature. The poor conductivity of the sample may be due to the native defects like vacancy and interstitials typical to these compounds. The activation energy for electrical conduction determined from temperature dependence of the resistance had indicated the presence of deep traps in forbidden gap.

CHAPTER 4

OPTIMIZATION OF CdTe FILMS

Overview

This chapter describes post deposition process such as heat treatment and also doping of CdTe films. Effect of heat treatment on composition of the CdTe films and its electrical properties have been studied. Doping of CdTe films with indium and presence of excess tellurium were studied in order to improve their electrical conductivity.

4.1 POST DEPOSITION PROCESSING

Post deposition heat treatment of doped CdTe has strong influence on structural and hence on other related properties, for instance, electrical and optical properties [Moutinho et al. 1998, Romeo et al. 2000, 2004, Enriquez and Mathew 2004]. Post deposition treatment may involve thermally activated diffusion of elements or segregation and chemical modifications. These factors are very critical in CdTe based solar cell fabrication. The high efficiency CdTe solar cells often involve annealing for 10-30 minutes at 400°C in CdCl₂ ambience after CdTe depositions. This heat treatment step is also known as CdCl₂ passivation or activation step, which involves grain growth by reducing strain energy or surface free energy [Zoppi et al. 2006, Consonni et al. 2008]. Scanning electron micrograph and diffraction studies on chlorine (Cl) doped CdTe as a function of annealing has shown structural reordering with <100> texture formation [Consonni and Feuillet 2009]. Positron annihilation studies on thermal evaporated CdTe has shown that density of divacancy $V_{Cd}-V_{Te}$ reduces from 10^{18} to 10^{16} cm⁻³ after annealing at 400° C for 30 min [Liszkay et al. 1994].

It is very difficult to avoid defect formation during growth of CdTe and related compounds, irrespective of the growth techniques used. The films are often found to have extended defects such as twin boundaries that lead to dangling bonds in grains. Such defects can act as traps for charge carriers and hence, as-deposited CdTe films

exhibit poor electrical conductivity [Yan et al. 2004]. Further, these extended defects enhance the segregation phenomena in grains, which may lead to doping inhomogeneities [Consonni et al. 2006, 2007]. Annealing in different atmosphere is a proven step for passivation of these defects and improves the electrical properties of the CdTe thin films [Giles et al. 1988, McCandless and Dobson 2004, Gessert et al. 2013].

On the other hand, depending on ambient conditions, heat treatment may alter the chemical composition of the materials and their electrical activity [Chamonal et al. 1982, Takahashi et al. 1985]. Upon annealing, for example, acceptor like Cl complex will dissociate into Cl donor and A-center. It also leads to diffusion and re-evaporation of Cl from film. Hence, reduction in concentration of Cl and its spatial redistribution in CdTe:Cl films take place [Consonni and Feuillet 2009]. Similar effects were found in Cu and Ag doped CdTe films. In such cases, low temperature annealing produces acceptor like defects and higher temperature treatments lead to formation of compensating complexes due to excess Cu diffusion into CdTe [Chamonal et al. 1982].

In the present work, effect of annealing on composition and electrical conductivity of CdTe thin films grown using thermal evaporation technique has been studied. The undoped and doped CdTe films were grown on quartz substrate. This would avoid possible diffusion of sodium ion during heat treatment from commonly used sodalime glass substrates and its consequence on structure and electrical properties.

Compositional analysis of the CdTe was carried out as a function of annealing temperature. The EDAX data of the CdTe films deposited at different substrate temperatures and annealed at 573 K in air and vacuum for 2 hours is given in Table 4.1. As can be seen from the Table 4.1, the stoichiometry was attained for the CdTe film deposited at substrate temperature of 473 K in the case of air annealing. The CdTe films deposited at lower substrate temperatures, annealed in air were Cd rich, and expected to show n-type conductivity. CdTe films annealed in vacuum were stoichiometric irrespective of substrate temperature. In both cases, the films were Te rich prior to the annealing. Out diffusion and re-evaporation of excess Te while

annealing in vacuum may be the reason for observed stoichiometry in respective CdTe films. Similar results have been reported earlier [Sravani et al. 1995, Ahmad et al. 2014].

Table 4.1: Composition of CdTe annealed at 573 K in air and vacuum for 2 hours

Substrate Temperature (K)	Cd/Te (at. %)	
	Air Annealed	Vacuum Annealed
373	52.0/48.0	50.3/49.7
423	51.0/49.0	50.1/49.9
473	50.2/49.8	49.3/50.7

All the CdTe films deposited at different substrate temperatures and annealed at different conditions had high resistance ($> 2 \text{ G}\Omega$ at room temperature). The variation of resistance with temperature were plotted to determine the activation energy for both air and vacuum annealed films (Fig. 4.1). The activation energy was extracted from the slope of the straight line and is given in Table 4.2. The activation energy varied from 0.56 eV to 0.73 eV as substrate temperature varied from 300 K to 473 K.

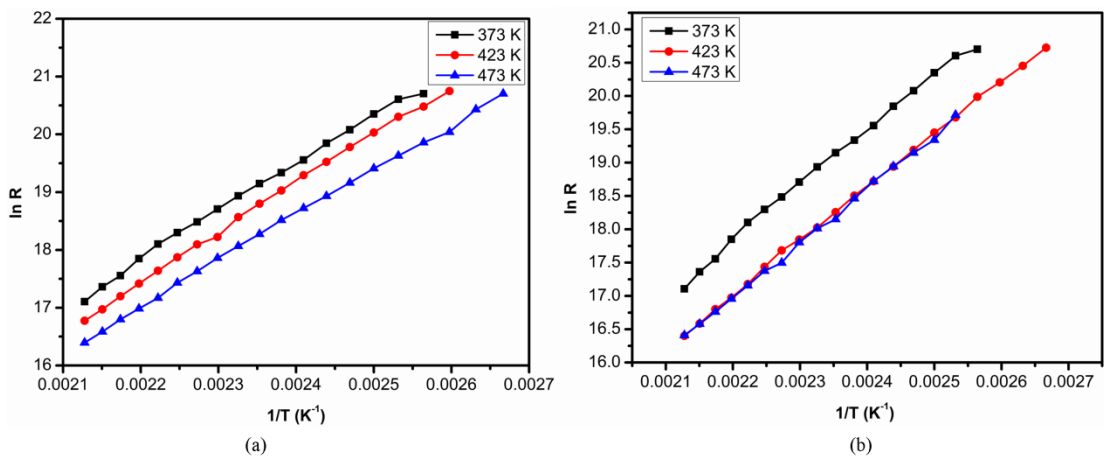


Fig. 4.1: Variation of resistance as a function of temperature of CdTe thin films annealed (a) in air and (b) vacuum.

Table 4.2: Activation energy of CdTe films deposited at different substrate temperature and annealed for 2 hours.

Substrate Temperature (K)	Activation energy (eV)	
	Air (573 K)	Vacuum (573 K)
300	0.56	0.57
373	0.68	0.72
423	0.56	0.70
473	0.72	0.73

The increase in activation energy of the air annealed CdTe films with substrate temperatures might be due to the variation of composition with substrate temperature. It is well known that the stoichiometric II-VI compounds have very high resistivity, as carrier density is very small. Off-stoichiometric films have vacancies or point defects that are electrically active due to ionic nature of the compounds and hence, act as either donor or acceptors. These defects contribute to the carrier density of the films, thereby reducing the activation energy. In vacuum annealed CdTe, composition was close to stoichiometric composition and did not vary much with substrate temperature. For stoichiometric films, the conduction will be mostly intrinsic and the activation energy corresponds to the centre of the band gap. The charge carrier concentration as determined from Hall Effect measurements is of the order 10^{13} cm^{-3} .

4.2 DOPING

The optical, electrical, and mechanical properties of CdTe thin films can be considerably changed by doping. Among II-VI compounds, only CdTe can be doped to get n-type or p-type conductivity with relative ease. First or fifth group elements act as acceptors and third or seventh group elements act as donors. Nonetheless, dopants may exhibit amphoteric nature depending on either it occupies atomic or interstitial site. The doping of Cu in CdTe is an example for such behavior. When Cu is added in small concentration, it occupies Cd site, acts as an acceptor and as the content of Cu increases, it may occupy interstitial sites that acts as donor [Wei and Zhang 2002, Kranz et al. 2013]. This will lead to carrier type conversion and thereby,

will have deleterious effect on electrical properties of CdTe. It has been a major obstacle in achieving high efficiency in CdTe based thin film solar cell.

The main feature of CdTe and other II-VI compounds is the ionic nature of the bonding between adjacent atoms in contrast to the covalent bonding in other group semiconductors. This gives rise to a range of electrically active native defects and their associated complexes that hinders the doping through self-compensation and dopant compensation properties of these compounds. In addition, chemical solubility, diffusivity, and segregation of the dopants, formation of second phase create formidable challenge.

Despite the difficulties in doping, the demands of technological front on properties of CdTe based devices have made advances in finding out the possible routes for successful doping. Some of them are equilibrium approach such as co-doping [Neumark 1997, Desnica 1998] and a few are non-equilibrium approach e.g., ion implantation and low temperature crystal growth [Georgobiani et al. 1989, Wichert et al. 1993, Hwang et al. 1996].

In CdTe solar cells, increasing the hole density and carrier lifetime would increase the open circuit voltage and hence, the efficiency. The carrier density in as-deposited CdTe is in the range of 10^{13} - 10^{14} cm^{-3} . This will also increase the series resistance of the films thereby reducing the efficiency. Cu is the most commonly used dopant in CdTe based solar cells. In such cases, Cu is actually added to back contact from which it diffused into CdTe while processing. This was found to increase the carrier lifetime in CdTe [Gessert et al. 2005, 2009]. But aging effect and fast diffusion of Cu seem to deteriorate the photovoltaic property of CdTe [Gessert et al. 2005]. Recently, there are a few reports where Te was added in excess to CdTe in order to increase hole density [Sravani et al. 1995, Heisler et al. 2013, Ahmad et al. 2014]. Adding excess Te is expected to overcome the limitation imposed by upper limit of Cu doping in CdTe.

For detector application, the resistivity of the CdTe should be high ($>10^9$ $\Omega\text{-cm}$) to reduce dark current, device noise and mobility-lifetime product for photo-generated carriers so that it can reach the electrodes before getting lost through recombination.

These semi-insulating CdTe are obtained via doping with deep donors or acceptors such as Ge and Sn [Panchuk et al. 1999, Fiederle et al. 2004, Babentsov et al. 2007, 2008]. However, high resistive CdTe were often obtained via doping with shallow donors such as In, Al and Cl [Eiche et al. 1993, Fiederle et al. 2003, Xu et al. 2009]. These dopants are expected to improve the n-type conductivity of CdTe. The interaction of shallow dopants and native defects in the materials give rise to high resistivity [Biswas and Du 2012]. Hence, the control of native defects and dopants is desirable to achieve required conductivity.

In the present work, effect of doping on properties of CdTe films during the growth and subsequent annealing was studied. Two dopants were considered in the study namely indium (In) and tellurium (Te). The dopants were mixed with CdTe powder and evaporated from molybdenum boat. The variation of electrical resistance and carrier concentration was studied by varying the dopant content in source material. The samples were annealed at 573 K for 2 hours. A small concentration of indium in CdTe is expected to act as donor impurity and enhance the n-type conductivity, if deep level or compensating defects are minimized. In the second case, excess tellurium is added to CdTe that creates Cd vacancies. The Cd vacancies act as acceptors, therefore, are expected to improve the p-type conductivity in CdTe films.

4.2.1 In doped CdTe films:

The properties of the grown films depend considerably on the crystalline quality and the composition of the compounds. Fig. 4.2 shows the XRD patterns of CdTe and of In doped CdTe thin films deposited, respectively on quartz substrate. The XRD pattern of all samples exhibited single strong peak at an angle $2\theta = 28.3^\circ$, which corresponds to (111) plane of CdTe. Similar features have been found for Te doped CdTe. Doping with In and Te did not alter the crystal parameters and crystallinity.

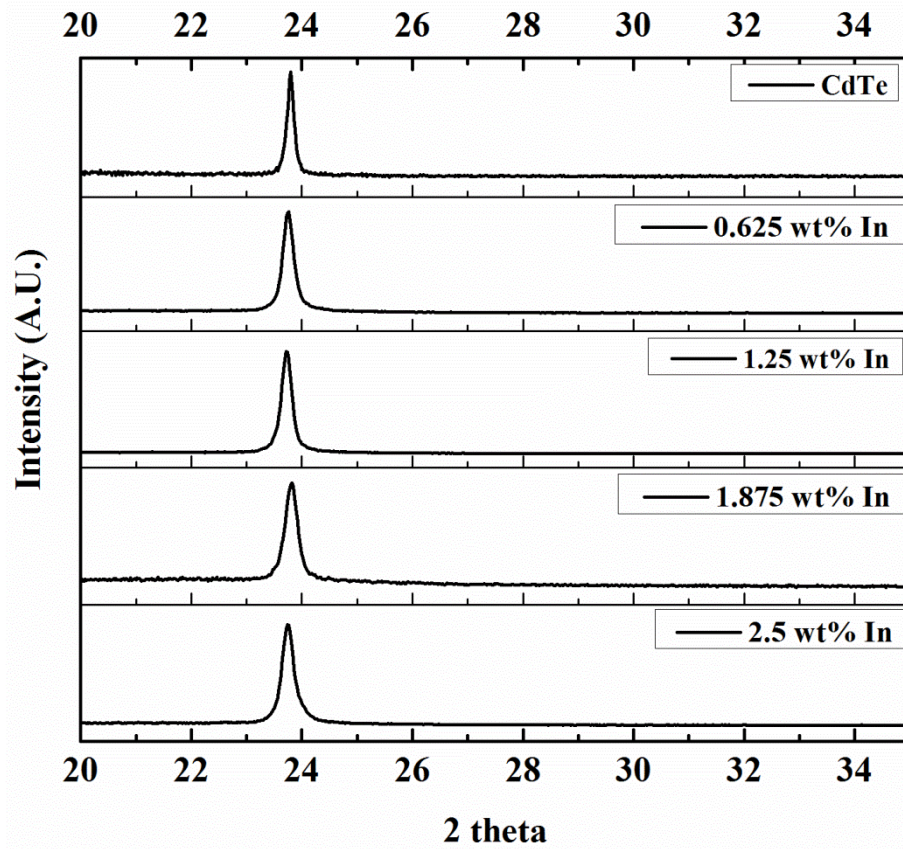


Fig. 4.2: XRD patterns of CdTe and In doped CdTe

The resistivity, activation energy for electrical conduction and majority carrier type for different In concentration are listed in Table 4.3. Fig. 4.3 shows the variation of resistance with temperature, from which the activation energy was extracted. The samples having lowest In concentration (wt% 0.625) had high resistivity. Further increase in In concentration in the films reduced the resistivity, as it can be seen in Table 4.3. However, the decrease in resistivity is small in these two samples in comparison to the undoped and sample with 0.625 wt% In. The main reason for this, is the electrical activity of dopants in CdTe and related compounds are controlled by native defects. Generally, the room temperature deposited CdTe films are excess in Te, which creates acceptor like Cd vacancy (V_{Cd}) or Te interstitials (Te_i). In such cases, adding small quantity of In to CdTe increases the resistance due to the compensation of donors by acceptor-like defects and further increase in In concentration increases donor density.

Table 4.3: Resistivity and thermal activation energy of electrical conduction of In doped CdTe

In concentration (wt %)	Resistivity, ρ (Ω -cm)	Activation energy, E_a (eV)	Carrier type
0.625	--	0.79	--
1.250	1500	0.36	n
1.875	1310	0.34	n

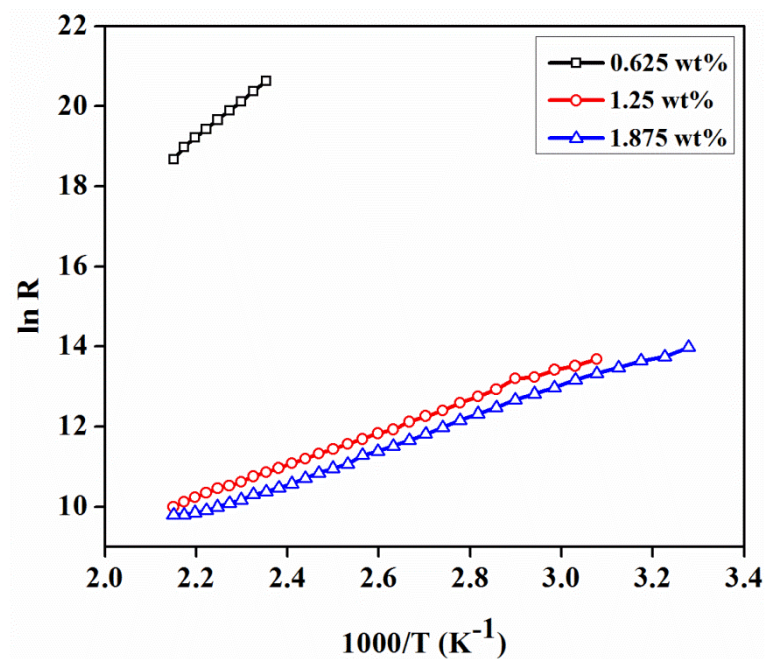


Fig. 4.3: Variation of resistance of In doped CdTe with temperature.

4.2.2 Effect of annealing on In doped CdTe

Annealing of CdTe samples seemed to reduce the resistivity and thermal activation energy of electrical conduction. In Table 4.4, the thermal activation energies for the In doped CdTe films before and after annealing at 573 K for 2 hours are compared. The improvement in the conduction might be due to the diffusion and proper redistribution of In in CdTe film. As an effect of annealing, the carrier concentration in In doped CdTe had improved up to 10^{15} cm^{-3} , which were very low to be measured at room temperature in undoped and lowest concentration (0.625 wt%) In doped CdTe.

Table 4.4: Effect of annealing on activation energy and carrier concentration of In doped CdTe

In wt%	Carrier concentration (cm ⁻³)	Activation energy, E _a (eV)	
		Annealed at 573 K for 2 hrs	as-deposited
0.625	2.52 x 10 ¹³	0.0940	0.79
1.250	6.67 x 10 ¹⁴	0.0280	0.36
1.875	9.30 x 10 ¹⁴	0.0110	0.34
2.500	1.15 x 10 ¹⁵	0.0097	0.29

4.2.3 Te Doped CdTe

It has been observed that, the CdTe films without any extrinsic doping has very low conductivity. The electrical conductivity in these films can also be improved by adding excess of Te. The excess Te gives hole density upto about 10¹⁶ cm⁻³ by the formation of acceptor-like V_{Cd} and/or Te_i. The resistivity, activation energy for electrical conduction and majority carrier type for different amount of excess Te are listed in Table 4.5.

Table 4.5: Resistivity and electrical conduction activation energy of excess Te in CdTe

Excess Te in CdTe (wt%)	Resistivity, ρ (Ω-cm)	Activation energy, E _a (eV)	Carrier type
1.250	2920	0.25	p
1.875	964	0.16	p
2.500	456	0.13	p

Similar to In doped CdTe, the films with excess Te, small concentration of excess Te (1.25 wt%) has high resistivity and activation energy. At high concentration of excess Te, i.e., 1.875 wt% and 2.5 wt%, the resistivity and activation energy reached the reported respective values [Glang et al. 1963]

4.3 CONCLUSIONS

The post deposition treatment and doping are important steps in order to improve the structural, compositional and hence, the electrical properties desired for applications of CdTe. As-deposited films in the present work were Te rich, which attained stoichiometric composition upon annealing. Air annealing of CdTe films lead to Cd rich films. Annealing of doped CdTe films was also found to improve the electrical properties of the films. Indium doped CdTe films, upon annealing, had improved n-type conductivity. The electron density also varied from 10^{13} to 10^{15} cm^{-3} with In content from 0.625 wt % to 2.5 wt % in CdTe films. Similarly, hole density varied from 10^{13} to 10^{16} cm^{-3} with excess Te concentration from 1.25 wt% to 2.5 wt% in CdTe films.

CHAPTER 5

FABRICATION AND EVALUATION OF HETEROJUNCTIONS

Overview

In this chapter, the electrical properties of n-ZnSe/p-CdTe, n-CdSe/p-ZnTe, p-Si/n-CdTe, and n-Si/p-CdTe prepared by thermal evaporation are described. The electrical studies include the dark current-voltage characteristics and temperature dependence of saturation current to understand the parameters controlling the carrier transport mechanism in the heterojunction diode. The admittance and capacitance-voltage characteristics of the junction at different frequencies and bias voltages provide insight into the defect structure in the bulk and at interfaces. The results of current-voltage and capacitance-voltage characteristics have been evaluated, as they are crucial to determine the device performance.

5.1 INTRODUCTION

Heterojunctions are formed by joining two different semiconductors having different energy band gap. The difference in energy band gap is accommodated by discontinuities in valence and conduction band edges i.e., ΔE_v and ΔE_c . Band bending on either side of the interface is seen in p-n junctions and metal-semiconductor junctions, but band discontinuity is unique to heterojunctions. Such discontinuities play a crucial role in determining carrier transport and confinement properties of the heterojunctions. They also influence the optical response and in general, the performance of heterojunction based devices. Heterojunctions offer a wide range of design choice for novel semiconductor devices like bipolar junction transistors, high electron mobility transistors, laser diodes, light emitting diodes, photo-detectors, photovoltaic, etc.

Based on the conductivity type of the semiconductors involved in heterojunctions, they can be classified into two types: isotype (having same type of conductivity e.g. n-n and p-p) and anisotype (having different type of conductivity such as p-n junctions). Three different kinds of heterojunctions are possible depending on band alignment at

interface of constituent compounds (Fig. 5.1). They are Type I (straddled alignment), Type II (Staggered alignment) and Type III (broken alignment). Type I heterojunctions are advantageous for light emitting or laser diode applications, as such kind of heterojunctions can confine charge carriers in narrower band gap materials. In type II heterojunctions, the conduction and valance band edge of one material is lower than the corresponding band edge of the other material. This feature of the heterojunction enhances the spatial separation of photo-generated charge carriers, which makes them very attractive for photovoltaic applications [Lo et al. 2011, Wang et al. 2014]. Thus, desired device characteristics can be achieved by suitable combination of compounds.

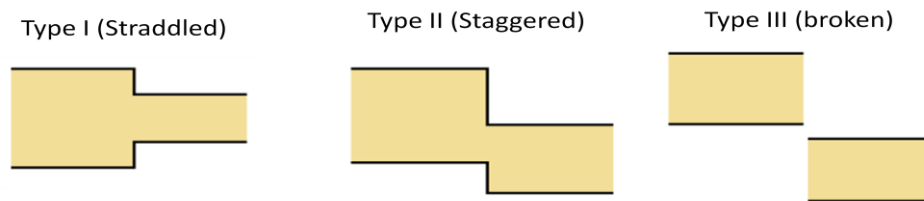


Fig. 5.1: A schematic showing three possible band alignments at hetero-interface

The interest in II- VI semiconductor heterojunctions arise from the necessity of forming p-n junction and low resistance ohmic contact in solar cell, LEDs, and other optoelectronic devices. Moreover, tandem solar cells containing multiple heterojunctions made up of different II-VI compound have great potential for high efficiency.

5.2 FABRICATIONS OF HETEROJUNCTIONS

The heterojunction of n-ZnSe/p-CdTe, n-CdSe/p-ZnTe, In doped n-CdTe/p-Si and Te rich p-CdTe/n-Si were fabricated using thermal evaporation to study their electrical properties. High purity powders of CdTe (Sigma Aldrich, 99.999%), CdSe (Sigma Aldrich, 99.999%), ZnSe (Alfa Aesar, 99.999%) and ZnTe (Alfa Aesar, 99.999%) were used as sources. The pressure in the evaporation chamber for all thin film growth was maintained at approximately 10^{-5} mbar. The distance between source and substrate distance was about 10 cm. The desired patterns of the sample for electrical studies were defined through shadow mask placed on the substrate during the deposition. For electrical characterization of the films, In (Alfa Aesar, 99.999%) was

used as metal contact for n-type materials and Ag (Alfa Aesar, 99.999%) for p-type materials. The electrical transport mechanism and interface properties such as barrier height and band offsets were analyzed using current-voltage (I-V) and capacitance-voltage-frequency (C-V-f) characteristics of the heterojunctions. The ac modulation amplitude of 50 mV and frequency sweep from 20Hz to 2MHz were used for C-V and admittance measurements.

5.3 EVALUATION OF HETEROJUNCTIONS

I-V characteristics of heterojunction provide essential parameters, such as the barrier height, parasitic resistances etc., which limit device performance. In heterojunctions, the barrier heights at the interface for electrons and holes are of different magnitude. Depending on the band alignment at interface, the current in a heterojunction consists of only of electrons or holes. In homojunctions, the diffusion of carriers is a significant contributor for the voltage dependence of the current. In heterojunctions, I-V characteristics depend on thermionic emission across the interface at low doping level and the tunnel current in heavily doped semiconductors. Several authors have proposed and verified models on conduction mechanism in heterojunctions [Chang 1965, Horio and Yanai 1990, Bhapkar and Mattauch 1993, Yang et al. 1993, Cavallini and Polenta 2008], which is similar to thermionic emission and diffusion model (referred as TED) proposed by Sze and Crowell [1966] for a metal-semiconductor junction. Hence, the I-V characteristics of heterojunction can be represented in general form as follows,

$$I = I_s \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (5.1)$$

where, I_s is the reverse saturation current, k is Boltzmann's constant, n is diode ideality factor, T is the temperature and q is the elementary charge. The saturation current I_s is given as

$$I_s = AA^{**}T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \quad (5.2)$$

where A^{**} is the reduced effective Richardson constant, A is area of the device and ϕ_b is the barrier height. According to above model expressed by Eq. 5.1, the ideality

factor should be unity. However, in practical cases, the diode current deviates from TED conduction mechanism at lower and high bias voltages. The deviation from ideal nature can be attributed to the presence of defects and series resistance of diode. These factors contribute to different conduction mechanisms that are prevalent at different bias levels. The series resistance arising from the bulk resistance of the semiconductors and metal-semiconductor interface affects the junction current and hence, the device performance. Another factor affecting the device performance is the shunt resistance, which provides leaky paths for the charge carriers at reverse bias conditions and low forward bias [Dongaonkar et al. 2010]. The above Eq. 5.1 can be re-written by considering the series and shunt resistance as follows:

$$I = I_0 \left\{ \exp \left[\frac{q(V - IR_s)}{nkT} \right] - 1 \right\} + \frac{V - IR_s}{R_{sh}} \quad (5.3)$$

where R_s is series resistance and R_{sh} is shunt resistance. The first term in Eq. 5.3 corresponds to junction current and second term is shunt leakage current, which contributes to total current through the diode.

As long as the density of thermally generated free carriers is dominant, the current flows in diodes according to the above equations 5.1, 5.2, and 5.3. Otherwise, the current is controlled by space charge build-up due to the low mobility and low thermally generated charge carriers at high-injected current. In such cases, the current increases as square of the voltage. In presence of traps, the current depends on its density and activation energy, which can be expressed as follows [Mathew 2003]:

$$I = \left(\frac{9AV^2 N_c \mu \epsilon_0 \epsilon_r}{8L^3 N_t} \right) \exp \left(\frac{-E_t}{kT} \right) \quad (5.4)$$

where ϵ_r is the relative permittivity, N_c is the effective density of the states in the conduction band, N_t is the concentration of traps with activation energy E_t , L the thickness of the film, μ carrier mobility.

Capacitance-voltage characteristics are useful for determining fundamental parameters in heterojunctions such as charge carrier concentrations and barrier height. In reverse bias condition, the variation of depletion region width of the

heterojunctions and hence, variation of the junction capacitance with bias voltage can be approximated by [Sze and Ng 2007],

$$\frac{1}{C^2} = 2 \left[\frac{\left(V - V_b + \frac{kT}{q} \right)}{q \epsilon_o \epsilon_r N A^2} \right] \quad (5.5)$$

where ϵ_r dielectric constant, V is applied voltage, V_b is built-in potential, N is doping density and A is the effective area of the diode. The junction capacitance at different bias voltages were measured by superimposing an ac supply of 50 mV modulation amplitude over dc bias voltage and frequency sweep from 20Hz to 2MHz.

5.4 n-ZnSe/p-CdTe HETEROJUNCTIONS

Among II-VI compounds, CdTe is one of the extensively studied materials, particularly for photovoltaic (PV) applications. It has a near optimum band gap to achieve maximum efficiency as required by Shockley and Queisser limit (1961). Thin film PV cell fabricated with CdTe/CdS is the most efficient cell among the II-VI compounds, but efficiency is still far from its theoretical limit. The band gap difference and absorption beyond wavelength 500nm limits its maximum achievable efficiency [Fahrenbruch 1977, Chu and Chu 1993, 1995]. Replacing a CdS layer with wider band gap materials as the window layer is expected to enhance the efficiency of PV cells [Aranovich et al. 1978, Chu and Chu 1993, Spalatu et al. 2011]. Hence, p-CdTe/n-ZnSe should have higher theoretical conversion efficiency [Bube et al. 1977]. Very few studies have been reported on the optical and photovoltaic properties of p-CdTe/n-ZnSe heterojunction prepared using close spaced sublimation technique [Bube et al. 1977, Buch et al. 1977, Chu et al. 1992, Potlog et al. 2011, Spalatu et al. 2011]. Further, for improvement of the efficiency of a CdTe based device, detailed study of conduction mechanism and current limiting parameters, which decides device efficiency, is needed.

Electrical properties of the vacuum deposited II-VI compound thin films depend on the composition and structure of the films. Both ZnSe and CdTe layers used for forming heterojunctions were not intentionally doped with impurities and they were not chemically or thermally treated. Such films deposited on unheated substrates had

very high electrical resistance due to self-compensating property inherited by these compounds [Rusu and Rusu 2000, Gowrish Rao et al. 2013]. Fig. 5.4.1 shows the I-V curves of p-CdTe/n-ZnSe heterojunction. The heterojunction shows the rectifying behavior, which is typical to p-n junction diode. Assuming that the conduction occurs mainly due to the TED, which is typical to heterojunctions, the forward current varies with the voltage according to the Eq. 5.1.

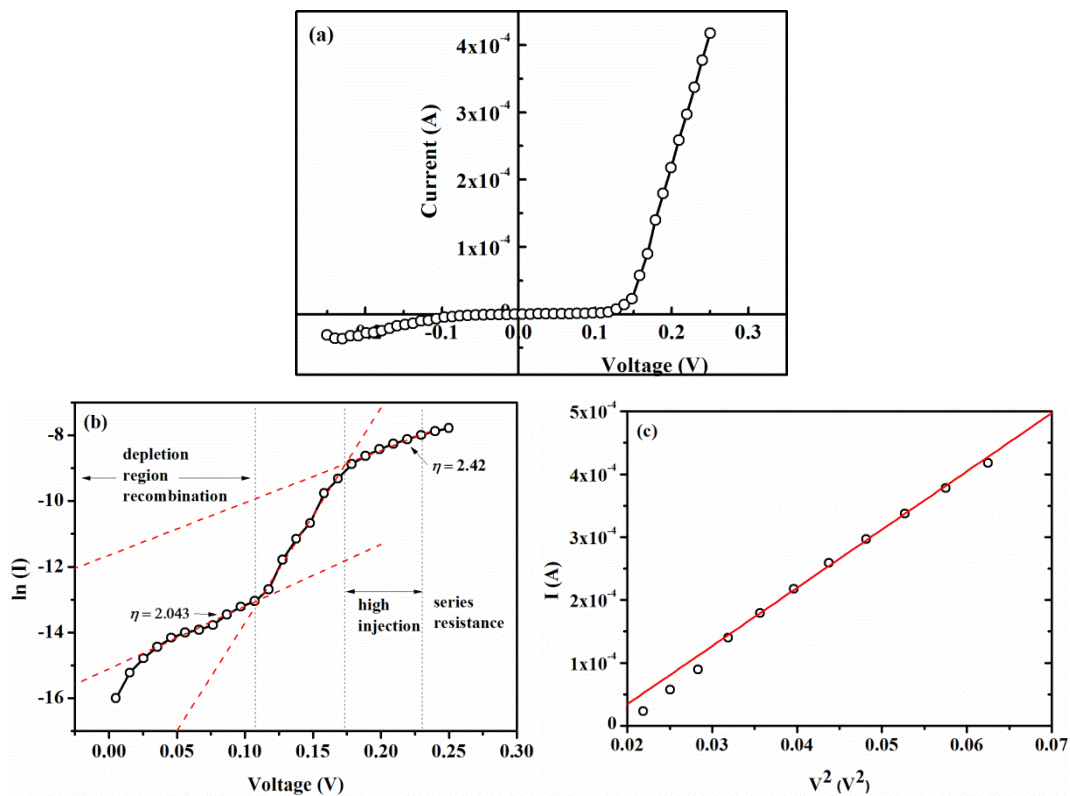


Fig. 5.4.1: (a) I-V characteristic (b) $\ln I$ vs. V and (c) I vs. V^2 curve of n-ZnSe/p-CdTe heterojunction

To analyze the conduction mechanism involved in the heterojunction the I-V characteristic was plotted in a semi logarithmic scale as shown in Fig. 5.4.1(b). The slope of the curve gives the ideality factor n ; it can vary from 1 to 2 or above, depending on the conduction mechanism involved. Fig. 5.4.1(b) shows the different regions corresponding to different values of n . In the first part, up to 0.1V, $n \cong 2$ indicates dominance of trap-assisted generation recombination current in the depletion region. In the second region, spanning from voltage 0.1 to 0.17, $n \cong 1$ implies ideal diode current in this region. Beyond 0.17 V, the ideality factor $n > 2$ suggests that

conduction mechanism is other than diffusion or recombination current. High injection and series resistance may limit the current in this region. Eq. 5.3 can approximate the linear dependence of the I-V characteristic at higher forward voltages. R_s is estimated from the inverse of the slope of the higher forward bias, which was $\sim 253\Omega$. Fig. 5.4.1(c), plot of I vs. V^2 , drawn for higher bias voltage, was found to make a better linear fit corresponding to the shallow trap square law, characteristic of space charge limited conduction, given by Eq. 5.4.

In order to determine the barrier height, the p-CdTe/n-ZnSe interface is characterized with C-V. Fig. 5.4.2(a) and 5.4.2(b) show the voltage dependence of the capacitance and inverse square of the capacitance of the heterojunction, respectively, measured at 100 kHz and 2 MHz signal frequency. In an ideal abrupt junction, the capacitance should decrease with increasing reverse voltage due to the increase in depletion width with voltage and it should be independent of frequency. C^{-2} versus V curve should be a straight line given by the Eq. 5.5. Slope of C^{-2} versus V is commonly used to determine the carrier density or doping density and intercept at C^{-2} is zero to find V_b of the junction. As can be seen from the Fig 5.4.2(a) C-V does depend on the frequency, indicating the presence of electrically active traps at interface [Hoffman et al. 2001]. The voltage intercept of the $C^{-2}(V)$ in Fig. 5.4.2(b) is also too large to consider as built-in potential. This indicates the presence of an insulating layer at the interface, formed due to inter-diffusion of components [Buch et al. 1977, Mauk et al. 1990]. In such cases, the built-in potential can be calculated from Eq. 5.6

$$qV_{bi} = E_g - E_f(CdTe) - E_f(ZnSe) - \Delta E_c \quad (5.6)$$

where E_g is the energy band gap of CdTe, $E_f(CdTe)$ and $E_f(ZnSe)$ are Fermi levels in respective compounds, ΔE_c is the energy difference between conduction bands of CdTe and ZnSe. The qV_{bi} was found to be ~ 0.9 eV.

Based on the results of the electrical characterization, a band profile for p- CdTe/n- ZnSe heterojunction is drawn, as shown in Fig. 5.4.3, using electron affinity rule. The band alignment shows the conduction band offset, ΔE_c , is 0.19 eV and valence band

offset, ΔE_v , is 1.12 eV. The junction offers small barrier for electrons and large barrier for holes, hence blocking from crossing junction. Thus, while compared to CdS/CdTe, the band offset of CdTe/ZnSe favors the higher conversion efficiency.

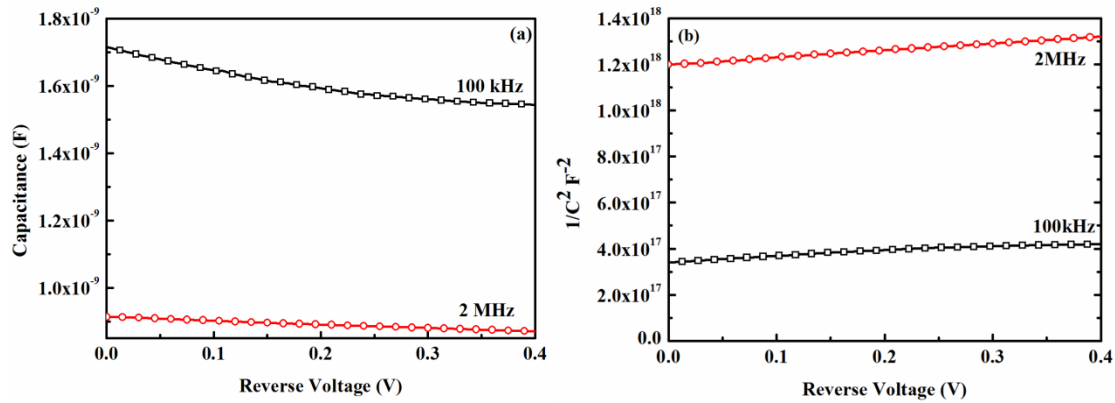


Fig. 5.4.2: (a) Junction capacitance and (b) C^{-2} as function of voltage of n-ZnSe/ p- CdTe heterojunction

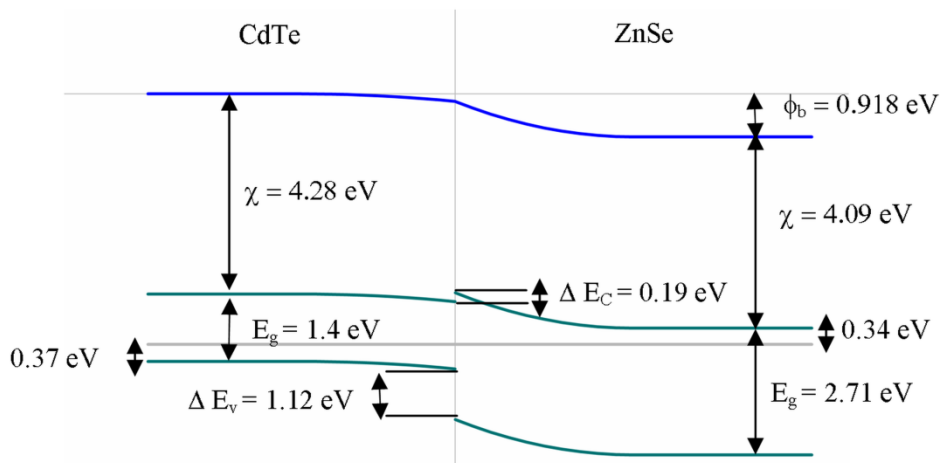


Fig. 5.4.3: Band profile of p-CdTe/n-ZnSe heterojunction

5.5 n-CdSe/p-ZnTe HETEROJUNCTIONS

CdSe/ZnTe heterojunction caught the attention of researchers in optoelectronic field such as LEDs, Laser diodes and solar cells owing to their small lattice mismatch [Samarth et al. 1989], direct band gap and high absorption coefficient of both materials involved in visible region [Fahrenbruch 1977, Chu and Chu 1995]. Further, CdSe/ZnTe heterojunction is a type-II heterojunction, where the conduction and valence band edges of one material is lower than the corresponding band edges of other material [Milnes and Feucht 1972]. This feature of the heterojunction enhances

the spatial separation of photo-generated charge carriers, which makes the junction very attractive for photovoltaic applications [Lo et al. 2011, Wang et al. 2014]. The earlier studies of making use of these properties were on bulk devices and hetero-epitaxial grown devices [Gashin and Simashkevich 1973a, 1973b, Buch et al. 1976], using close space vapor transport [Buch et al. 1977b], semi close space technique [Bakr and Feodrov 1994], hot-wall vacuum evaporation [Pal et al. 1990] and thermal evaporation [Patel et al. 1994]. These studies were focused on growth and the photoelectric properties of the heterojunctions. The green LED application of this heterojunction is also explored by charge carrier injection into ZnTe layer [Phillips et al. 1992, Wang et al. 1993]. However, the efficiency of these heterojunctions was low compared to the CdTe based cells. On the other hand, couple of simulation works suggest that CdSe/ZnTe junctions can be used in tandem to the high efficiency CdTe or CIGS cells [Mahawela et al. 2005, Xiao et al. 2010]. This may further extend the efficiency of CdTe and CIGS cells.

Fig. 5.5.1(a) shows the room temperature I-V characteristics for n-CdSe/ p-ZnTe heterojunction. The heterojunction shows the rectifying behavior with rectification ratio 9.05 at ± 0.5 V. To understand the conduction mechanism in CdSe/ZnTe heterojunction, I-V of the diode is analyzed using TED model given by Eq. 5.1. I-V curve was fitted to this model by plotting it as shown in Fig. 5.5.1(b). The saturation current and ideality factors extracted from the intercept and the slope of semi-log plot of the forward I-V are found to be $0.43 \mu\text{A}$ and 3.34, respectively. Fig. 5.5.1(c) shows temperature dependence of I-V characteristics of the heterojunction. I-V measurements were taken at different temperatures from 303 K to 373 K for each 5 K increase in temperature. The variation of I_s with inverse temperature (Richardson's plot) was plotted as shown in Fig. 5.5.1(d), and used to determine the barrier height, ϕ_b , of the n-CdSe/ p-ZnTe interface. A value of 0.36 eV for ϕ_b was obtained from the slope of the Richardson's plot. In principle, the ideality factor varies from 1 to 2, implying either diffusion or recombination dominated phenomena and at intermediate values combination of both. Larger value of n also indicates large series resistance and that the current conduction is controlled by some other mechanism [Jeong et al. 2011].

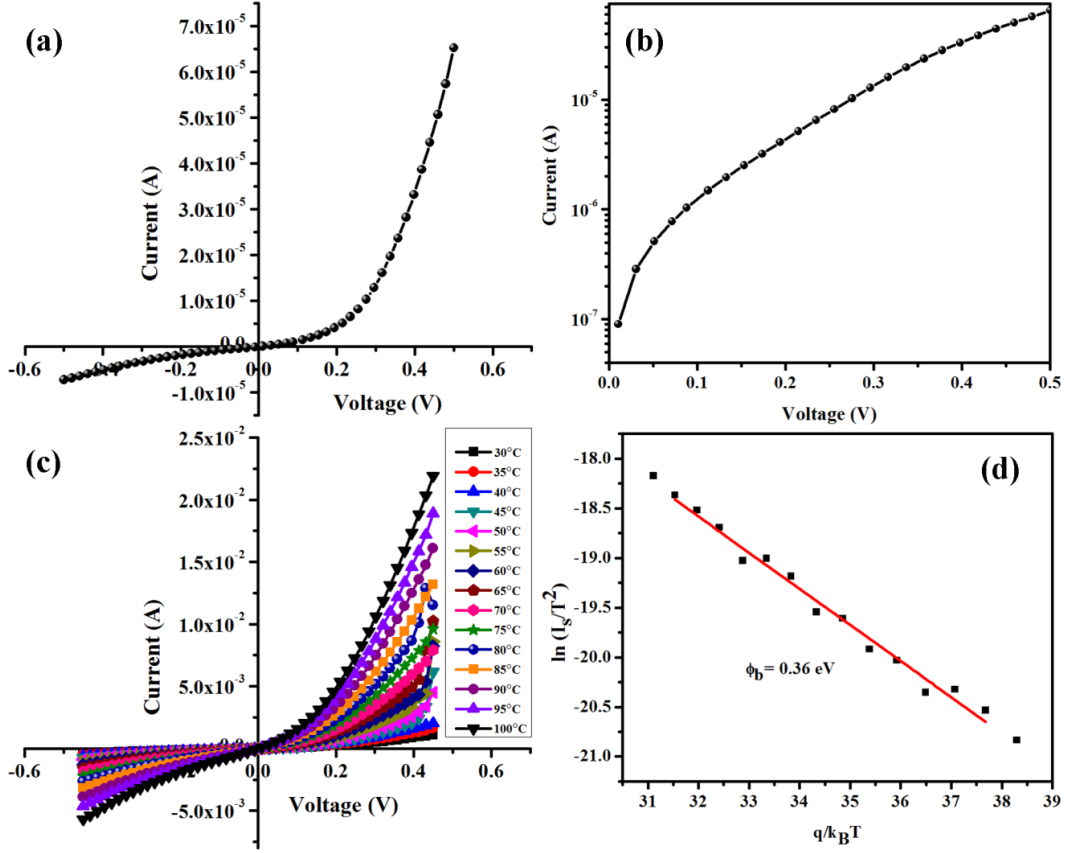


Fig. 5.5.1: (a) I-V curve of n-CdSe/ p-ZnTe diode (b) the variation of $\ln I$ with voltage, (c) temperature dependence of I-V and (d) Richardson's plot.

I-V curve indicates that series (R_s) and shunt (R_{sh}) resistance affect the current. The values of R_s and R_{sh} are commonly extracted by fitting the I-V curve to equivalent circuit models represented by Eq. 5.3 incorporating resistors in series and parallel to the diode [Pallarès et al. 2006, Macabebe et al. 2008]. According to that, shunt leakage current shows ohmic behavior, but it is often found that shunt leakage current is non-linear [Breitenstein et al. 2004, McMahon et al. 2005, Alonso-García and Ruíz 2006, Kunz et al. 2009, Dongaonkar et al. 2010] and also leakage current is symmetric about $V=0V$. The non-linear behavior of shunt current at reverse and low forward biases is found to be due to the space charge limited conduction (SCL) i.e.,

$$I_{sh} = G_{0,sh}V + I_{0,sh}V^{n_{sh}} \quad (5.7)$$

where $I_{0,sh}$ is SCL current magnitude, n_{sh} is the shunt current power exponent and $G_{o,sh}$ is the constant conductance component at low biases.

The symmetry feature of the shunt current was utilized to subtract it from total diode current and also fitted using PV analyzer to extract the diode parameters [Dongaonkar 2014]. Fig. 5.5.2 shows the fitted forward current and the extracted parameter is given in Table 5.5.1. The graph shows measured forward curve (red square symbol) which is clearly higher than the actual junction current (blue solid line), after subtraction of shunt contribution (dashed lines) to diode current. Further, the values of the R_s and R_{sh} were derived by plotting junction resistance (R_j) or dV/dI verses voltage as shown in Fig. 5.5.3. The values conform to those obtained by fitting to equivalent circuit model represented by Eq. 5.3 and 5.7.

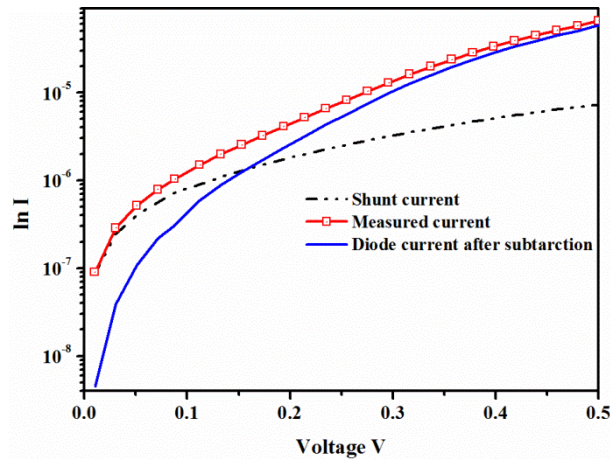


Fig. 5.5.2: Forward I-V curve fitted using model given in [Dongaonkar 2014]

Table 5.5.1: Extracted diode parameters using equivalent circuit model

R_s	I_{0sh}	n_{sh}	G_{sh}
(Ω)	(A)		(S)
2088.96	2.1455×10^{-05}	2.65387	7.88799×10^{-06}

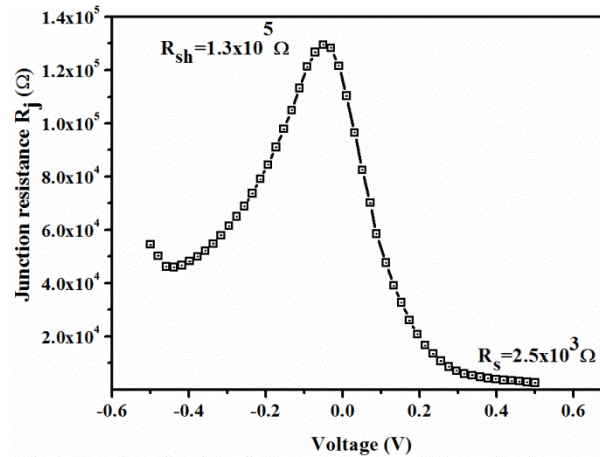


Fig. 5.5.3: Variation of junction resistance with bias voltage

In an alternative analysis, the I-V characteristic of the diode is plotted in log-log scale as shown in Fig. 5.5.4(a), as opposed to semi-log scale used in earlier analysis. The curves show better fit to the power law model ($I \propto V^m$) rather than the exponential model described above. In addition, it shows two regions belonging to different conduction regimes. At voltages lower than 0.1 V, power $m=1$ which is corresponding to ohmic behavior and at voltages above 0.1 V, $m=2$ indicating that current in this range of bias is limited by space charges [Rose 1955]. Eq. 5.4 can give the temperature dependence of the SCLC regime of dark I-V. The values of N_t and E_t values can be determined by plotting current as a function of temperature at a constant potential as shown in Fig. 5.5.4(b). The measurement was done keeping voltage constant at 0.3 V. The $\ln I$ vs. temperature shows linear dependence and $E_t = 0.4$ eV and $N_t = 6.54 \times 10^{15} \text{ cm}^{-3}$ were calculated from the slope and intercept of the graph, respectively. Thus current in reverse and lower forward bias is severely affected by non-linear SCL current. The origin of shunt leakage current can be attributed to the defects present in the bulk and at the interface of the junction. High resistance of bulk and contact barrier may be the reason for observed high series resistance.

Fig. 5.5.5(a) shows the C-V and admittance characteristics of the CdSe/ZnTe heterojunction. It can be noted that the barrier height of 0.7 eV measured from the C-V is higher than that computed from the I-V characteristics. This can be attributed to the presence of interface states and bulk states contributing to the measured capacitance

and hence, the measured barrier height. The presence of the defect state is evident from the frequency dependence of the measured C-V [Hoffman et al. 2001].

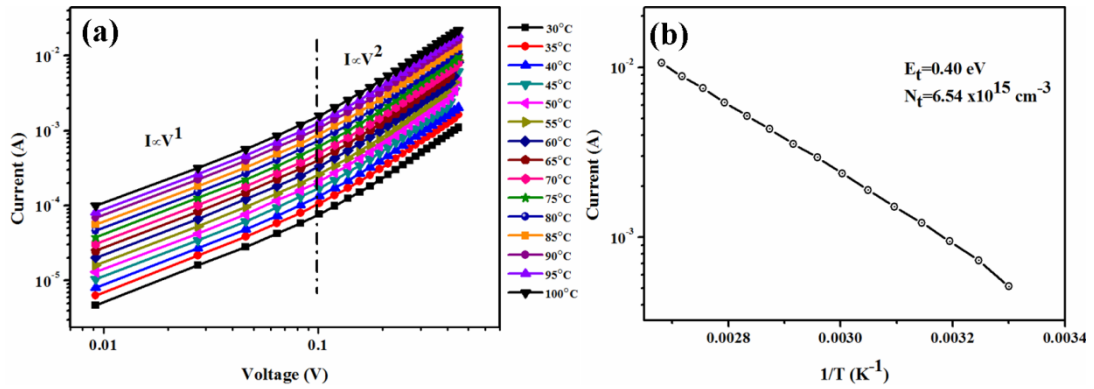


Fig. 5.5.4: (a) Plot log I vs. log V and (b) variation of current with temperature

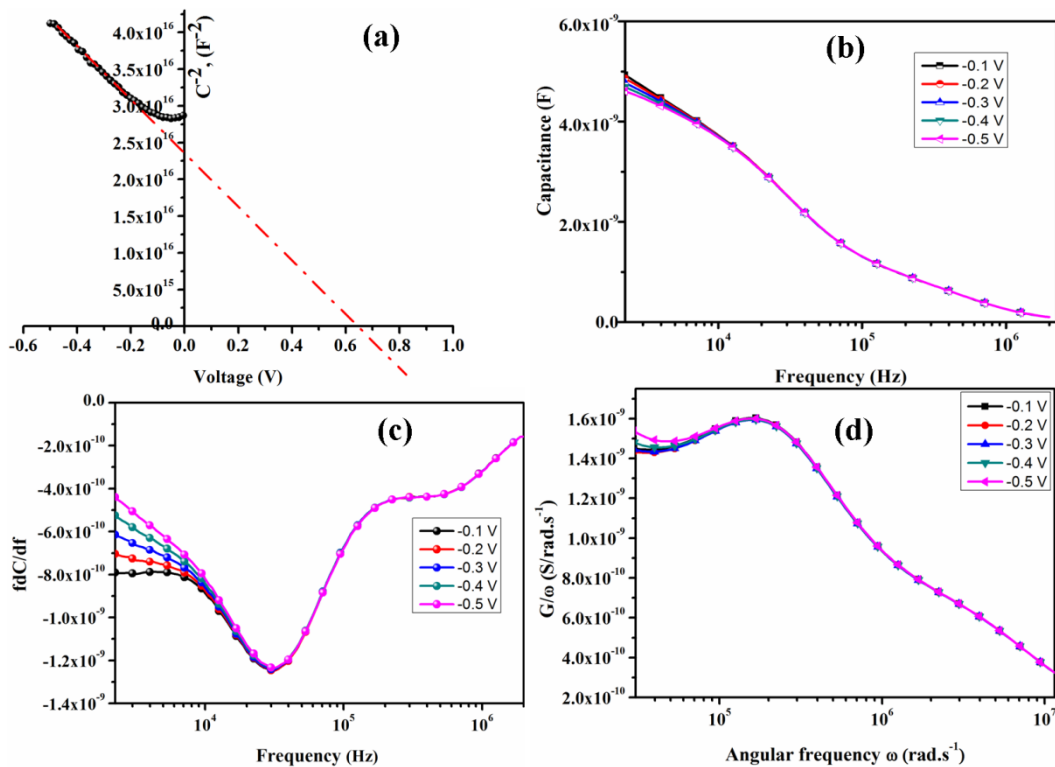


Fig. 5.5.5: Junction capacitance of CdSe/ ZnTe heterojunction: (a) C^{-2} as function of voltage, (b) capacitance, (c) differential capacitance as function of frequency and (d) conductance as function angular frequency.

Also, the admittance measurements, where the capacitance and conductance as function of frequency, showing an inflection and a peak are shown in Fig. 5.5.5(b) and 5.5.5(d), respectively [Oldham and Naik 1972, Losee 1975, Pautrat et al. 1980]. The differential capacitance as a function of frequency shown in Fig. 5.5.5(c) reveals two peak in measured range. In order to distinguish between the bulk and interface defects C-f measurements were done at different bias voltages. The stronger peak may be arising from the bulk defect state as it is independent of the bias voltage [Herberholz et al. 1998, Kneisel et al. 2000]. A weak peak at higher frequency implies the presence of the Schottky barrier contact [Li et al. 2010]. These results are in line with the above analysis of I-V characteristics.

5.6 CdTe/Si HETEROJUNCTIONS

CdTe/Si heterostructures are being studied for their detector applications, particularly for room temperature X-ray, γ -ray detectors and as hybrid substrates for the growth of HgCdTe based infrared detectors [Reynolds 1989, Ashokan and Sivananthan 1999, Rogalski 2012]. The advantage of Si as substrate for these applications is possibility of large area detector array and easy integration with Si based readout circuits. Further, low cost in comparison to other substrates such as Ge and sapphire, earth abundant material, mechanical strength, and good thermal conductivity has motivated to use Si as substrate despite of large lattice mismatch between Si and CdTe [Ashokan and Sivananthan 1999, Rogalski 2003, 2007, 2011]. The large lattice mismatch will lead to large defect density in CdTe and hence in HgCdTe detector, which is deposited on these composite substrates. The high defect density leads to low performance of the detectors. These problems were circumvented by in situ cyclic annealing, using interfacial layer such ZnTe, and using different orientation substrates, which reduced the defect density significantly in CdTe on Si [Smith et al. 2000].

The success of II-VI alloys grown on CdTe/Si heterostructures in IR detectors and imaging sensor has influenced its use in high efficiency multi-junction solar cells. Currently, multi-junction or tandem solar cell based on III-V compounds and their alloys grown on germanium has the highest efficiency. However, they are very costly

and not as efficient as expected. Hence, efforts were focused on replacing Ge with lower cost Si and borrowing IR detector technology. Recently, Carmody [2010] and his group have reported photovoltaic properties of epitaxially grown n-type CdTe and its related compounds such as CdZnTe on p-Si wafer [Carmody et al. 2010, Xu et al. 2010]. These devices fabricated using MBE technique, had lower defect density in comparison to commonly used growth technique for thin film PV cell fabrications. Thus, cost of fabrication is on the higher side; yet, the results provided insight on defects and grain boundaries that do not exist in crystalline films and only manifest in polycrystalline films, which affect the device performance.

However, the MBE grown crystalline CdTe based monolithic multijunction structures are still costly and involves complex process in comparison to the processing of polycrystalline CdTe devices. On the other hand, the heterojunctions formed with compound semiconductors are being studied in order to take the advantage of band offsets at the hetero-interface and properties of the Si for device performance, which can reduce the cost [Hotový et al. 2010, Avasthi et al. 2013, Hsu et al. 2013, Mondal et al. 2013, Liu et al. 2014]. The required band alignment can be attained by choosing suitable material from wide range of compounds. Depending on band offset at the interface sometimes, only one type of carrier will cross the interface while other type will see a large barrier for its flow and hence it will be blocked. This kind of structure can spatially separate charge carriers and avoid undesirable recombination.

The experimental results on these structures and on polycrystalline CdTe based solar cells are guide to achieve high open circuit voltage and high fill factors for required high efficiency. Doping (i.e., N_A-N_D or N_D-N_A) absorber materials improves built-in-voltage and the open circuit voltage, but excess doping will reduces fill factors faster than the increase in open circuit voltage [Kanevce and Gessert 2011]. The reduction in fill factor is due to reduction in depletion region width (in case of Cu doped CdTe, where excess Cu diffusing into CdS). For detector application, the resistivity of the CdTe should be high ($>10^9 \Omega\text{-cm}$) to reduce dark current and device noise and mobility-lifetime product for photo-generated carriers so that it can reach the electrodes before getting lost through recombination. These semi-insulating CdTe

are obtained via doping with deep donors or acceptors such as Ge and Sn [Panchuk et al. 1999, Fiederle et al. 2004, Babentsov et al. 2007, 2008]. However, high resistive CdTe were often obtained via doping with shallow donors such as In, Al and Cl [Eiche et al. 1993, Fiederle et al. 2003, Xu et al. 2009]. These dopants are usually expected to improve the n-type conductivity of CdTe. The interaction of shallow dopants and native defect in the materials give rise to high resistivity [Biswas and Du 2012]. Hence, the control of native defects and dopants is desirable to attain required conductivity.

In the present study, CdTe/Si heterojunction was fabricated by thermal evaporation of CdTe on Si substrate. Prior to the deposition, Si was dipped in 1% HF solution for 2 minutes followed by ultrasonication in isopropyl alcohol and acetone for 15 minutes each. As deposited CdTe has very high resistivity, use of such films in device will lead to poor performance. In order to improve the conductivity of the CdTe, films were doped with In for n-type conductivity and excess of tellurium (Te) for p-type conductivity. Two different types of heterojunctions, In doped n-CdTe films on p-Si and CdTe having excess Te with n-type Si were formed to study the effect of doping on electrical transport in CdTe/Si heterojunction. The charge carrier concentration influences the field distribution in junction and barrier at interface. This can be seen in Fig. 5.6.1, representing the band diagram of these two type of heterojunctions.

The band profile was constructed based on Anderson model. Using this model the conduction band offset ΔE_c and valance band offset ΔE_v were calculated from the difference between the electron affinities of Si and CdTe, $\chi_{si} = 4.05$ eV and $\chi_{CdTe} = 4.28$ eV. The values of electron affinities were taken from previously published literature. The band gap of the CdTe was obtained from optical characterization, which is approximately 1.47 eV. The carrier density of both n and p type Si wafers were calculated from the resistivity of the particular wafers. Carrier density of p-type Si was around $1.47 \times 10^{16} \text{ cm}^{-3}$ and for n-type Si $4.83 \times 10^{15} \text{ cm}^{-3}$. The carrier concentration of the p-CdTe (2.5 wt% excess Te) was $8.13 \times 10^{14} \text{ cm}^{-3}$ and in n-type CdTe (2.5 wt% In) was $1.15 \times 10^{15} \text{ cm}^{-3}$ determined using Hall measurement. The carrier concentration and carrier type made the impact on the band profile, which can be seen in Fig. 5.6.1. In n-CdTe/p-Si (Fig. 5.6.1 (a)), the conduction or valance band

does not show spiked barrier for the flow of electrons or hole across the barrier. However, p-CdTe/n-Si (Fig. 5.6.1 (b)) has spiked barrier for both hole and electron that may affect the transport of the carriers across the interface. The band bending is seen in CdTe with minimum bending on Si side because of lower carrier concentration in comparison to Si in both cases. Thus, the depletion region extends more into CdTe rather than into Si. The small signal capacitance studies of these kinds of structures reveal more about the CdTe property such as carrier concentration and defect states in the band gap and at CdTe/Si interface.

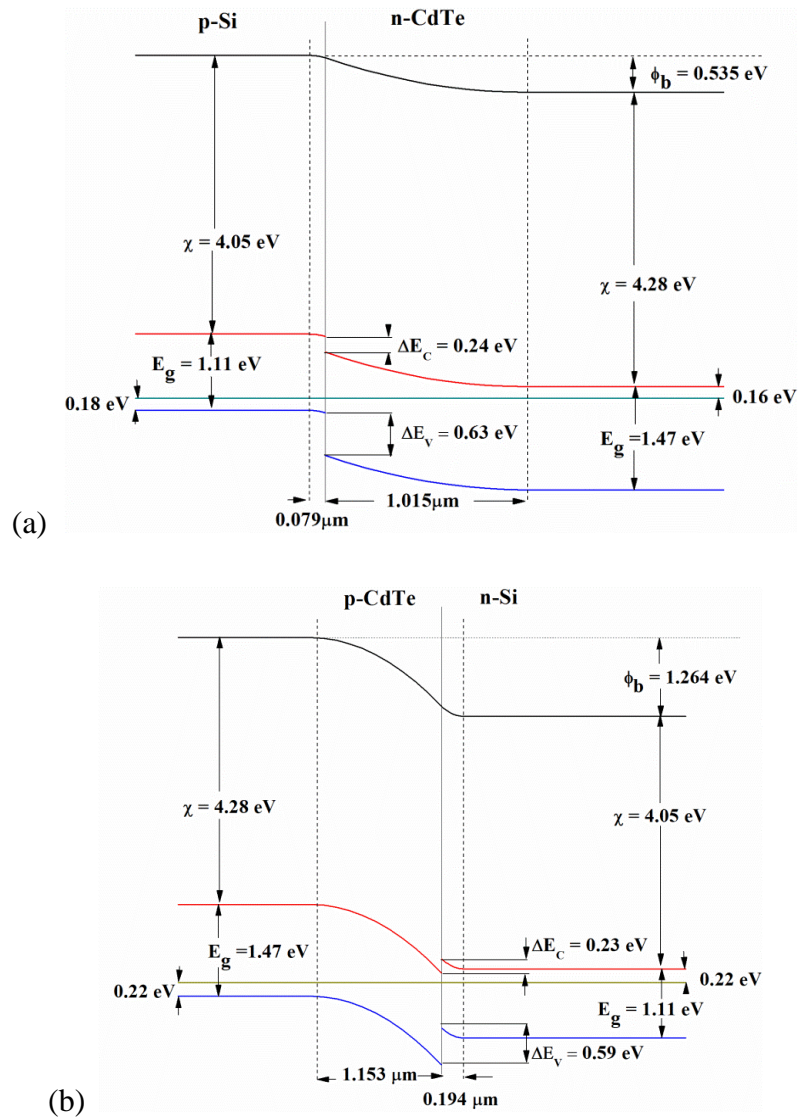


Fig. 5.6.1: Representation of band diagram of (a) n-CdTe/p-Si and (b) p-CdTe/n-Si heterojunctions

In order to elucidate the effect of In and excess Te concentration in CdTe on properties of heterojunction C-V characterization of both n-CdTe/p-Si and p-CdTe/n-Si was carried out. The as-deposited samples doped with In n-CdTe/p-Si and Te excess p-CdTe/n-Si did not show any variation with applied bias voltage. The dependence of slope of Schottky-Mott plot on In in n-CdTe/p-Si and excess Te in p-CdTe/n-Si for samples annealed at 300 °C for 2 hours is shown in Fig. 5.6.2 and 5.6.3, respectively. The carrier density, built-in potential, and depletion layer width derived from these plots is given in Table 5.6.1 and 5.6.2. For the case of In doped CdTe, the slope of the curve has decreased with increase in In concentration. The slope is inversely proportional to the carrier density at the edge of depletion region. The carrier densities in CdTe were determined (in Table 5.6.1) using Schottky-Mott relation (Eq. 5.5) also found to increase with increase in In concentration. Similar trend was observed in the case of Te excess – p-CdTe/n-Si heterojunction (Fig. 5.6.3 and Table 5.6.2)

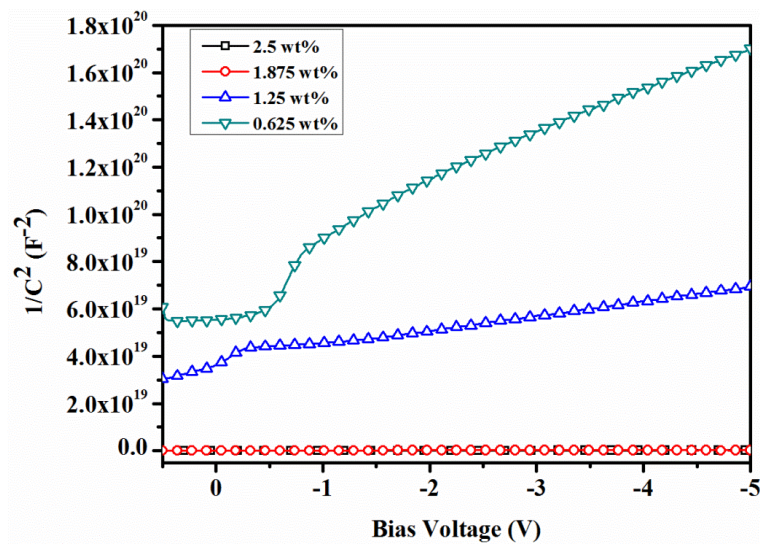


Fig. 5.6.2: Schottky-Mott plot of n-CdTe/p-Si heterojunction with different In wt% in n-CdTe

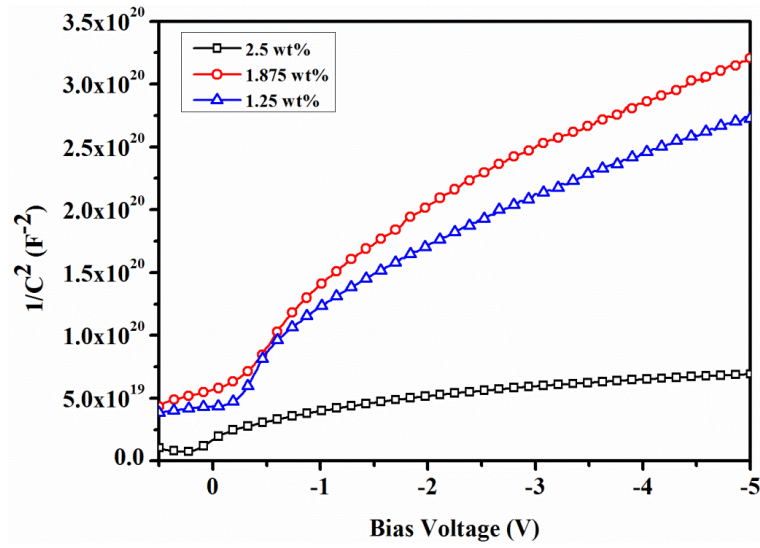


Fig. 5.6.3: Schottky-Mott plot of p-CdTe/n-Si heterojunction with different Te wt% in p-CdTe

Table 5.6.1: Carrier density, built-in potential, and depletion layer width in n-CdTe/p-Si heterojunction for different In wt% (annealed at 300 °C for 2 hours)

In (wt %)	n (cm ⁻³)	V _b (V)	W (m)
2.5	2.05x10 ¹⁷	0.296	4.58x10 ⁻⁸
1.875	6.53x10 ¹⁶	0.201	8.79x10 ⁻⁸
1.25	5.41x10 ¹⁴	1.401	5.39x10 ⁻⁸
0.625	1.66x10 ¹⁴	0.183	2.11x10 ⁻⁶

Table 5.6.2: Carrier density, built-in potential, and depletion layer width in p-CdTe/n-Si heterojunction for different excess Te wt% (annealed at 300 °C for 2 hours)

Te (wt %)	p (cm ⁻³)	V _b (V)	W (m)
2.5	7.89x10 ¹⁴	1.23	1.16x10 ⁻⁶
1.875	2.45x10 ¹⁴	1.53	2.13x10 ⁻⁶
1.25	2.60x10 ¹⁴	1.26	1.87x10 ⁻⁶

In both cases, the curve has shown deviation from linearity, which would be found in ideal conditions. The curves in both plots have multiple slopes at different bias voltage regions indicating the presence of mid-gap trap states on CdTe side. Many researchers have reported presence of large defect density at CdTe/Si interface in

previous work on this system [Smith et al. 2000, Chen et al. 2008, Rogalski 2011]. This may be attributed to the large lattice mismatch between CdTe and Si. Evaporated films will also usually have a large number of point defects, which may manifest as deep levels in band gap. In reverse bias condition, the band bending will be larger, as more number of deep levels fall below Fermi level in depletion region. This when occupied by the carriers will contribute to the space charge just the same way as shallow donor or acceptors. This in turn contributes the carrier density more than the actual. The factors affecting the C-V measurements and behavior exhibited in many practical heterojunctions is represented in Fig. 5.6.4. Arrow 1 shows the effect of voltage sharing by the back contact under forward biases. Arrow 2 shows the effect of the static response of the deep levels. Arrow 3 shows the effect of punch-through under reverse biases [Li et al. 2012]. Hence, it is assumed that similar factors are affecting the heterojunctions in present study.

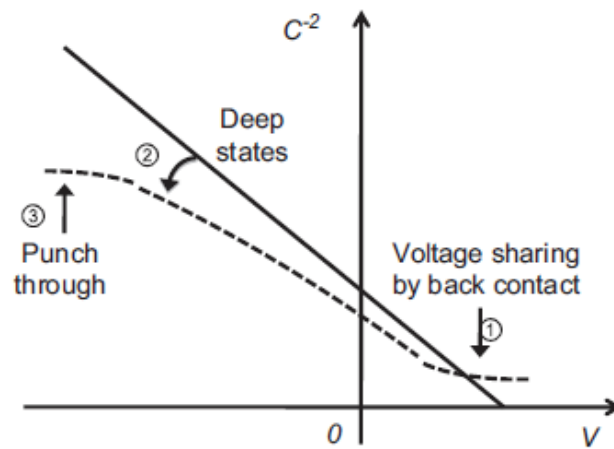


Fig. 5.6.4: Mott–Schottky plot of a fictitious device with uniform carrier density N_a . The solid line represents the ideal case in the CV analysis. The dashed line represents the non-ideal case with factors affecting the capacitance at different voltages [Li et al. 2012].

The carrier density in junction determines the depletion layer width and built-in potential. In p-CdTe, the carrier concentration did not vary much with the Te content, so is built-in potential and depletion layer width (Table 5.6.2). It can also be noted that, the values obtained by the Schottky-Mott analysis match with that of band

profile given in Fig. 5.6.1(b). The carrier concentration has shown drastic variation in n-CdTe/p-Si with In content in n-CdTe. However, depletion layer width was large for only lowest In content and it is closer to CdTe layer thickness. That implies the 0.625 wt% In CdTe is fully depleted. The electrical resistivity measurement (in chapter 4) has also shown that these films were highly resistive in comparison to higher In content films. The depletion layer width in higher In content (1.25 to 2.5 wt %) is much smaller than the expected values, which may be due to the contribution from trap states in addition to charge carriers to the capacitance measurements.

Further, to analyze the interface properties of the CdTe/Si heterojunctions, C-V measurements were done as a function of frequency. The frequency dependence of the C-V for n-CdTe/p-Si and p-CdTe/p-Si heterojunction is shown in Fig 5.6.5 and Fig 5.6.6. The C-V characteristic should not be frequency dependent if the heterojunction is abrupt and free from traps at the interface. In the presence of interface traps and series resistance, C-V characteristic will show a peak [Nicollian and Goetzberger 1965, Castagné and Vapaille 1971, Kar and Varma 1985]. The peak position and amplitude depend on interface state density, series resistance, and doping concentration. These factors make capacitance frequency dependent. If the resistivity of the semiconductor is high then the dielectric relaxation frequency falls within the commonly used measurement frequency range. Along with dielectric relaxation, the trapping and de-trapping process of electrons, which responds to the lower measuring frequency, contributes to the capacitance measured at lower frequency.

The capacitance measurement as a function of frequency often exhibits inflection point in capacitance at a specific frequency. The inflection in capacitance may be indication of dielectric relaxation in high resistance materials or freeze-out of trap level contributing the capacitance just below this point. As seen above, the frequency dependence of C-V characteristics is clear indication of presence of such factors. Fig. 5.6.7 shows capacitance as a function of frequency in a range of 20 to 2M Hz for both n-CdTe/p-Si and p-CdTe/n-Si heterojunctions. It can be noted that in Fig. 5.6.7(b) plots showing inflection points at test signal frequency around 100 Hz. At higher frequencies in Te doped p-CdTe/n-Si, capacitance for all samples becomes independent of frequency reaching a constant value i.e. geometric capacitance for the

samples. The geometric capacitance arises from the bulk of the CdTe and depends on the thickness of the CdTe layer, as it may be completely depleted. Hence, in the case of Te doped CdTe dielectric relaxation is playing a role in capacitance measurement. In n-CdTe, as shown in Fig. 5.6.7(a), the capacitance as a function of frequency has shown different trend indicating that trap state in band gap may be contributing to the measurement.

The analysis of junction capacitance as function of voltage and frequency indicated that the depletion region is mostly spread on CdTe side in both n-CdTe/p-Si and p-CdTe/n-Si with minimum band bending on Si side. The junctions consist of large number of defects on CdTe side giving rise to trap states in CdTe band gap.

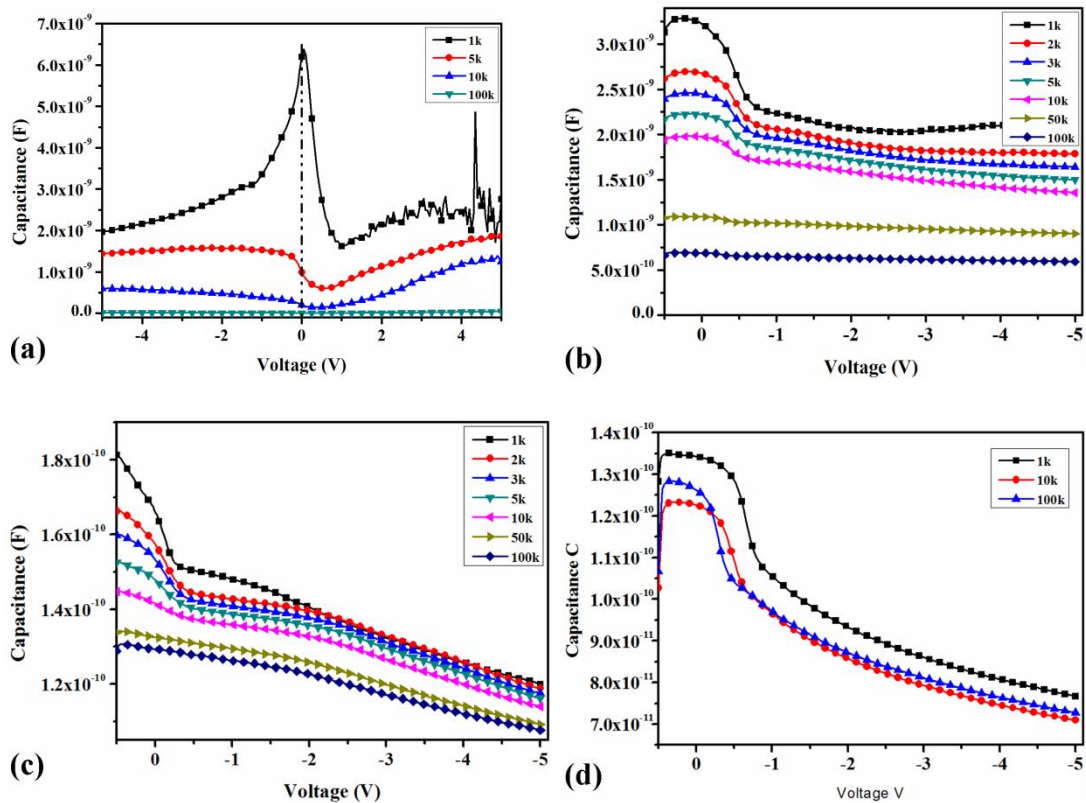


Fig. 5.6.5: Frequency dependency of C-V curve for n-CdTe/p-Si heterojunction with In content (a) 2.5 wt%, (b) 1.875 wt%, (c) 1.25 wt% and (d) 0.625 wt%

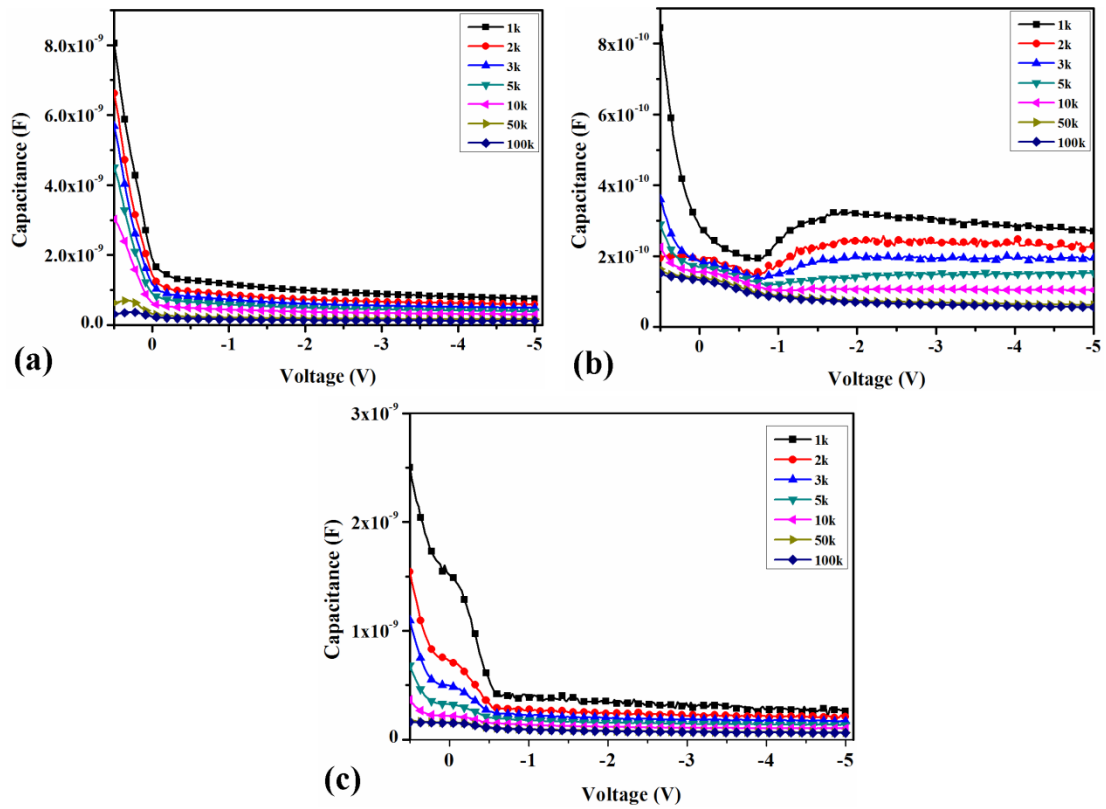


Fig. 5.6.6: Frequency dependency of C-V curve for p-CdTe/n-Si heterojunction with Te content (a) 2.5 wt%, (b) 1.875 wt% and (c) 1.25 wt%

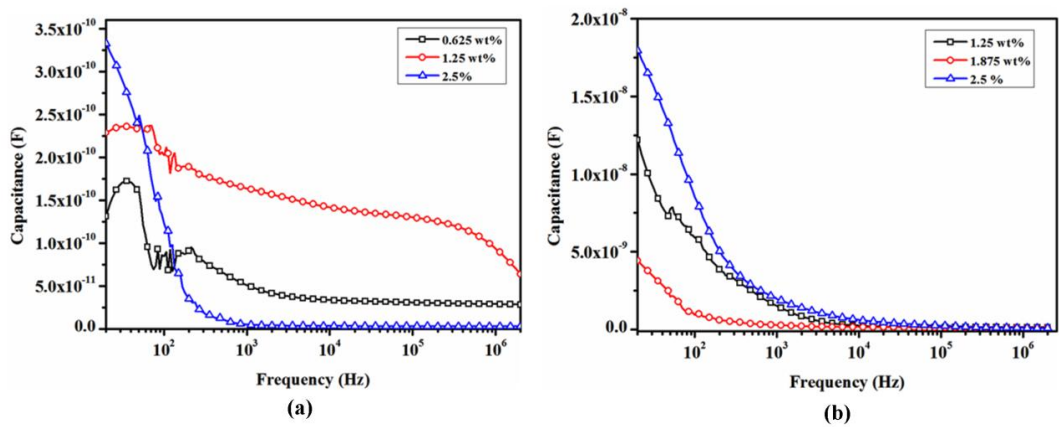


Fig. 5.6.7: Capacitance as a function of frequency for (a) n-CdTe/p-Si heterojunctions for different In content and (b) p-CdTe/n-Si heterojunction with different Te content.

In order to understand the conduction mechanism in n-CdTe/p-Si and p-CdTe/n-Si heterojunctions, dark current-voltage behavior of the junctions were studied. The I-V

characteristics of In doped n-CdTe/p-Si heterojunction is shown in Fig. 5.6.8. Forward current has shown increase with increasing In content in annealed samples, while as-deposited samples show random trend for increase in indium content. This may be attributed to uniform distribution of dopants on annealing. These I-V curves were analyzed by fitting the plots to the model given in Eq. 5.1 based on the assumption that the “thermionic emission and diffusion” of the carrier is the underlying conduction mechanism. The ideality factor extracted from the slope of linear part in semi-log plot of I-V curve, would reveal the conduction mechanism in the junction under study. According to the thermionic emission diffusion model, the ideality factor should be close to one. However, the ideality factors extracted from the fitting of the curve were much larger than the expected values. Recombination current given by Shockley-Reed-Hall theory can also be ruled out as the ideality factor is >2 . The large defect density on CdTe side as seen from capacitance measurements may lead to the high values of ideality factor or may be indicating that conduction mechanism is other than the model given in Eq.5.1. Several other transport mechanisms may be present at the same time as found in earlier junctions. The dominance of those current depends on doping density on both side of the junction, defects in depletion region and the extra barriers due the band alignment at hetero-interface.

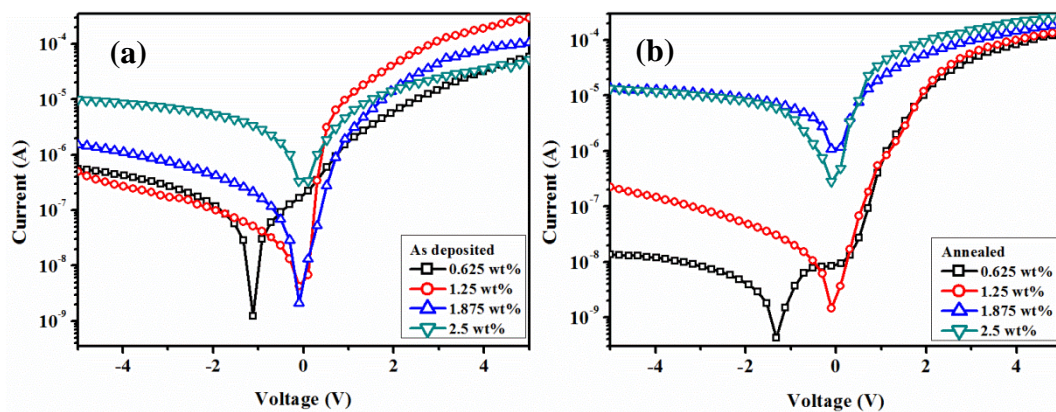


Fig. 5.6.8: I-V characteristics of (a) as-deposited and (b) annealed (at 300° C for 2 hours) n-CdTe/p-Si heterojunctions with different In content

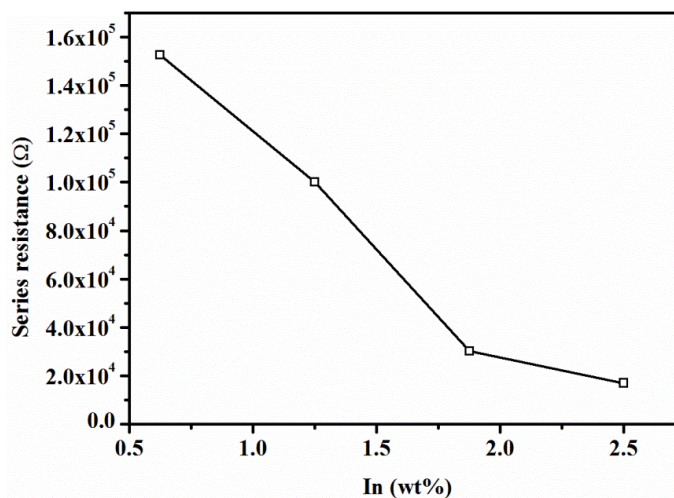


Fig. 5.6.9: Series resistance reduction with different In content for annealed (at 300° C for 2 hours) sample of n-CdTe/p-Si heterojunctions

At higher voltages (beyond 1.5 to 2V) in Fig. 5.6.8 (b), the series resistance was found to limit the current for all the samples. However, the series resistance was found to decrease with increasing In content as shown in Fig. 5.6.9. The dynamic junction resistance analysis for these heterojunction over a bias voltage range -5 to +5 V is shown in Fig. 5.6.10. These plots give further insight into conduction mechanism near low bias voltage. As seen from Fig. 5.6.10, the shunt resistance was found to decrease drastically with increasing In content leading to increase in leakage current in reverse bias condition. A spike-like feature of resistance near zero bias in Fig. 5.6.10 implies that the multi-tunneling-capture-emission through trap states near the interface may be controlling the current at lower bias voltages [Matsuura et al. 1984].

I-V characteristic of p-CdTe/n-Si is shown in Fig. 5.6.11. It can be seen from the current behavior that the series resistance affects at higher voltages (above 3V). The ideality factor of these diodes is also very high (> 2), thus the conduction mechanisms is controlled by neither thermionic emission diffusion current nor SRH generation recombination current. Other possible conduction mechanisms are band-to-band tunneling or multistep tunneling recombination [Ribben and Feucht 1966] or multistep tunneling capture emission [Matsuura et al. 1984]. For band-to-band, tunneling the carrier concentration density must be very high. Hence, multi-step tunneling through

defect states may be controlling the current in junction. The hump like feature near zero bias in Fig. 5.6.12 is also in line with argument of multi step tunneling mechanism through defect state across the interface regulate the current in these junctions.

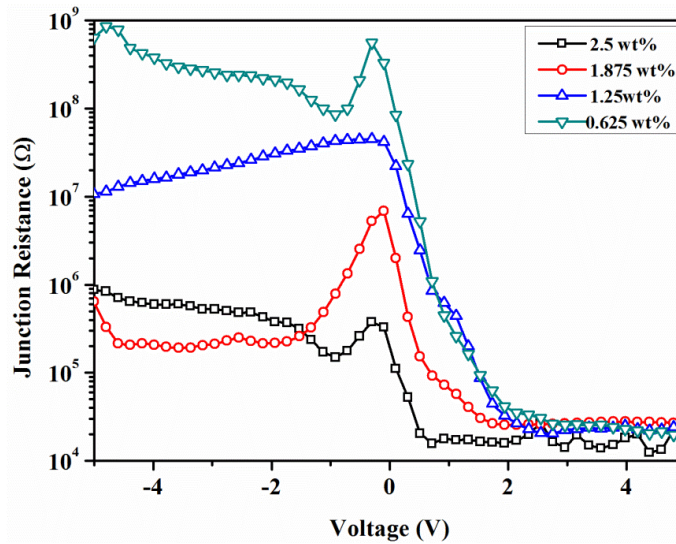


Fig. 5.6.10: Junction resistance as a function of bias voltage for annealed (at 300° C for 2 hours) samples of n-CdTe/p-Si heterojunctions with different In content

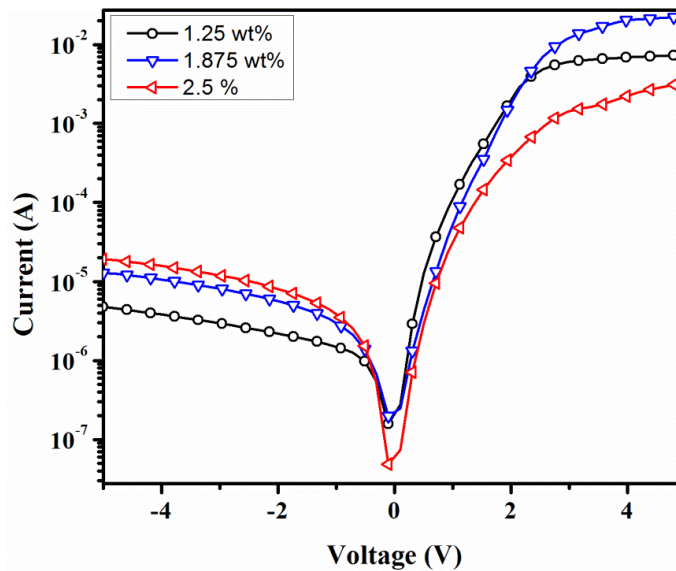


Fig. 5.6.11: I-V characteristics of annealed (at 300° C for 2 hours) p-CdTe/n-Si heterojunctions with different Te content

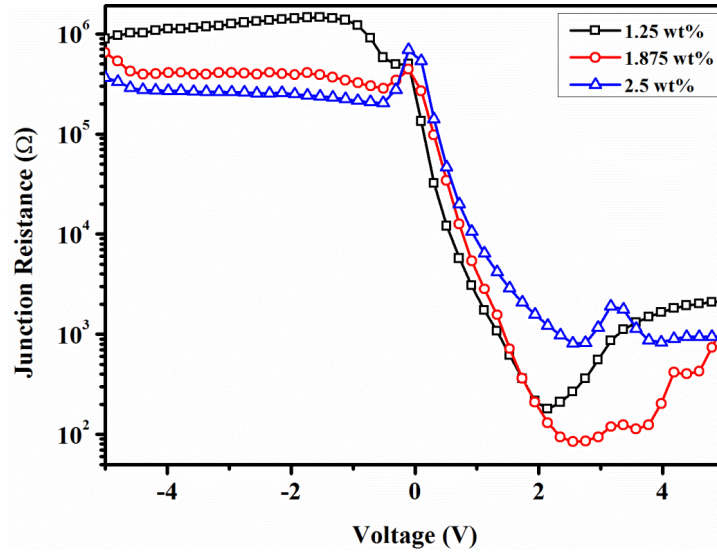


Fig. 5.6.12: Junction resistance as a function of bias voltage for annealed (at 300° C for 2 hours) samples of p-CdTe/n-Si heterojunctions with different Te content

5.7 CONCLUSIONS

Four different heterojunction, namely p-CdTe/n-ZnSe, n-CdSe/p-ZnTe, n-CdTe/p-Si, and p-CdTe/n-Si were fabricated using thermal evaporation method. The heterojunctions were evaluated through I-V and C-V measurements, as transport properties and interface properties such as barrier height and defect states of the heterojunctions play crucial role in deciding the device applicability. All the heterojunctions have shown rectifying nature as seen from the I-V characteristic.

Current conduction in p-CdTe/n-ZnSe was dominated by the trap-assisted recombination and high injection current as determined from ideality factors in diode equation used for fitting the measured I-V curves. Capacitance measurements revealed the presence of traps and insulating interfacial layer that controls the current transport across the junction. However, larger band gap of ZnSe and valence band offset are favorable for better performance.

I-V characteristics of n-CdSe/p-ZnTe heterojunction were analyzed with TED model and SCLC model. The barrier height of n-CdSe/p-ZnTe junction $\phi_b = 0.36$ eV and ideality factor $n = 3.34$ were obtained for the heterojunction. The higher ideality factor and lower Richardson's constant than the theoretically expected values suggest

the deviation of charge transport mechanism from TED model. In an alternative analysis, I-V curves showed better fit to the power law indicating that total diode current is combination of TED and SCLC. In addition, the analysis revealed that the junction had high series resistance and non-linear SCL shunt current. The shunt leakage current found to be space charge limited and showed symmetry in the vicinity of $V=0$. Both I-V characteristics analysis and admittance measurements indicated the presence of defect states affecting junction current.

In case of n-CdTe/p-Si and p-CdTe/n-Si, the analysis of junction capacitance as function of voltage and frequency indicated that the depletion region is mostly spread on CdTe side in both n-CdTe/p-Si and p-CdTe/n-Si with minimum band bending on Si side. The junctions consist of large number of defects on CdTe side giving rise to trap states in CdTe band gap. The carrier concentration determined from C-V in n-CdTe showed drastic change from $1.66 \times 10^{14} \text{ cm}^{-3}$ to $2.05 \times 10^{17} \text{ cm}^{-3}$ with increasing In concentration from 0.625 wt% to 2.5 wt%, whereas in case of p-CdTe, it did not vary significantly with addition of excess Te. The carrier concentration results are in conformity with results obtained using Hall Effect measurements. A slight deviation in C-V measured carrier density may be due to the interplay of defect states in C-V measured values. From the analysis of I-V curves of the n-CdTe/p-Si and p-CdTe/n-Si, it can be concluded that current conduction mechanism in both junctions is deviated from the ideal diode nature. The variation of dynamic resistance of both CdTe/Si junction with respect to bias voltage clearly shows that the current in diode is limited by traps in materials as well as at the interface. Further, the series resistance is found to affect the current at higher bias voltages. However, with increasing doping concentration in CdTe the series resistance decreased.

CHAPTER 6

CONCLUSIONS AND SCOPE FOR FURTHER WORK

6.1 INTRODUCTION

The objective of the present work was to understand the electrical transport properties in some of the technologically important II-VI compound heterojunctions. These compounds are known to exhibit high electrical resistivity with low intrinsic carrier concentration and low carrier mobility in the thin film form. In addition, the self-compensation effects involving defects restrict the conductivity of the films. An effective utilization of these compound semiconducting thin films can only be possible by improving the carrier density and/or mobility of the carriers. Detailed investigations are needed to attempt these improvements. As a step in this direction, the work was carried out to grow individual films, studying the effect of growth and processing conditions on the properties of the films, and then to form heterojunction of these compounds using growth conditions optimized from initial works. The heterojunctions were characterized with a range of electrical measurements i.e., based on I-V and C-V to gain insight about charge transport and to evaluate device applicability. The important conclusions that can be drawn from the work are summarized below.

6.2 CONCLUSIONS

6.2.1 Preparation of II-VI compound thin films

Initially, the CdTe, CdSe, ZnTe, and ZnSe have been grown using vacuum evaporation and the effect of growth parameter, in particular substrate temperature on its crystal structure, stoichiometry, and electrical properties were studied.

The elemental composition of the films found to be non-stoichiometric when deposited on a substrate at room temperature. The elemental ratios between II group element and VI group element for CdTe, CdSe, ZnTe, and ZnSe were 0.89, 0.85, 0.78, and 0.95, respectively. Increasing substrate temperature improved the elemental ratio towards unity and stoichiometric composition was attained for CdTe, CdSe,

ZnTe, and ZnSe at substrate temperatures 523 K, 453 K, 553 K, and 423K, respectively. As stoichiometry improved, the crystallinity also enhanced due to the re-evaporation of disordered and excess elemental component at elevated substrate temperature. The XRD analysis showed that all four compounds had stable phase i.e. CdTe ZnTe and ZnSe had cubic (sphalerite) phase while CdSe had hexagonal (wurtzite) phase.

All the four samples had poor conductivity when deposited at room temperature. The poor conductivity of the sample may be due to the native defects like vacancies and/or interstitials typical to these compounds. The activation energy for electrical conduction determined from temperature dependence of the resistance has indicated the presence of deep traps in forbidden gap.

6.2.2 Processing and doping of CdTe

The post deposition treatment and doping are important steps in order to improve the structural, compositional and hence, the electrical properties desired for applications of CdTe. As-deposited films in the present work were Te rich, which attained stoichiometric composition upon annealing. Air annealing of CdTe films lead to Cd rich films. Annealing of doped CdTe films was also found to improve the electrical properties of the films. Indium doped CdTe films, upon annealing, had improved n-type conductivity. The electron density also varied from 10^{13} to 10^{15} cm^{-3} with In content from 0.625 wt % to 2.5 wt % in CdTe films. Similarly, hole density varied from 10^{13} to 10^{16} cm^{-3} with excess Te concentration from 1.25 wt% to 2.5 wt% in CdTe films.

6.2.3 Heterojunctions of II-VI compounds

Four different heterojunction, namely p-CdTe/n-ZnSe, n-CdSe/p-ZnTe, n-CdTe/p-Si, and p-CdTe/n-Si were fabricated using thermal evaporation method. The heterojunctions were evaluated through I-V and C-V measurements, as transport properties and interface properties such as barrier height and defect states of the heterojunctions play crucial role in deciding the device applicability. All the heterojunctions have shown rectifying nature as seen from the I-V characteristic.

Current conduction in p-CdTe/n-ZnSe was dominated by the trap-assisted recombination and high injection current as determined from ideality factors in diode equation used for fitting the measured I-V curves. Capacitance measurements revealed the presence of traps and insulating interfacial layer that controls the current transport across the junction. However, larger band gap of ZnSe and valence band offset are favorable for better performance.

I-V characteristics of n-CdSe/p-ZnTe heterojunction were analyzed with TED model and SCLC model. The barrier height of n-CdSe/p-ZnTe junction $\phi_b = 0.36$ eV and ideality factor $n = 3.34$ were obtained for the heterojunction. The higher ideality factor and lower Richardson's constant than the theoretically expected values suggest the deviation of charge transport mechanism from TED model. In an alternative analysis, I-V curves showed better fit to the power law indicating that total diode current is combination of TED and SCLC. In addition, the analysis revealed that the junction had high series resistance and non-linear SCL shunt current. The shunt leakage current found to be space charge limited and showed symmetry in the vicinity of $V=0$. Both I-V characteristics analysis and admittance measurements indicated the presence of defect states affecting junction current.

In case of n-CdTe/p-Si and p-CdTe/n-Si, the analysis of junction capacitance as function of voltage and frequency indicated that the depletion region is mostly spread on CdTe side in both of them with minimum band bending on Si side. The junctions consist of large number of defects on CdTe side giving rise to trap states in CdTe band gap. The carrier concentration determined from C-V in n-CdTe showed drastic change from $1.66 \times 10^{14} \text{ cm}^{-3}$ to $2.05 \times 10^{17} \text{ cm}^{-3}$ with increasing In concentration from 0.625 wt% to 2.5 wt%, whereas in the case of p-CdTe, it did not vary significantly with addition of excess Te. The carrier concentration results are in conformity with results obtained using Hall Effect measurements. A slight deviation in C-V measured carrier density may be due to the interplay of defect states in C-V measured values. From the analysis of I-V curves of the n-CdTe/p-Si and p-CdTe/n-Si, it can be concluded that current conduction mechanism in both junctions is deviated from the ideal diode nature. The variation of dynamic resistance of both CdTe/Si junction with respect to bias voltage clearly shows that the current in diode is limited by traps in

materials as well as at the interface. Further, the series resistance is found to affect the current at higher bias voltages. However, with increasing doping concentration in CdTe the series resistance decreased.

6.3 SCOPE FOR THE FURTHER WORK

In order to enhance the performance of the devices incorporating these compounds, methods to increase uncompensated carrier concentration has to be found. Studies including co-doping and finding passivating mechanism to deactivate the compensating defects may help to improve the conductivity of these compound semiconductors. Finding a method to reducing contact barrier height in p-CdTe by either chemical treatment or incorporating an interfacial layer may improve the carrier collection and injection at metal/p-CdTe interface.

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PUBLICATIONS

Journal

1. Acharya, S., Bangera, K.V. and Shivakumar, G.K. (2016). “Conduction mechanism in n-CdSe/p-ZnTe Heterojunction.” *Journal of Elec Materi*, 45 (7), 3324–3331.
2. Acharya, S., Bangera, K.V. and Shivakumar, G.K. (2015). “Electrical characterization of vacuum-deposited p-CdTe/n-ZnSe heterojunctions.” *Appl Nanosci*, 5 (8), 1003–1007.

Conference

1. Acharya S., Bangera K. V., Shivakumar G. K., 2014, “Electrical studies on n-CdSe/p-ZnTe heterojunctions”, First International Conference on Large Area and Flexible Microelectronics at R. V. College of Engineering.

Shashidhara

Curriculum Vitae

Contact Information Thin film lab,
Department of Physics,
National Institute of Technology Karnataka, Surathkal,
Mangalore – 575025, India.
Tel. no.: 96611222669
acharyashashidhar@yahoo.in

Education

Aug 2010- **National Institute of Technology Karnataka, Surathkal, India.**

Present Ph.D., Physics (course work CGPA: 8.67)
Electrical studies on II-VI compound semiconductor for device applications.

July 2005- **Mangalore University, Mangalore, India.**

July 2007 M.Sc., Materials Science (60%)

Research Experience

Aug 2010- **National Institute of Technology Karnataka, Surathkal, India.**

Present Doctoral Student

Compound semiconductor thin films and heterojunctions

- Growth and characterization of technologically important II-VI semiconductors to provide an insight of the growth parameters on their optoelectronic properties.
- Studies on various types of heterojunctions consisting II-VI heterojunctions for possible device applications.

Supervisors : Prof. G. K. Shivakumar and Prof. Kasturi V. Bangera

Apr 2009 - **National Aerospace Laboratories, India.**

Aug 2010 Project Scientist

Solar selective coating

Involved in developing a spectrally selective coating, optimized for high absorptance and low thermal emittance with high thermal stability, using DC magnetron sputtering.

Project leader: Dr. Harish C. Barshilia

Mar 2008 - **National Aerospace Laboratories, India.**

Mar 2009 Project graduate trainee

Nanostructured hard coatings

Involved in preparation of multilayer (TiN/CrN), nanocomposite (TiAlSiN and TiAlCrYN) thin film coatings having high values of hardness. Also carried out the characterization of the thin films using various microscopes, spectroscopic, diffraction techniques and performance evolution of coating.

Mentor: Dr. Harish C. Barshilia

Academic Experience

June 2010- **National Institute of Technology Karnataka, Surathkal, India.**

June 2014 Teaching Assistant

B. Tech. Physics Laboratory

M. Sc. Physics laboratory and Projects (Semiconductor Thin Films)

Aug 2007- **Pilikula Regional Science Centre, Mangalore, India.**

Mar 2008 Educational officer

Involved in science popularization programs through setting up and demonstration of scientific models, organizing various educational, astronomy and natural awareness programs.

Skills

Multi component thin films growth - Thermal Evaporation, DC, Pulsed DC and RF Magnetron (balanced and unbalanced) Sputtering

Thin films characterization - X-Ray Diffraction, SEM, EDAX, XPS, Raman Spectroscopy, UV-Vis Spectrophotometer, Optical thin films thickness measurement system, Photoluminescence

Device characterization - DC Source Measure Units, Digital Multimeters, Electrometers, DC Probe Station, Precision LCZ Meters, Monochromator with PMT, Hall effect set-up, Oscilloscopes

Software - Origin, Matlab, COMSOL Multiphysics, Materials Studio, MS office, Windows, Ubuntu

Publications

Journal Papers (Peer Reviewed)

1. **Shashidhara Acharya**, Kasturi V Bangera and Shivakumar G K
“*Conduction mechanism in n-CdSe/p-ZnTe Heterojunction*”, Journal of Electronic Materials, Volume 45, issue 7, 2016, Pages 3324-3331
2. **Shashidhara Acharya**, Kasturi V Bangera and Shivakumar G K
“*Electrical characterization of vacuum-deposited p-CdTe/n-ZnSe heterojunctions*”, Applied Nanosciences, Volume 5, issue 8, 2015, Pages 1003-1007
3. Harish C. Barshilia, Moumita Ghosh, **Shashidhara**, Raja Ramakrishna and K. S. Rajam
“*Deposition and characterization of TiAlSiN nanocomposite coatings prepared by reactive pulsed direct current unbalanced magnetron sputtering*”, Applied Surface Science, Volume 256, Issue 21, 15 2010, Pages 6420-6426
4. Harish C. Barshilia, **Shashidhara Acharya**, Moumita Ghosh, T.N. Suresh, K.S. Rajam, Manohar S. Konchady, Devdas M. Pai, Jagannathan Sankar
“*Performance evaluation of TiAlCrYN nanocomposite coatings deposited using four-cathode reactive unbalanced direct current magnetron sputtering system*”, Vacuum, Volume 85, Issue 3, 24 2010, Pages 411-420

Conferences

1. **Shashidhara Acharya**, Kasturi V Bangera, Shivakumar G K,
“*Electrical studies on n-CdSe/p-ZnTe heterojunctions*”,
In: First International Conference on Large Area and Flexible Microelectronics, Dec 2014 at R. V. College of Engineering, Bangalore, Karnataka, India.
2. Harish C. Barshilia, Moumita Ghosh, **Shashidhara Acharya**, Suresh T.N. and K. S. Rajam,
“*Characterization of TiAlCrYN nanocomposite coatings prepared using four-cathode reactive unbalanced direct current magnetron sputtering system*”. In: International Conference on Nanomaterials and Nanotechnology, 13-16 Dec 2010, K. S. Rangasamy College of Technology, Tiruchengode, India.
3. Harish C. Barshilia, Moumita Ghosh, **Shashidhara Acharya**, Rajarama Krishna and K. S. Rajam
“*Deposition of TiAlSiN nanocomposite coatings using four-cathode reactive direct current unbalanced magnetron sputtering system*”, In: International Conference on Surface Modification Technologies XXIII, Nov 2-5, 2009, GRT Temple Bay, Mamallapuram, India.

4. Moumita Ghosh, **Shashidhara**, Harish C. Barshilia, K. S. Rajam
“*Development of TiAlSiN nanocomposite coatings*” Presented at Annual Seminar in Hindi (ANSH-2010), Aug 30, 2010, NAL, Bangalore, Karnataka, India.

Workshops

1. International Winter school on Organic Electronic Materials and Devices (OEMD 2013), 19-21 Dec 2013, National Institute of Technology Karnataka, Surathkal, India.
2. Workshop on Quantum Mechanism and Applications, 22-24 Mar 2013, Department of Physics, National Institute of Technology Karnataka, Surathkal, India.
3. 8th INUP Hands on Training in “*Nanoelectronicis Fabrication Technologies*”, 18-27 July 2011, Centre for Nano Science and Engineering, Indian Institute of Science, Bangalore, India.
4. MEMS Design Software Training Program, 30 May – 4 June 2011, MEMS Design Centre, National Institute of Technology Karnataka, Surathkal, India.
5. One-day symposium on “*Recent Advances in Photonics*”, Mar 29th 2011, Centre for Atomic and Molecular Physics Manipal University, Manipal, India.
6. 3rd International Winter School for Graduate Students (iWSG) and 5th Indian Nanoelectronicis Users Program (INUP) Familiarization Workshop on Nanofabrication Technologies, 3-8 Jan 2011, Centre for Nano Science and Engineering, Indian Institute of Science, Bangalore, India.
7. Awareness Workshop on The Facility of UGC-DAE Consortium For Scientific Research, 6-7 Sep 2010, Manipal Institute of Technology Manipal, India.