DESIGN OF AN INVERTER-BASED HIGH GAIN OTA, AND ITS APPLICATION IN DELTA SIGMA MODULATORS AND CLASS-D AMPLIFIERS FOR AUDIO APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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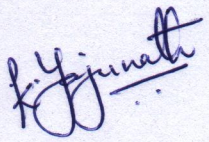
DECLARATION

I hereby ***declare*** that the Research Thesis entitled **DESIGN OF AN INVERTER-BASED HIGH GAIN OTA, AND ITS APPLICATION IN DELTA SIGMA MODULATORS AND CLASS-D AMPLIFIERS FOR AUDIO APPLICATIONS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.



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CERTIFICATE

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Dedicated to my parents

Abstract

The Semiconductor IC industry is largely driven by the demands of digital IC design. One of the largely adopted practices is to scale down the technology node and operate on lower supply voltages. This led to faster devices with lower dynamic power consumption. The digital design has hugely benefitted from this. However, there are a large family of analog circuits which suffer performance degradation when operated on low supply voltages. Therefore, for such applications, it is common to operate analog designs on higher supply voltages i.e. in excess of 1 V. In addition, portable, battery powered electronic applications such as digital microphones, image sensors, data acquisition systems, hearing aids, etc., demand low power consumption to save on battery energy. Almost all analog designs have Operational Tranconductance Amplifier (OTA) as one of the integral blocks for realizing various functionalities. OTAs offering sufficiently high dc gain (as per the requirements of application) with lower power consumption will help in realizing the objective of low-power design.

This research is an outcome of the efforts towards proposing an architecture for realizing an inverter-based OTA for switched capacitor based applications and prove its candidature in a couple of applications. The proposed OTA can achieve dc gain in excess of 100 dB and it can be made stable without the need for any explicit compensation scheme. A complete analysis of the OTA along with the design procedure has been presented.

The proposed OTA has been designed in 1P6M UMC 180 nm standard CMOS process technology from UMC Technologies. The power supply for operation has been chosen to be 1.8 V. Two OTAs have been presented, one for biomedical applications and the other for audio applications. The OTA designed for biomedical applications offers a dc gain of 109.3 dB and a unity gain bandwidth (UGB) of 5.29 MHz at 81° phase margin with a capacitive load of 2.5 pF for a typical process corner at room temperature (27°C). The quiescent current consumption of the OTA is 4.79 μA, resulting in a power consumption of 8.62 μW. The second OTA for audio applications offers a dc gain of 96.8 dB and a UGB of 19.4 MHz at 86°

phase margin with a capacitive load of 5 pF for a typical process corner at room temperature. This design draws a quiescent current (I_Q) of 38.4 μA. The proposed OTA has been proved to be robust though Monte-Carlo simulations. It is also proved to be one among the best designs found in the literature, from the Figure-of-Merit commonly used for evaluating OTAs.

To validate the worthiness of the proposed OTA, a 1-bit third order discrete time Delta Sigma Modulator has been designed for audio applications using the proposed inverter-based OTA. The three integrators of the feed-forward modulator use the proposed OTA as their main block. The classical modulator, without the use of any dedicated improvement scheme, achieves a peak SNR of 91.2 dB and peak SNDR of 87.7 dB with a dynamic range of 89.9 dB. The modulator consumes 570.6 μW operating on 1.8 V supply. The Figure-of-Merit proves that the modulator is a fitting candidate among similar modulators found in the literature.

Extending further, a Class D audio amplifier has been designed. The class-D amplifier is targeted for 8 Ω speaker load. The on-chip amplifier adopts the delta-sigma-modulation scheme for achieving audio-grade performance. The power-stage has been designed to have 97.5% efficiency. The class-D amplifier, without any additional scheme for improving the performance, offered a dynamic range of 89.7 dB along with a best THD+N of -85.8,dB for 8 Ω speaker load delivering a maximum power of 100 mW while operating on 1.8 V supply. The efficiency of the amplifier is 92.3% at the peak output power. The amplifier is found to be one of the best in its class.

Keywords: Inverter-based OTA, high gain, cascoding, gain-boosting, switched capacitor integrator, delta sigma modulator, feed-forward topology, audio applications, class D amplifier.

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Abbreviations

CDA	Class D Amplifier
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DR	Dynamic Range
DSM	Delta Sigma Modulator
DTDSM	Discrete - Time Delta Sigma Modulator
DFT	Discrete Fourier Transform
FoM	Figure of Merit
IC	Integrated Circuit
IGB-OTA	Inveter-based Gain-Boosted Operational Transconductance Amplifier
NMOS	N-channel Metal Oxide Semiconductor
NTF	Noise Transfer Function
NBW	Noise Bandwidth
OSR	Over Sampling Ratio
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PMOS	P-channel Metal Oxide Semiconductor
PVT	Process, supply Voltage and Temperature
SoC	System on Chip
SC	Switched Capacitor
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SQNR	Signal to Quantization Noise Ratio
THD+N	Total Harmonic and Distortion plus Noise Ratio
UGB	Unity Gain Bandwidth in radians per second
UMC	United Microelectronics Corporation

Notations

C_{ox}	Gate-oxide capacitance
f_b	Signal bandwidth in Hz
f_{clk}	Clock frequency in Hz
f_{in}	input Signal frequency in Hz
f_N	Nyquist frequency in Hz
f_s	Sampling frequency in Hz
$1/f$	Flicker noise
g_m	Gate transconductance in Siemens
g_o	Output conductance of MOSFET in Siemens
g_{mb}	Bulk-transconductance in Siemens
k	Boltzmann Constant
L	Channel length of the MOSFET
η	Sub-threshold slope factor
q	Electronic charge
$S(f)$	Power Spectral Density
T	Absolute temperature
μ	Carrier mobility
V_{TH}	Threshold voltage
V_T	Thermal voltage
V_{GS}	Gate-source voltage of the MOSFET
V_{DS}	Drain-source voltage of the MOSFET
V_{BS}	Bulk-source voltage of the MOSFET
ω	Angular frequency in radians per second
γ	Noise co-efficient
W	Channel width of the MOSFET

.

Chapter 1

INTRODUCTION

1.1 MOTIVATION

The invention of transistor was a giant leap forward for the field of electronics. Smaller size, higher reliability and the requirement of only milli watts of power to operate, made the world to move from the conventional vacuum tube based systems to transistor based ones. With the invention IC's in the subsequent years, the world witnessed a drastic change in the landscape of electronics industry. The entire electronic circuit got integrated on a single chip which resulted in electronic devices that are lighter, smaller and cheaper. Since then, the field of electronics has advanced in productivity and performance at a pace unmatched in technological history.

Over the last two decades, the semiconductor IC industry has been rapidly and consistently scaling the CMOS technology and has immensely benefited from it. The scaling of technology is largely driven by the performance gain offered by the digital circuits. It resulted in faster devices with lower dynamic power consumption and allowed integration of more and more functionality per unit area. However, the performance of analog and mixed-signal circuits does not necessarily improve with technology scaling. The major effect of technology scaling, from an analog design perspective, can be listed as follows.

- Supply voltage is scaled down with the technology reducing the voltage headroom available for analog circuits.

- Threshold voltage of Metal-Oxide-Semiconductor (MOS) transistors does not scale consistently with the supply voltage.
- Intrinsic gain of transistor reduces.
- Linearity offered by the transistors reduces.
- Noise increases as the transistor density increases.
- Dynamic range reduces, due to reduced linearity and increased noise.
- Gate leakage current increases.
- The effect of layout parasitics becomes more pronounced.

The above limitations are the impediments for analog and mixed-signal circuits in taking advantage of technology scaling. This has prompted the circuit designers to try implementing as much as analog functions in digital domain. As a result, computational and signal processing tasks are now performed predominantly by digital circuits since they can be realized by extremely small and simple structures that can in turn be combined to obtain very complex, accurate, and fast systems (Pavan et al. 2017). However, we live in an analog world that cannot be accurately represented with purely digital design. Therefore, despite a number of efforts over the years to replace analog with digital circuits, analog still has a solid foothold in chip design. Digitally assisted analog design techniques like digital calibration allowed some of the analog and mixed-signal circuits to be integrated with the digital blocks. However, high performance analog and mixed-signal circuits are essential as they are the interface between the analog signal from/to real world and the digital signal processors.

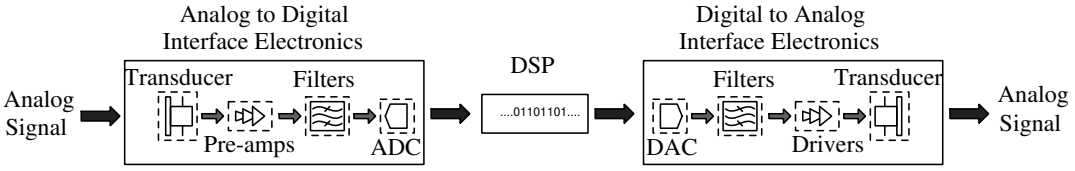

Figure 1.1: Generic analog signal processing system (Pavan et al. 2017)

Figure 1.1 shows a generic analog signal processing system. The real world analog signal is sensed by an appropriate transducer and it is amplified by pre-amplifier stage

since the sensed real world analog signal is usually weak. Then, a filter stage filters out unwanted signal components and an Analog-to-Digital Converter (ADC) converts it into digital domain, allowing the Digital Signal Processor (DSP) to do the necessary signal processing. Bio-medical applications fall under this front-end category where bio-siganls are sensed by bio-sensors and are converted into digtal domain. To convert the digital signal back to an analog form, a Digital to Analog Converter (DAC) is used followed a filter stage which removes any unwanted signal components that were intentionally/unintentionally added by ADC and DSP. And then, the filtered signal is strengthened by the driver stage in order to drive an appropriate transducer. Audio amplifier is an example for the back-end application where the input audio signal has to amplified to a level suitable for driving the speaker load. These analog signal processing circuits are required to be implemented on a single chip along with the digital circuits. Often, digital circuits are operated on a lower supply voltage, commonly known as core voltage, to take advantage of performance gain with respect to speed and dynamic power loss. And, analog circuits are operated on a higher voltage, typically made available for Input-Output (IO) pads, to take advantage of voltage head-room (Pavan et al. 2017).

The demand for portable consumer electronics such as mobiles, tablets, laptops, wireless speakers, smart wearables etc., has increased quite significantly over the last few years. As these devices are battery powered, the battery life is one of the key factors which decide the commercial success of these products. Unfortunately, the battery technology has not kept up with the energy requirement of the portable electronic devices. Therefore, these applications require circuit designs that are power efficient.

Switched capacitor (SC) circuits are used in the discrete-time implementation of most of the analog and mixed signal integrated circuit (IC) designs such as filters and data converters (Quinn and van Roermund 2007, Razavi 2017). Operational Transconductance Amplifier (OTA) is the fundamental building block of switched capacitor circuits and it accounts for a large fraction of the total power consumed by the IC. Further, the dc gain of an OTA determines the accuracy of charge transfer in the SC circuits and therefore plays a significant role in the overall performance of SC application (Quinn and van Roermund 2007). To demonstrate the significance of OTA's dc gain in SC circuits, consider a SC integrator shown in Figure 1.2. V_i is the input to the integrator and V_o is the output of the integrator. C_s is the sampling

capacitor used for sampling the input signal and C_i is the integrating capacitor that accumulates the charge transferred from C_s in every clock cycle. Initially capacitor C_i is reset in ϕ_{rst} phase. ϕ_1 is the sampling phase in which input V_i is sampled onto the sampling capacitor C_s. ϕ_2 is the integration phase during which the total charge on the sampling capacitor C_s is completely transferred onto the integrating capacitor C_i, provided that the dc gain of OTA is infinite.

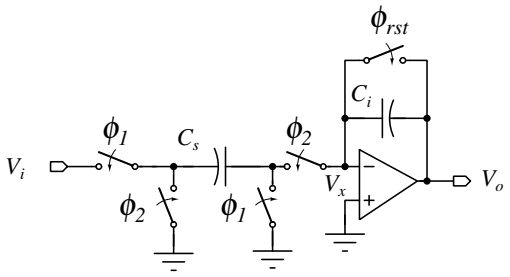

Figure 1.2: Switched Capacitor Integrator circuit (Bourdopoulos et al. 2003)

To study the effect of finite dc gain of the OTA on the integrator, let us consider the gain of OTA to be A_0. Therefore, node voltage V_x at the inverting terminal of OTA can be expressed as follows at all times.

$$(0 - V_x)A_0 = V_o \tag{1.1}$$

$$\therefore V_x = -\frac{V_o}{A_0} \tag{1.2}$$

The equivalent circuit of switched capacitor integrator during the two clock phases are shown in Figure 1.3.

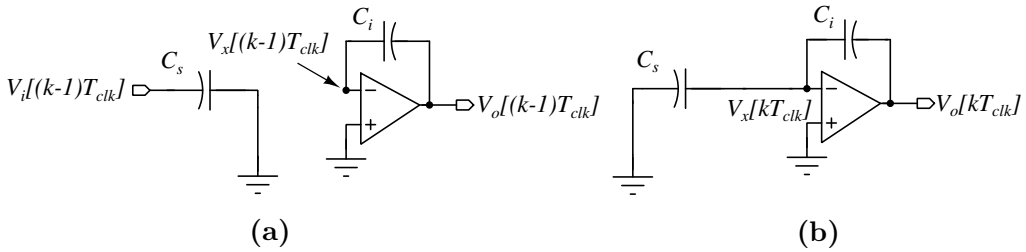

Figure 1.3: Equivalent circuit of SC Integrator during (a) ϕ_1 phase (b) ϕ_2 phase

The total charge $Q_{\phi 1}$ during ϕ_1 phase can be expressed as follows

$$\begin{aligned} Q_{\phi 1} &= (0 - V_i[(k-1)T_{clk}])\, C_s + (V_x[(k-1)T_{clk}] - V_o[(k-1)T_{clk}])\, C_i \\ &= -V_i[(k-1)T_{clk}]C_s + (V_x[(k-1)T_{clk}] - V_o[(k-1)T_{clk}])\, C_i \end{aligned} \tag{1.3}$$

Using 1.2 in 1.3, we get

$$\begin{aligned} Q_{\phi 1} &= -V_i[(k-1)T_{clk}]C_s + \left(\frac{-V_o[(k-1)T_{clk}]}{A_0} - V_o[(k-1)T_{clk}]\right) C_i \\ &= -V_i[(k-1)T_{clk}]C_s - \left(1 + \frac{1}{A_0}\right) V_o[(k-1)T_{clk}]C_i \end{aligned} \tag{1.4}$$

And the total charge $Q_{\phi 2}$ during ϕ_2 phase can be expressed as follows

$$\begin{aligned} Q_{\phi 2} &= (V_x[kT_{clk}] - 0)\, C_s + (V_x[kT_{clk}] - V_o[kT_{clk}])\, C_i \\ &= V_x[kT_{clk}]C_s + (V_x[kT_{clk}] - V_o[kT_{clk}])\, C_i \end{aligned} \tag{1.5}$$

Using 1.2 in 1.5, we get

$$\begin{aligned} Q_{\phi 2} &= \left(-\frac{V_o[kT_{clk}]}{A_o}\right) C_s + \left(-\frac{V_o[kT_{clk}]}{A_o} - V_o[kT_{clk}]\right) C_i \\ &= -\frac{V_o[kT_{clk}]}{A_o} C_s - \left(1 + \frac{1}{A_o}\right) V_o[kT_{clk}]C_i \end{aligned} \tag{1.6}$$

Equating the total charge during ϕ_2 and ϕ_1 (i.e., equating 1.6 and 1.4), we get

$$\begin{aligned} -\frac{V_o[kT_{clk}]}{A_o} C_s - \left(1 + \frac{1}{A_o}\right) V_o[kT_{clk}]C_i &= -V_i[(k-1)T_{clk}]C_s \\ &\quad - \left(1 + \frac{1}{A_0}\right) V_o[(k-1)T_{clk}]C_i \end{aligned} \tag{1.7}$$

Applying Z-transform on 1.7, we get

$$-\frac{V_o[z]}{A_o} C_s - \left(1 + \frac{1}{A_o}\right) V_o[z]C_i = -z^{-1}V_i[z]C_s - \left(1 + \frac{1}{A_0}\right) z^{-1}V_o[z]C_i \tag{1.8}$$

Simplifying this, we get

$$\frac{V_o[z]}{V_i[z]} = \frac{C_s}{C_i} \frac{z^{-1}}{\left[\left(\frac{1}{A_0}\right)\frac{C_s}{C_i} + \left(1+\frac{1}{A_0}\right)(1-z^{-1})\right]} \tag{1.9}$$

Further, 1.9 can be expressed as follows (Luo et al. 2013b).

$$\frac{V_o[z]}{V_i[z]} = \frac{C_s}{C_i}\left(\frac{\lambda z^{-1}}{1-pz^{-1}}\right) \tag{1.10}$$

$$\lambda = \frac{1}{1+\left(1+\frac{C_s}{C_i}\right)\frac{1}{A_0}} \tag{1.11}$$

$$p = \frac{\left(1+\frac{1}{A_0}\right)}{1+\left(1+\frac{C_s}{C_i}\right)\frac{1}{A_0}} \tag{1.12}$$

where (1-λ) represents the gain error and $(1-p)$ represents the phase error in a SC integrator. When the gain of the OTA, A_0, is infinite, $\lambda = p = 1$ and it results in an ideal integrator transfer function as given in 1.13.

$$\frac{V_o[z]}{V_i[z]} = \frac{C_s}{C_i}\left(\frac{z^{-1}}{1-z^{-1}}\right) \tag{1.13}$$

The gain error and phase error can be approximately expressed as follows.

$$1 - \lambda \approx \left(1+\frac{C_s}{C_i}\right)\frac{1}{A_0} \tag{1.14}$$

$$1 - p \approx \frac{C_s}{C_i}\frac{1}{A_0} \tag{1.15}$$

From 1.14 and 1.15, it is evident that gain error and phase error are inversely proportional to A_0 and therefore it is a necessity in SC integrators to have OTA with a high dc gain. A dc gain of 40 dB with $C_s = C_i$ results in a gain error of 2 % and a phase error of 1 %. In delta sigma modulators, phase error shifts the zeroes of the noise transfer function and thus affects the stability of the feedback loop. In Pavan et al. (2017), it was suggested that in the design of delta sigma modulators, it is a good practice to have an OTA with dc gain in excess of 80 dB. DC gains of the OTA

in some of the high performance discrete-time SC based applications are outlined in Table 1.1.

Table 1.1: Summary of OTA's dc gain in discrete-time based applications

Reference	Application	OTA Architecture	OTA DC Gain
Kang et al. (2008)	Audio	Folded Cascode	76 dB
Kuo et al. (2010)	Audio	2 stage Cascade	76 dB
Luo et al. (2013b)	Audio	Inverter-based	83 dB
Daoud et al. (2016)	Wireless Communication Systems	Telescopic	96 dB
Hwang et al. (2017)	Audio	Inverter-based	> 85 dB

It is clearly evident from the table that OTAs with high dc gain (> 75 dB) have been used in SC applications and therefore, as suggested in Pavan et al. (2017), it is accepted that OTAs designed for SC application should have dc gain gain in excess of 80 dB.

High gain OTAs are typically realized using one of the following topologies. Cascade of amplifiers, Cascode (telescopic) and Folded Cascode. Cascade of amplifiers are realized by cascading multiple stages of amplifiers (typically two). They are capable of offering high swing at the output upto rail-to-rail. However, it is critical to ensure stability in closed loop operation, owing to the presence of multiple poles. Multiple stages along with the compensation requirements make OTAs power hungry. Cascode architecture is capable of offering gain of the order of that of a cascaded OTA, but with a single stage. Stability requirement is relaxed owing to single stage. However, it seriously fails to offer a large swing at the output. Therefore, this type of OTAs are best suited for applications where the signal swing requirement is small, for example DSM. Folded cascode OTA offers slightly higher swing when compared to Cascode but falls short in stability and power requirement. Cascode/Folded-cascode amplifiers are also cascaded with a common-source amplifier stage to achieve higher swing and dc gain. However, this comes with a penalty of compensation and associated power requirements.

A CMOS Inverter-based architecture has been found as an alternative method, in literature, for realizing OTAs (Figueiredo et al. 2011, Shrimali and Chatterjee 2011, Michel and Steyaert 2012, Wilson et al. 2013, Luo et al. 2013b, Harjani and Palani 2015, Lee et al. 2016, de Aguirre and Susin 2018). Such OTAs have been

seen as a replacement for traditional OTA's, especially for Switched-Capacitor (SC) applications. The idea here is to use a CMOS inverter, operated at a point on the transfer characteristics where the slope is maximum. The inverter being a single ended amplifier, the differential operation, if any, has to be realized using pseudo-differential architecture and has been the case as per the literature. A CMOS inverter has a poor gain, making it unsuitable for OTA applications. The CMOS inverters are found to be used with cascode transistors and additional gain boosting stages to have dc gain sufficiently high enough to be used as OTAs (Luo et al. 2013b, Lee et al. 2016). Due to the single stage structure and simplicity, this kind of architecture is found to be a promising candidate for OTA realization, especially for SC applications.

This research is an outcome of the efforts of designing an inverter-based low power OTA to offer dc gain in excess of 80 dB and stability with a very good margin, for SC applications. The major contributions of this research work are given in the following section.

1.2 CONTRIBUTIONS

The research proposes an architecture for realizing inverter-based high gain OTAs intended for supply voltages more than sum of threshold voltages of NMOS and PMOS transistors i.e. $V_{TH,n} + |V_{TH,p}|$. A detailed analysis on the design aspects and stability has been presented. The proposed architecture has been validated by designing OTAs in 180 nm standard CMOS process for operation on 1.8 V supply. Two designs have been presented. The first design with a dc gain of 109.3 dB is targeted for biomedical applications. The OTA has been designed to have a unity gain bandwidth (UGB) in excess of 3 MHz for a load capacitance (C_L) of 2.5 pF with power consumption of 8.62 μW. The second OTA has been targeted for audio applications. The OTA is intended for use in SC loop filter of discrete-time DSM (DTDSM). The OTA is designed to offer 96.8 dB dc gain with UGB of 19.4 MHz for C_L=5 pF. In both the cases, the OTAs are stable with phase margin in excess of 80° without any explicit compensation. Thanks to the single stage architecture.

A 1-bit third order DTDSM has been designed using the second OTA to prove that the proposed design fits well for SC applications. A feed-forward architecture has been chosen for implementing the loop filter of DTDSM. The DTDSM, for audio

applications, is proved to be one of the best among the state-of-the-art designs offering a peak Signal to Noise and Distortion Ratio (SNDR) of 87.7 dB.

One of the power hungry analog systems in many of the portable electronics is the audio amplifier. The efficiency of such amplifiers is crucial from the battery life perspective. A Class-D amplifier (CDA) is best in its class with respect to efficiency. However, one of the limiting factor in achieving the efficiency is the power consumption in the control circuit. The proposed OTA, having low power, has been tested for its candidature in CDA. A CDA using DTDSM loop has been designed for 8 Ω speaker load. The CDA achieved an efficiency of 92.3% with an A-weighted peak Total Harmonic Distortion plus Noise (THD+N) of -90.3 dB, again one among the best in class.

1.3 PRIOR WORK

The OTA being the basic building block, various architectures have been proposed in the literature. Requirement on the OTA is different for different applications. However, in this research, the OTA design is targeted for switched capacitor applications that do not demand rail-to-rail swing. For application like DTDSM, the swing requirement on SC integrators (and hence the OTA) can be relaxed with a careful choice of filter coefficients. Further, the dc gain of an OTA determines the accuracy of charge transfer in the SC circuits (Quinn and van Roermund 2007). Therefore, it is essential for SC circuits to have an OTA that offers sufficiently high dc gain in order to ensure charge transfer with a desired accuracy. This research also targets OTA design for such applications. Some of the 2-stage OTA designs found in literature are presented here.

A two stage body-input OTA is presented in Chatterjee et al. (2005). It offers a dc gain of 62 dB and UGB of 10 MHz with a phase margin (PM) of 45° for a load capacitance C_L of 20 pF. A Figure-of-Merit (FoM), computed using (1.16), is found to be 1333 kV^{-1}.

$$\mathrm{FoM} = \frac{\mathrm{UGB\,(MHz)} \times \mathrm{C_L\,(pF)}}{\mathrm{I_Q\,(mA)}} \tag{1.16}$$

Perez et al. (2009) presents a two-stage OTA with enhanced slew rate designed in 180 nm process. It has a simple differential amplifier first stage and a common-source second stage. The OTA, operating on 1.8 V has a dc gain of 74 dB with a phase

margin (PM) of about 70°. The UGB is 160 MHz with a power of 362 μW for a load capacitance C_L of 1.75 pF. FoM of this OTA is found to be 773 kV^{-1}.

An OTA with a simple differential amplifier first stage and a common-source amplifier with cascode transistors as second stage has been presented in Kang et al. (2008) and has been used in a CDA with DSM based control loop. The OTA offered 76 dB dc gain, 78° PM and 110 MHz UGB for C_L of 1.85 pF. The OTA is operated on 3 V supply and achieves an FoM of 291 kV^{-1}.

The differential input, single ended output OTA presented in Moallemi and Jannesari (2012), targeted for SC applications, has a telescopic cascode first stage and a simple differential second stage. Designed in 180 nm process, the OTA is capable of offering a dc gain of 77 dB with PM of only 45°. Though it is found to offer a UGB of 475 MHz, the power requirement was 5.1 mW for a C_L of 3 pF resulting in FoM of 503 kV^{-1}.

An OTA offering 114 dB dc gain has been presented in Najjarzadegan et al. (2015). The OTA designed in 180 nm has an UGB of 305 MHz consuming a power of 4.3 mW. The FoM of this OTA is found to be 635 kV^{-1}.

The OTAs presented in Farsani and Ghaderi (2016), Sarkar and Panda (2017) are designed in 180 nm process and they offer a dc gain of 90.7 dB and 87.7 dB respectively. However they have relatively poor FoM of 71 kV^{-1} and 70 kV^{-1}.

In Daoud et al. (2016), a gain-boosted telescopic OTA has been presented which has been used in DTDSM targeted for a signal bandwidth of 2 MHz and 3.84 MHz. Though the dc gain offered by the OTA is 96 dB, with a UGB of 487 MHz, the FoM was found to be only 57 kV^{-1}.

The OTA in Pourashraf et al. (2017) offers a FoM of 1627 kV^{-1}. It is a two-stage OTA and both the stages have cascode architecture. The dc gain offered is 67 dB with a UGB of 570 kHz while consuming 14.5 μW power from $\pm$0.9 V supply.

The OTA presented in Garradhi et al. (2018) has 77 dB dc gain with a FoM of 358 kV^{-1}. The PM is found to be only 40°. It has a two stage architecture with a differential first stage and a cascode second stage.

Lopez-Martin et al. (2017) presents an OTA offering FoM as large as 5541 kV^{-1}. The OTA is designed to drive C_L of 70 pF with a power of 120 μW. However, despite being a single stage amplifier, the PM achieved is 60° due to the folded cascode architecture. The dc gain of the OTA is 81.7 dB.

Table 1.2: Performance summary of 2-stage OTAs found in literature

	Kang et al. (2008)	Perez et al. (2009)	Moallemi and Jannesari (2012)	Najjarzadegan et al. (2015)	Daoud et al. (2016)	Farsani and Ghaderi (2016)	Pourashraf et al. (2017)	Sarkar and Panda (2017)	Garradhi et al. (2018)
Supply (V)	2	1.8	-	-	1.4	1.8	±0.9	± 1.8	±0.6
DC Gain (dB)	76	74	77	114	96	90.7	67	87.7	54
UGB (MHz)	110	160	475	305	487	995	0.57	24.8	4
PM (°)	78	70	45	61	-	82	84	65	40
C_L (pF)	1.85	1.75	3	5	1	0.5	23	1	1
Power (μW)	2100	362	5100	4300	12000	12600	14.5	318.6	40
FOM (kV^{-1})	291	773	503	635	57	71	1627	70	358

Performance summary of these OTAs are presented in Table 1.2. For a good DTDSM design, the OTA should be chosen to have dc gain in excess of 80 dB (Pavan et al. 2017). This will help in keeping all distortion terms to sufficiently low level ≈ -90 dBc. In the light of this, the following conclusions can be made from the OTAs found in the literature as presented above.

1. The OTAs that are found to offer dc gain in excess of 80 dB suffer from poor FoM, except one. The OTA presented in Lopez-Martin et al. (2017) has a dc gain 81.7 dB and FoM 5541 kV^{-1}. However, it is to be noted that, the OTA is designed for a large capacitive load of 70 pF. For low values of C_L the phase margin will definitely degrade below 60°.

2. The OTAs having FoM in excess of FoM of 500 kV^{-1} are found to have either dc gain less than 80 dB or consume more power (in the order of mW).

A CMOS Inverter-based architecture has been found to replace the traditional architecture for realizing OTAs. In literature, these OTAs have been found to be used in a few applications and some of them are listed below.

An inverter-based OTA has been proposed in Chae and Han (2009) for DSM application for audio band. The OTA designed in 180 nm has been operated on 0.7 V. With cascode architecture, the dc gain is found to be 60 dB. The third order DTDSM designed, using this OTA, is found to offer a peak SNDR of 81 dB for an OSR of 100.

A two-stage fully differential inverter-based OTA employing self-biasing techniques is presented in Figueiredo et al. (2011). The OTA is designed in 130 nm standard CMOS technology and operates on 1.2 V. It offers a gain of 70 dB with a UGB of 35 MHz and PM of 45° for a C_L of 5.5 pF. The OTA consumes a power of 110 μW.

A three-stage inverter-based OTA with feed-forward compensation technique is presented in Shrimali and Chatterjee (2011). The OTA is designed in 130 nm standard CMOS technology and it is operated on 1.2 V. Despite being a three stage design, the gain offered is only 39.5 dB. However, it offers a UGB of 11 GHz with 62° PM for a C_L of 600 fF. The power consumption of the OTA is 18 mW.

A simple inverter has been used as OTA in a DTDSM in Michel and Steyaert (2012). The OTA is designed in 130 nm standard CMOS technology. The gain realized from the OTA operating on a supply voltage of 250 mV is only 30 dB with a UGB of 6.3 MHz for C_L of 3 pF. The third order DTDSM, for signal band of 10 kHz, offered a peak SNDR of 61 dB for an OSR of 70.

Wilson et al. (2013) proposed a fully differential, low-power current-starving inverter-based amplifier topology designed in 180 nm process. It achieves a dc gain of 48.3 dB with a UGB of 2.4 MHz for a C_L of 6 pF, while operating on 0.9 V. Its power consumption is 3.74 μW.

The OTA presented in Luo et al. (2013b) has been used for DTDSM designed to operate on 0.8 V in 65 nm CMOS process technology. The OTA, employing cascode transistors with gain-boosting, is found to offer 83 dB dc gain and 49 MHz UGB for a 5.75 pF C_L. The DTDSM designed for audio band has a 2-1 cascaded architecture and offers a peak SNDR of 91 dB for an OSR 128. It is found that, the OTA uses body bias technique for both PMOS and NMOS transistors of the inverter, which requires a tripple-well CMOS process technology.

A 2-1 cascaded DTDSM, designed in 130 nm CMOS process, in Luo et al. (2013a) presents an inverter-based OTA. It uses cascode transistors along with gain-boosting technique to achieve a dc gain of 67 dB operating on 1.2 V supply. The UGB is

45.3 MHz for 1.5 pF C_L. As in Luo et al. (2013b), this design also requires a tripple-well process.

A PVT tolerant inverter based OTA, designed in 65 nm CMOS process technology, has been presented in Harjani and Palani (2015). It uses a three stage design. The first stage does the common-mode rejection, the second stage employs cascode architecture for achieving higher gain and the third stage is a miller compensated driver stage. All the stages are biased with the constant gm biasing technique. The proposed OTA offers around 62 dB gain and UGB of around 101 MHz with PM of 62° for a 1 pF C_L.

An adaptive-biased inverter-based OTA has been presented in Gönen et al. (2016). The inverter using cascode transistors are biased adaptively so as to keep the current to 125 μA for a dc gain of 65 dB. The OTA is used in a Zoom-ADC that employs a combination of an asynchronous SAR ADC and a free-running 1b DSM. The course output from the SAR ADC is used to continuously update the references of DSM. The ADC, designed in 180 nm CMOS technology, achieved a peak SNDR of 98.3 dB for audio band with a sampling frequency of 11.29 MHz.

An improved version of the OTA proposed in Gönen et al. (2016) has been presented in Lee et al. (2016). The adaptive biasing scheme has been modified and the quiescent current has been kept to 50 μA. A third order DTDSM realized using this OTA, in silicon, for audio band offered a peak SNDR of 97.7 dB with an OSR of 128.

de Aguirre and Susin (2018) presents a third order continuous-time DSM (CTDSM) based on single stage inverter-based OTA. Operating on 0.6 V, the OTA provides a dc gain of 38.4 dB with UGB of 14.4 MHz with PM of 90° for a C_L of 8 pF. Its consumes a power of 40.1 μW.

Inverter-based OTAs are also used in the design of CTDSMs (Wang et al. 2013, Essawy and Ismail 2014, Irfansyah et al. 2015, Ismail and Mostafa 2016) and filter designs (BarthÚlemy et al. 2008, Braga et al. 2019).

The performance summary of some of these inverter-based OTAs is presented in Table 1.3. It is found that inverter-based OTAs have been used for designs operating on lower supply voltage and they consume power in excess of 50 μA when operated at higher supply voltages (VDD > 1 V) despite the fact that these inverter-based OTAs do not provide dc gain in excess of 80 dB except Luo et al. (2013b).

SC circuit based data converters, operating on supply voltages greater than 1 V, are used in the design of several portable, battery powered electronic applications such as digital microphones (Le et al. 2010, Thomas 2013), bio-sensors (Agah et al.

Table 1.3: Performance summary of inverter-based OTAs found in literature

	Figueiredo et al. (2011)	Shrimali and Chatterjee (2011)	Michel and Steyaert (2012)	Wilson et al. (2013)	Luo et al. (2013a)	Luo et al. (2013b)	Harjani and Palani (2015)	Lee et al. (2016)	de Aguirre and Susin (2018)
Supply (V)	1.2	1.2	0.25	0.9	1.2	0.8	0.9	1.8	0.6
DC Gain (dB)	70	39.5	30	48.3	67	83	62	60	38.4
UGB (MHz)	35	11000	6.3	2.4	45.3	49	101	30	14.4
PM (°)	45	62	-	-	-	-	62	-	90
C_L (pF)	5.5	0.6	3	6	1.5	5.75	1	5.2	8
Power (μW)	110	18000	0.62	3.74	57.2	34.5	6.3	90	40.1
FOM (kV^{-1})	2100	440	7620	3465	1425	6533	14428	3120	1723

2010, Hall et al. 2013, Van Helleputte et al. 2015), image sensor (Chae et al. 2011), data acquisition systems (Liu et al. 2012, Lee et al. 2015), hearing aids (Porrazzo et al. 2013, Custódio et al. 2013, Noh et al. 2013), etc. Such applications require low-power designs, which would result in a relatively cooler devices with longer battery run time. Also, it is common to operate analog signal processing blocks on a higher supply (available for IO) to take advantage of head room available, even though the digital circuitry are operating on low supply voltages. For designs like DTDSM based CDAs, the inverter is required to offer gains in excess of 80 dB and at the same time keep the quiescent current to a sufficiently low value.

Inverter-based OTAs for SC applications, operating on higher supply voltages requires a re-look into the design. An OTA that delivers high dc gain with lower power consumption is the necessity and designing such an OTA is quite challenging. Any research contribution in this direction is considered to be worth the effort. The OTA design is targeted for two applications namely bio-medical applications and audio applications, covering both the front-end and back-end categories.

1.4 ORGANIZATION OF THESIS

The thesis has been organized as follows.

The chapter 2 proposes the inverter-based OTA architecure for realizing a very high gain. It also gives a detailed analysis of the achitecture, its stability and design steps.

The chapter 3 is dedicated for the design of OTA using the proposed architecture. It presents two OTAs for biomedical and audio applications along with all necessary simulation results.

The chapter 4 presents the design of the DTDSM. After a brief introdcution to DTDSM, the chapter outlines the design of SC based implementation of the DTDSM. The circuit design and implementation of each and every block of DTDSM has been presented and the chapter is concluded with the simulation results.

In chapter 5, an on-chip CDA design has been presented. With a brief introduction to CDA, the chapter outlines the design of a DSM based CDA. The design of full-bridge power stage has been outlined along with the driving schemes. Simulation results are presented at the end of the chapter.

Conclusion are drawn in chapter 6, along with the scope for future research.

Chapter 2

INVERTER-BASED OTA AND ITS DESIGN ANALYSIS

2.1 CMOS INVERTER AS AN OTA

A simple CMOS inverter formed using a NMOS and a PMOS, shown in Figure 2.1a, can act as single-ended amplifier. The slope of the voltage transfer characteristics (VTC) at a given point on the VTC is gain offered by amplifier. Therefore, to obtain maximum gain for a given inverter, the operating point should be at a point on the VTC where the slope is maximum, as shown in Figure 2.1b. In this figure, it can be seen that the magnitude of the slope of VTC reaches maximum when the input V_i is set at the voltage V_{MID}. Or in other words, inverter when biased at V_{MID} offers the maximum gain.

Another point to note here is that the slope of VTC is negative at any operating point, due to which the output for an input sinusoid is 180° out of phase with respect to the input. Therefore, one can easily build a negative feedback around this amplifier by using a feedback network. If the gain offered by inverter amplifier is made sufficiently large enough, then the closed loop gain can be made to be solely decided by the feedback factor.

The small signal DC gain offered by the CMOS inverter in Figure 2.1a is given in (2.1) where g_{m1p} and g_{m1n} are the tranconductance of transistors $M1p$ and $M1n$

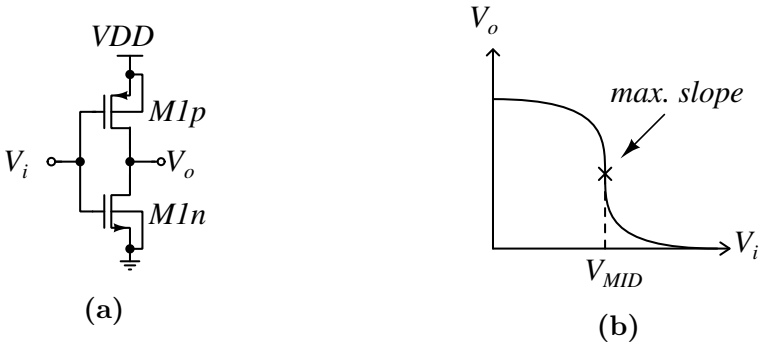

Figure 2.1: CMOS inverter(a) Schematic circuit (b) VTC

respectively and g_{o1p} and g_{o1n} are their output conductances.

$$A_{v,simple} = \frac{g_{m1p} + g_{m1n}}{g_{o1p} + g_{o1n}} \tag{2.1}$$

The gain $A_{v,simple}$ is not sufficiently large enough for the inverter to be used as an OTA. For the inverter designed in 180 nm a DC gain in the range 20-35 dB can only be expected. However, with some modifications and additional circuits the gain of the inverter can be enhanced. Cascoding technique, the common approach used to improve the output impedance of a transconductor, can be readily adopted to CMOS inverter amplifier too. Figure 2.2 shows the schematic circuit of a cascoded inverter. The resulting gain of the circuit is given in (2.2). Here, the two cascode bias voltages V_{biasp} and V_{biasn} should be additionally generated.

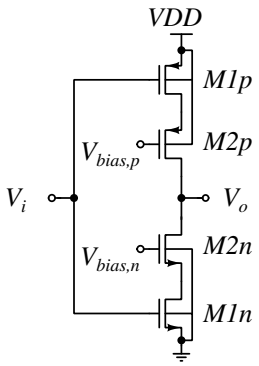

Figure 2.2: Schematic circuit of cascoded inverter (Luo et al. 2013b)

$$A_{v,cascode} = \frac{g_{m1p} + g_{m1n}}{\frac{g_{o1p}g_{o2p}}{g_{m2p}} + \frac{g_{o1n}g_{o2n}}{g_{m2n}}} \tag{2.2}$$

The DC gain can further be increased by employing gain-boosting technique with the help of two amplifiers of gains $-A_p$ and $-A_n$ realized using a common-source stage. Schematic of this modified amplifier is shown in Figure 2.3 and the overall gain is given in (2.3)

$$A_{v,gain\,boost} = \frac{g_{m1p} + g_{m1n}}{\frac{g_{o1p}g_{o2p}}{g_{m2p}A_p} + \frac{g_{o1n}g_{o2n}}{g_{m2n}A_n}} \tag{2.3}$$

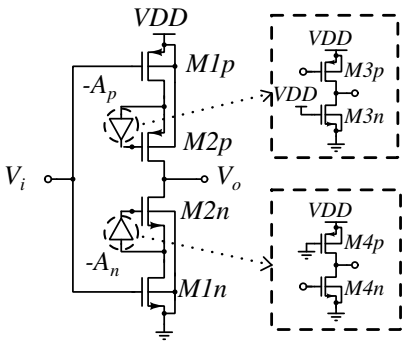

Figure 2.3: Schematic of an inverter with gain-boosting (Luo et al. 2013b)

The gate-source voltage of transistors $M1p$ and $M1n$, when the input is set at V_{MID} is,

$$V_{SG,1p} = V_{DD} - V_{MID} \tag{2.4}$$

$$V_{GS,1n} = V_{MID} \tag{2.5}$$

V_{MID} and V_{DD} are the voltages that sets the bias for $M1p$ and $M1n$ which in turn sets the quiescent current in the inverter. For low power applications, the quiescent current should be kept at low values. Often, low quiescent current is set by maintaining the transistors in the weak inversion region. Operating the transistors in weak inversion has another advantage, which is, for a given drain current, the transconductance offered by the transistor is higher than that of the transistor operated in strong inversion. This is explained as follows.

Consider an NMOS transistor operated in strong inversion region ($V_{GS} > V_{TH}$) and biased in saturation ($V_{DS} \geq V_{GS} - V_{TH}$). Where V_{GS} is the gate-source bias

voltage, V_{DS} is the drain-source voltage and V_{TH} is the threshold voltage of the transistor. The transconductance of the transistor, for a given aspect ratio, is given by (2.6)

$$g_{m,SI} = \frac{2I_D}{(V_{GS} - V_{TH})} \tag{2.6}$$

Where I_D is the drain current.

For a transistor operated in weak inversion, the transcondutance offered by the transistor is approximated as in (2.7)

$$g_{m,WI} = \frac{I_D}{\eta V_T} \tag{2.7}$$

Where, V_T is the volt-equivalent of temperature (or thermal voltage) having a value $\approx$26 mV at room temperature. $\eta = \frac{C_{ox}+C_{dep}}{C_{ox}}$ and it is a process dependent parameter ($\approx$2/3 in weak inversion).

Assuming that the gate overdrive $V_{GS} - V_{TH}$ is maintained at atleast 100 mV, from (2.6) and (2.7), it can be clearly inferred that $g_{m,WI}$ can easily be more than three times of $g_{m,SI}$. Therefore, operating transistor in weak inversion has a clear advantage of power and gain. However, this comes at the expense of signal swing.

For maintaining the transistors in weak inversion it is required that $|V_{GS}| \leq |V_{TH}|$. This requirement poses serious limitation on the maximum V_{DD} that can be used i.e., $V_{DD} < V_{TH,n} + |V_{TH,p}|$. At higher supply voltages, $|V_{GS}| \geq |V_{TH}|$ and the transistors cannot be operated in weak inversion. The quiescent current through $M1p$ and $M1n$ transistors can be significantly high since their gate overdrive voltage can be quite high or in other words, to achieve a given transconductance (g_m), these inverters have to burn more power than in the case when they are operated in weak inversion. Therefore, these inverters are not power efficient at higher supply voltages and hence not suitable for low power applications.

This research proposes an architecture for inverter-based OTA to realize high DC gain while keeping the quiescent current to a low value.

2.2 PROPOSED OTA

In order to retain the advantages of operating the inverter in weak inversion even when operated at higher supply voltage, two source follower circuits with active load have been added to the signal path. The complete schematic of the proposed inverter-based gain-boosted OTA (IGB-OTA) is shown in Figure 2.4. Cascoding and gain-boosting techniques are used to achieve a higher DC gain. The PMOS and NMOS transistors, $M1p$ and $M1n$ respectively, form the inverter. The inverter transistors are cascoded with $M4p$ and $M4n$ to increase the effective output impedance of the inverter and thereby achieves a higher small signal voltage gain. The gain is further improved using gain-boosting technique (Bult and Geelen 1990). Common-source amplifiers formed by transistors $M5p$, $M6n$ and $M6p$, $M5n$ offer gain-boosting.

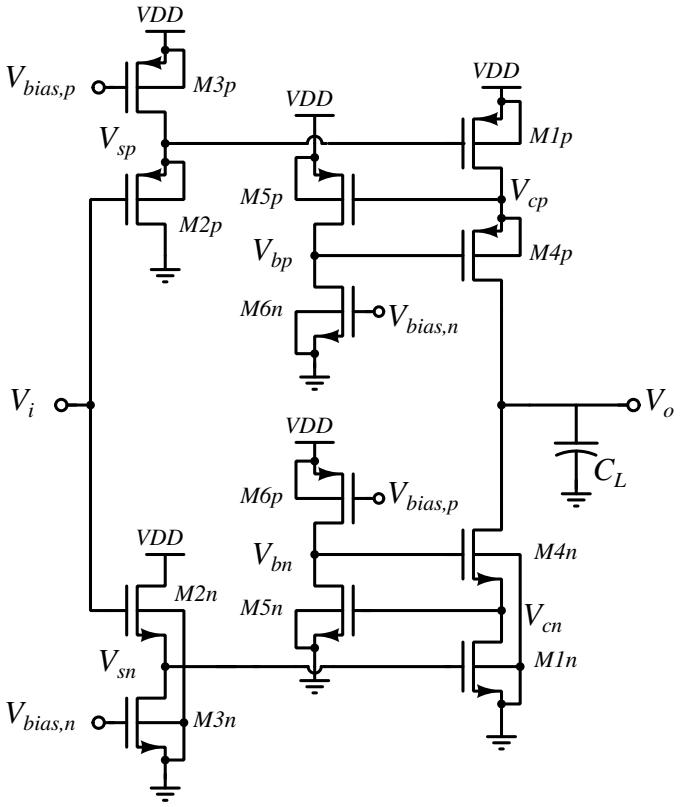

Figure 2.4: Schematic of the proposed IGB-OTA

Two source follower circuits with active load, formed using $M2p$, $M3p$ and $M2n$, $M3n$, are used to level shift the input common-mode before applying to the main

inverter transistors $M1p$ and $M1n$. Their main role is to bias $M1p$ and $M1n$ in sub-threshold region and thus limit the inverter quiescent current. Note that, each source follower stage adds an additional pole to the overall OTA. It is necessary to place these poles, from both the source followers, beyond UGB of the OTA. This requirement makes the quiescent current consumption of the source follower stages to be higher than that of the main inverter. However, the overall power consumption can be designed to be lower than in the case when the inverter is directly operated at higher supply voltage. This calls for a careful biasing and sizing of source follower transistors to ensure stability.

2.2.1 Small Signal Analysis

An incremental circuit of Figure 2.4 is shown in Figure 2.5. A_{sp} and A_{sn} are the small

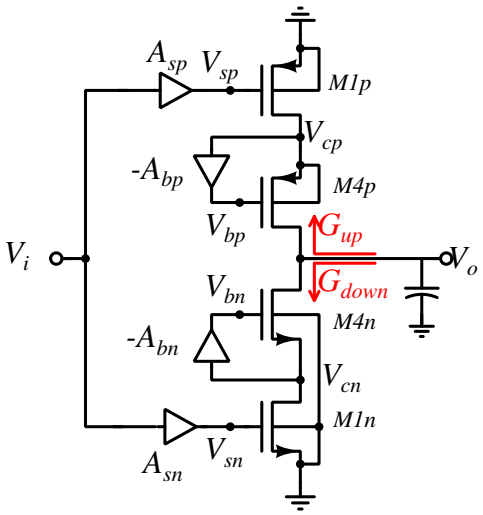

Figure 2.5: Incremental Circuit of proposed IGB-OTA

signal voltage gains of PMOS and NMOS level shifters (source followers) respectively. A_{bp} and A_{bn} are the small signal voltage gains of gain-boosting amplifiers (common-

source) for PMOS and NMOS cascode transistors respectively.

$$A_{sp} = \frac{g_{m_{2p}}}{(g_{m_{2p}} + g_{o_{2p}} + g_{o_{3p}})} \tag{2.8}$$

$$A_{sn} = \frac{g_{m_{2n}}}{(g_{m_{2n}} + g_{o_{2n}} + g_{o_{3n}})} \tag{2.9}$$

$$A_{bp} = -\frac{g_{m_{5p}}}{(g_{o_{5p}} + g_{o_{6n}})} \tag{2.10}$$

$$A_{bn} = -\frac{g_{m_{5n}}}{(g_{o_{6p}} + g_{o_{5n}})} \tag{2.11}$$

The overall transconductance G_m and overall output conductance G_{out} are given in (2.12) and (2.13) respectively.

$$G_m = -(g_{m_{1p}} A_{sp} + g_{m_{1n}} A_{sn}) \tag{2.12}$$

$$G_{out} = G_{up} + G_{down} \tag{2.13}$$

Overall gain of the the proposed single-ended IGB-OTA is given by (2.14).

$$A_v = \frac{G_m}{G_{out}} = -\frac{(g_{m_{1p}} A_{sp} + g_{m_{1n}} A_{sn})}{(G_{up} + G_{down})} \tag{2.14}$$

where G_{up} and G_{down} are the conductances seen up and down at the output node as shown in Figure 2.5, and are given by (2.15) and (2.16)

$$G_{up} \approx \frac{g_{o_{1p}} g_{o_{4p}}}{g_{m_{4p}} A_{bp}} \tag{2.15}$$

$$G_{down} \approx \frac{g_{o_{1n}} g_{o_{4n}}}{g_{m_{4n}} A_{bn}} \tag{2.16}$$

In all the equations, $g_{m_{xy}}$ and $g_{o_{xy}}$ represent the small signal transconductance and output conductance of the transistor Mxy respectively. From (2.14), it can be found that the DC gain is the product of three intrinsic gains of the transistors and with a careful design, a DC gain in excess of 90 dB can be easily achieved. Please note that, in the above analysis, body effect is assumed to be negligible.

2.2.2 Stability Analysis:

The proposed IGB-OTA is intended to be used in SC circuits where, the OTA is used in negative feedback configuration. Therefore, it is important to analyze the stability of the OTA and provide a design strategy for ensuring stability. As evident from the control theory, the location of the open loop poles of the OTA decides the closed loop stability. It is common to make OTA's frequency response to follow a first order response within its UGB. However, the proposed IGB-OTA has at-least seven poles and can be listed as below.

- One pole at the output node, V_o. It is preferred, here, to have this pole as a dominant pole.
- Two poles at the cascode nodes i.e., one each at nodes V_{cp} and V_{cn} in Figure 2.4.
- Two poles in the gain-boosting stage i.e., one each at nodes V_{bp} and V_{bn}
- Two poles in level shifter stage. i.e., one each at nodes V_{sp} and V_{sn}

In this section, effect of these poles on the response is analyzed. Since there are two identical signal paths in the proposed IGB-OTA (one from the upper half, through nodes $V_i \rightarrow V_{sp} \rightarrow V_{cp} \rightarrow V_o$ and the other from the lower half, through nodes $V_i \rightarrow V_{sn} \rightarrow V_{cn} \rightarrow V_o$), it would be sufficient and convenient to analyze the effect of poles in any one path. Accordingly, the analysis has been carried for the lower half through nodes $V_i \rightarrow V_{sn} \rightarrow V_{cn} \rightarrow V_o$ for which the incremental circuit is shown in Figure 2.6. And for the ease of mathematical analysis, the upper half section of the IGB-OTA is assumed to be identical to the lower half section.

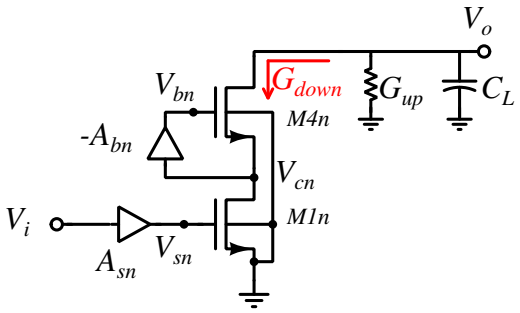

Figure 2.6: Incremental Circuit of lower half of the proposed IGB-OTA

2.2.2.1 Output pole (p_1)

The pole at the output node is a simple and real pole located at

$$p_1 = -\omega_1 = -\frac{G_{out}}{C_{out}} = -\frac{2\,G_{down}}{C_{out}} = -\frac{2\,g_{o_{1n}}g_{o_{4n}}}{g_{m_{4n}}A_{bn}C_{out}} \tag{2.17}$$

where C_{out} is the capacitance at the output node. This pole is intended to be made dominant. If the effect of other poles is made negligible at least up to UGB, then the transfer function of the IGB-OTA can be approximated as in (2.18),

$$A_{tot}(s) \approx \frac{A_{o,tot}}{1+\frac{s}{\omega_1}} \tag{2.18}$$

where,

$$A_{o,tot} = -\frac{2\,g_{m_{1n}}A_{sn}}{2\,G_{down}} \approx -\frac{g_{m_{1n}}A_{sn}g_{m_{4n}}A_{bn}}{g_{o_{1n}}g_{o_{4n}}} \tag{2.19}$$

ω_1 is the 3-dB bandwidth and $|A_{o,tot}|$ is the DC gain. UGB of the OTA in radians (ω_u) is then given as in (2.20).

$$\omega_u = \frac{|G_m|}{C_{out}} \tag{2.20}$$

Optimistically, if a DC gain of 100 dB is assumed, then it may be approximated that ω_u is 5 decades apart from ω_1, for a first order (-20 dB/decade roll-off) response.

2.2.2.2 Pole at node V_{cn} (p_2)

The pole at node V_{cn} is also a simple and real pole given by (2.21)

$$p_2 = -\omega_2 = -\frac{g_{o_{1n}}}{C_{v_{cn}}} \tag{2.21}$$

where $C_{v_{cn}}$ is effective capacitance at the node V_{cn}.
Taking the ratio of ω_2 to ω_1,

$$\frac{\omega_2}{\omega_1} = \frac{g_{m_{4n}}A_{bn}}{2\,g_{o_{4n}}}\frac{C_{out}}{C_{v_{cn}}} \tag{2.22}$$

From (2.22), it can be clearly seen that with C_{out} being the output capacitor

of the order of picofarads and $C_{v_{cn}}$ being the parasitic capacitance of the order of femtofarads, ω_2 can easily be more than five orders of magnitude when compared to ω_1. Or in other words, pole p_2 will effect the frequency response only beyond the UGB.

2.2.2.3 Pole at node V_{bn} (p_3)

Let us assume that A_{sn} is frequency independent. The gain-boosting amplifier A_{bn} is a single pole system and its transfer function can be written as,

$$A_{bn}(s) \approx \frac{A_{o,bn}}{1 + \frac{s}{\omega_3}} \tag{2.23}$$

where $A_{o,bn}$ and ω_3 are given by (2.24) and (2.25).

$$A_{o,bn} = -\frac{g_{m_{5n}}}{g_{o_{5n}} + g_{o_{6p}}} \tag{2.24}$$

$$\omega_3 = \frac{g_{o_{5n}} + g_{o_{6p}}}{C_{vbn}} \tag{2.25}$$

where C_{vbn} is the effective capacitance at node V_{bn}. The pole contributed by the node V_{bn} is at $p_3 = -\omega_3$ and is simple and real.
Substituting (2.23) in (2.17) and (2.19), the overall transfer function $A_{tot}(s)$ given in (2.18) takes the form as shown in (2.26)

$$A_{tot}(s) \approx \frac{A_{o,tot}}{1 + s\left(\frac{1}{\omega_1} + \frac{1}{\omega_3}\right)} \tag{2.26}$$

It is to be noted that even with the gain-boosting amplifier having a single-pole, the overall system offers a single pole response. However, the pole of the gain-boosting amplifier degrades the bandwidth (and hence UGB) of the IGB-OTA, which is not desired. If at all, the dependency of 3-dB bandwidth of IGB-OTA on ω_3 is to be made negligible, ω_3 should be chosen such that $\omega_3 >> \omega_1$. Importantly, it is sufficient if ω_3 is placed two decades apart from ω_1. Also, it is to be observed that with ω_u being five decades apart from ω_1, bandwidth requirement of the gain-boosting amplifier A_{bn} is relaxed to a large extent and hence the power requirement on A_{bn}.

2.2.2.4 Pole at node V_{sn} (p_4)

Source follower stage A_{sn} is a single pole system and its transfer function can be written as

$$A_{sn}(s) = \frac{A_{o,sn}\left(1+\frac{s}{\omega_z}\right)}{1+\frac{s}{\omega_4}} \tag{2.27}$$

where,

$$A_{o,sn} = \frac{g_{m_{2n}}}{g_{m_{2n}} + g_{o_{2n}} + g_{o_{3n}}} \tag{2.28}$$

The transfer function has a zero at $s = -\omega_z$ and a pole at $s = -\omega_4$ given by (2.29) and (2.30) respectively.

$$\omega_z = \frac{g_{m_{2n}}}{C_{gs,2n}} \tag{2.29}$$

$$\omega_4 = \frac{g_{m_{2n}} + g_{o_{3n}}}{C_{gs,2n} + C_{vsn}} \tag{2.30}$$

where $C_{gs,2n}$ is the gate-source capacitance of $M2n$ and C_{vsn} is the effective capacitance at node V_{sn} with respect to ground. Clearly, from (2.29) and (2.30), $\omega_z > \omega_4$. It is therefore required that ω_4 be placed beyond UGB in order to restrict the response to single-pole response. i.e.

$$\omega_4 > \omega_u \tag{2.31}$$

$$\frac{g_{m_{2n}} + g_{o_{3n}}}{C_{gs,2n} + C_{vsn}} > \frac{|G_m|}{C_{out}} \tag{2.32}$$

ω_4 can be pushed higher only by increasing $g_{m_{2n}}$. Therefore, it is imperative to burn power comparable to that of main inverter, if not less. Thus, source follower, in fact, poses a limit on reducing the power of the IGB-OTA. Or in other words, for low bandwidth applications where the required UGB is low, the source follower stage can be designed to consume low power, thus reducing the overall power of the IGB-OTA.

2.2.3 Noise Analysis

In this section, the intrinsic noise of the proposed IGB-OTA is analyzed.

The thermal noise of a MOSFET can be modelled by a current source connected

between drain and source terminals and its mean squared value over a bandwidth of one hertz is given as in (2.33).

$$\overline{I_{n,th}^2} = 4kT\gamma g_m \tag{2.33}$$

where k is the Boltzman constant, T is the temperature in kelvin, γ is 2/3 for MOSFET in saturation and 1/2 for MOSFET in sub-threshold.

The flicker noise of a MOSFET can also be modeled by a current source connected between drain and source terminals and its mean squared value is given as in (2.34).

$$\overline{I_{n,1/f}^2} = \frac{K}{C_{ox}WL}\frac{1}{f} \tag{2.34}$$

2.2.3.1 Noise contribution of main inverter

- **Noise contribution of main inverter transistor $M1n$:** The input referred noise voltage due to $M1n$ transistor, with the assumption that source follower is offering unity gain, can be written as

$$\overline{V_{n,in,1n}^2} \approx \frac{kT\gamma}{g_{m1n}} + \frac{K}{4C_{ox}W_{1n}L_{1n}}\frac{1}{f} \tag{2.35}$$

  Similarly, the input referred noise voltage due to $M1p$ transistor is

$$\overline{V_{n,in,1p}^2} \approx \frac{kT\gamma}{g_{m1p}} + \frac{K}{4C_{ox}W_{1p}L_{1p}}\frac{1}{f} \tag{2.36}$$

2.2.3.2 Noise contribution of cascode transistors and gain-boosting transistors

The noise contribution of the cascode transistors and the gain-boosting stage is relatively negligible compared to $M1n$ (Luo et al. 2013b) and therefore ignored.

2.2.3.3 Noise contribution of source follower stage

Input referred voltage noise due to NMOS source follower can be written as

$$\overline{V_{n,in,sn}^2} \approx kT\gamma\left(\frac{1}{g_{m2n}} + \frac{g_{m3n}}{g_{m2n}^2}\right) + \frac{K}{4C_{ox}fg_{m2n}^2}\left(\frac{1}{W_{2n}L_{2n}} + \frac{1}{W_{3n}L_{3n}}\right) \tag{2.37}$$

Similarly, the input referred noise voltage due to PMOS source follower is

$$\overline{V_{n,in,sp}^2} \approx kT\gamma\left(\frac{1}{g_{m2p}} + \frac{g_{m3p}}{g_{m2p}^2}\right) + \frac{K}{4C_{ox}fg_{m2p}^2}\left(\frac{1}{W_{2p}L_{2p}} + \frac{1}{W_{3p}L_{3p}}\right) \tag{2.38}$$

The total input referred voltage noise of the IGB-OTA

$$\overline{V_{n,in,tot}^2} \approx \overline{V_{n,in,1n}^2} + \overline{V_{n,in,1p}^2} + \overline{V_{n,in,sn}^2} + \overline{V_{n,in,sp}^2} \tag{2.39}$$

From the noise perspective, the following points can be made with respect to the design of IGB-OTA.

- g_m of the source follower input transistors i.e., $M2n$ and $M2p$ have to be chosen large to minimize the noise from the source follower. For the transistors operated in sub-threshold region, g_m will be limited by the power constraints (since, $g_m = I_D/\eta V_T$).
- $1/f$ noise can be minimized by choosing large gate area for $M1n$, $M1p$, $M2n$, $M2p$, $M3n$ and $M3p$.

2.3 DESIGN STEPS FOR A GIVEN APPLICATION

In this section, a detailed procedure for designing IGB-OTA is outlined. As already mentioned earlier in this chapter, the proposed IGB-OTA is targeted for switched capacitor integrator. For designing, the following parameters (specification) are taken as the input.

- Clock frequency (f_{clk}) at which the integrator is expected to operate.

- The effective load capacitance (C_L) the OTA is expected to drive.

The following are the steps for designing the proposed IGB-OTA for the above mentioned input specifications.

1. **Deciding on the UGB requirement for the IGB-OTA:**
   In switched capacitor applications, the UGB of the OTA determines the settling accuracy of the integrator output. If the UGB is insufficient, then the integrator output will not settle to the desired final value resulting in a dynamic error. The UGB of the OTA should be at least two times the integrator operating clock frequency, for keeping the settling error tolerance to 0.1% (Quinn and van Roermund 2007). However, it is common to choose UGB at least thrice or more than the clock frequency i.e.

$$\text{UGB} > 3\,(2\pi f_{clk}) \tag{2.40}$$

2. **Overall transconductance (G_m):**
   Once the UGB for a given application is known, the overall transconductance required for the IGB-OTA can be determined from UGB using (2.20) as follows

$$G_m = \text{UGB}.C_L \tag{2.41}$$

   For the proposed IGB-OTA, the overall transconductance is given by

$$\begin{aligned} G_m &= g_{m_{1p}} A_{sp} + g_{m_{1n}} A_{sn} && (2.42)\\ &\approx g_{m_{1p}} + g_{m_{1n}} && (2.43) \end{aligned}$$

   If the transconductances of PMOS and NMOS transistors are assumed to be equal, then

$$g_{m_{1p}} = g_{m_{1n}} = \frac{G_m}{2} \tag{2.44}$$

   Since, $M1n$ and $M1p$ are operated in sub-threshold, the drain current requirement on them can be calculated as

$$I_D = g_m \eta V_T \tag{2.45}$$

3. **Sizing of main inverter transistors $M1p$ and $M1n$:**
   $M1p$ and $M1n$ transistors have to be biased such that they operate in sub-threshold region. This is done by the respective source follower circuits. The gate-source voltage of $M1p$ and $M1n$ are chosen such that they operate in sub-threshold, preferably just below their respective threshold voltages $V_{TH,p}$ and $V_{TH,n}$. The transistors are then sized to carry the required drain current and to achieve the desired transconductance as in (2.44). Note that, choosing sufficiently large gate area is key for minimizing $1/f$ noise for low frequency applications.

4. **Sizing of cascode transistors $M4p$ and $M4n$:**
   For sizing cascode transistors, there are no hard requirements. However, choosing $M4p$ and $M4n$ to have same size as that of $M1p$ and $M1n$ transistors respectively is a good design practice.

5. **Sizing of transistors in the gain-boosting stages:**
   From section 2.2.2.3, it is clear that the design specification of gain-boosting stage is quite relaxed and therefore it can be optimized for power. The bias voltages $V_{bias,n}$ and $V_{bias,p}$ are chosen such that $M6n$ and $M6p$ transistors are operated in sub-threshold region. These transistors are sized in such a way that the quiescent current is sufficiently low when compared to the main inverter current, but sufficient enough to get a decent gain. Transistors $M5n$ and $M5p$ are sized appropriately to keep them in sub-threshold region.

6. **Sizing of transistors in the source follower stages**
   It has been shown in section 2.2.2.4 that the pole contributed by the source follower stage should be placed beyond the UGB of the IGB-OTA, to ensure sufficient phase margin. This can be achieved by choosing the transconductance of $M2p$ and $M2n$ appropriately, as seen from (2.30). Also note that, these transistors are responsible for level-shifting the input common-mode voltage ($V_{in,CM}$) for biasing the NMOS and PMOS input transistors of the main inverter.

Therefore the requirement on $M2p$ and $M2n$ are,

$$V_{sg,2p} = V_{DD} - V_{sg,1p} - V_{in,CM} \tag{2.46}$$

$$g_{m2p} > (g_{m1p} + g_{m1n}) \left(\frac{C_{gs,2p} + C_{vsp}}{C_{OUT}} \right) \tag{2.47}$$

$$V_{gs,2n} = V_{DD} - V_{gs,1n} - V_{in,CM} \tag{2.48}$$

$$g_{m2n} > (g_{m1p} + g_{m1n}) \left(\frac{C_{gs,2n} + C_{vsn}}{C_{OUT}} \right) \tag{2.49}$$

From (2.46) and (2.48), it is clear that, the requirement on $V_{sg,2p}$ and $V_{gs,2n}$ is fixed, once the main inverter design is freezed. Therefore, design of source

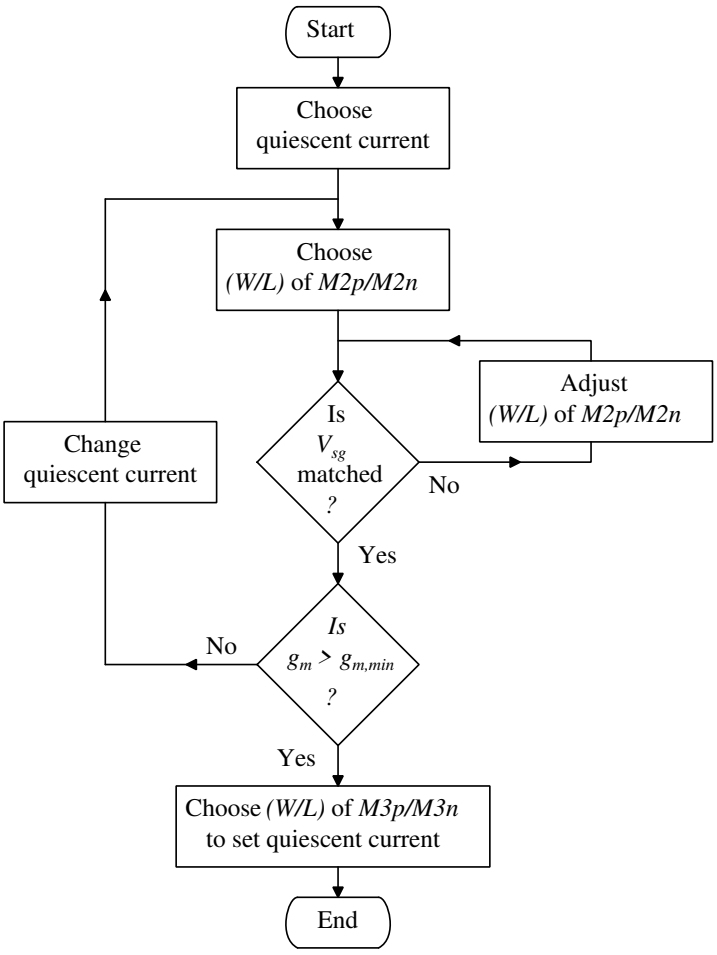

Figure 2.7: Flowchart for sizing the source follower circuit

followers boils down to choosing appropriate quiescent current and sizes for

of $M2p$ and $M2n$, meeting the in-equality given in (2.47) and (2.49), derived from (2.32). The design can be started by choosing the quiescent current for the source follower. Setting the source follower quiescent current equal to that of main inverter is a good starting point. The procedure to be followed is outlined in the form of a flowchart in Figure 2.7. Once the design is complete, the power can be reduced further by reducing the quiescent current (following the flowchart) if there is a sufficient margin available for g_{m2p} and g_{m2n}.

7. **Deciding on DC Gain:**
   DC gain of an OTA in a SC integrator determines the accuracy of charge transfer. A finite DC gain introduces static error at the output of integrator. In order to minimize the effect of static error on the performance of the overall system, DC gain in excess of 80 dB is desired for switched capacitor applications (Pavan et al. 2017). The proposed IGB-OTA can easily achieve a DC gain in excess of 90 dB with careful sizing and biasing of transistors.

2.4 SWITCHED CAPACITOR INTEGRATOR USING IGB-OTA

The proposed IGB-OTA is intended for switched capacitor applications. The single-ended architecture with a negative gain makes is readily available to be put in negative feedback. Figure 2.8a shows a parasitic insensitive single-ended switched capacitor integrator realized using the IGB-OTA. C_s is the sampling capacitor used for sampling the input signal and C_i is the integrating capacitor that accumulates the charge transferred from C_s in every clock cycle. The integrator employs auto-zeroing technique to cancel the OTA's offset and also helps in reducing the OTA's low frequency 1/f noise (Huijsing et al. 2013).

The SC integrator uses 4 different clock phases for its operation as shown in Figure 2.8b. ϕ_{1d} and ϕ_{2d} are the delayed versions of ϕ_1 and ϕ_2, in the sense that they are delayed at the falling edges.

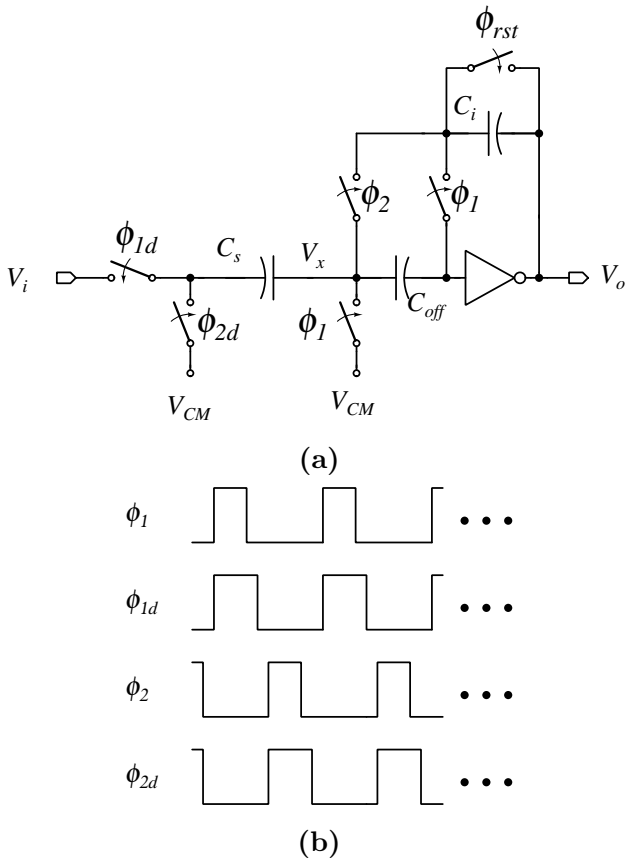

Figure 2.8: (a) A parasitic insensitive single-ended SC integrator (Luo et al. 2013b) and its (b) Clock phases

2.4.1 Operation of SC Integrator

The input V_i to the integrator is assumed to be a signal riding on a common-mode voltage V_{CM} i.e., $V_i = V_{CM} + v_i$, where v_i is the signal component. Initially the integrating capacitor C_i is discharged using ϕ_{rst}. This is a one time operation, typically performed as soon as the power supply is turned ON. In ϕ_1 phase (Figure 2.9a), input v_i is sampled onto the sampling capacitor C_s. At the same time the offset storage capacitor C_{off} stores the offset voltage i.e., the voltage difference between OTA's input DC bias voltage (V_{MID}) and V_{CM}. Note that, though inverter can be designed to offer V_{MID} equal to the desired V_{CM}, it is very difficult to maintain it across process, voltage and temperature.

In ϕ_2 phase (Figure 2.9b), C_{off} holds the offset voltage, making the node V_x act as a virtual ground and therefore the entire charge in C_s is transferred to C_i, which

holds its charge during ϕ_1 phase.

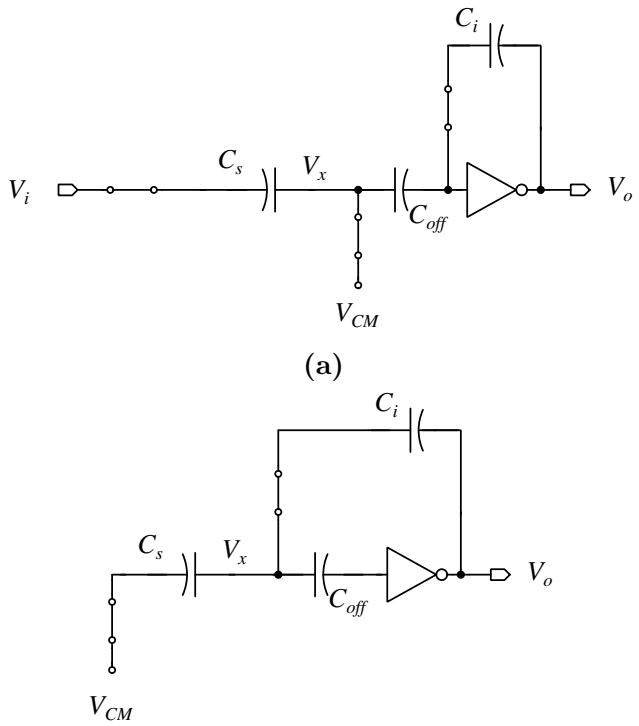

Figure 2.9: (a) ϕ_1 phase (b) ϕ_2 phase of integrator

The output of integrator v_o ($V_o = V_{CM} + v_o$) at the end of k^{th} clock cycle can be expressed mathematically, in time domain, as given in (2.50). The transfer function of the SC integrator in the z-domain is given by (2.51) (Allen and Holberg 2011)

$$v_o[k] = v_o[(k-1)] \; + \; v_i[(k-1)] \left(\frac{C_s}{C_i}\right) \tag{2.50}$$

$$\frac{V_o(z)}{V_i(z)} = \frac{C_s}{C_i}\left(\frac{z^{-1}}{1-z^{-1}}\right) \tag{2.51}$$

A point to be noted here is that, often, it is desired that, output common-mode voltage be set equal to that of the input common-mode voltage. This enables one integrator to drive a similar integrator. This can be easily achieved in a differential operation.

2.4.2 Pseudo-differential Switched Capacitor Integrator

The application of the proposed IGB-OTA in a differential SC integrator has been presented in this section. The IGB-OTA being single-ended, differential operation can only be achieved by connecting two IGB-OTA's in pseudo-differential fashion. Figure 2.10 shows a parasitic insensitive pseudo-differential switched capacitor integrator using an inverter-based OTA (Luo et al. 2013b). It also has a common-mode feedback (CMFB) circuit to ensure that the output common-mode voltage of the integrator is equal to that of the input common-mode voltage i.e., V_{CM}.

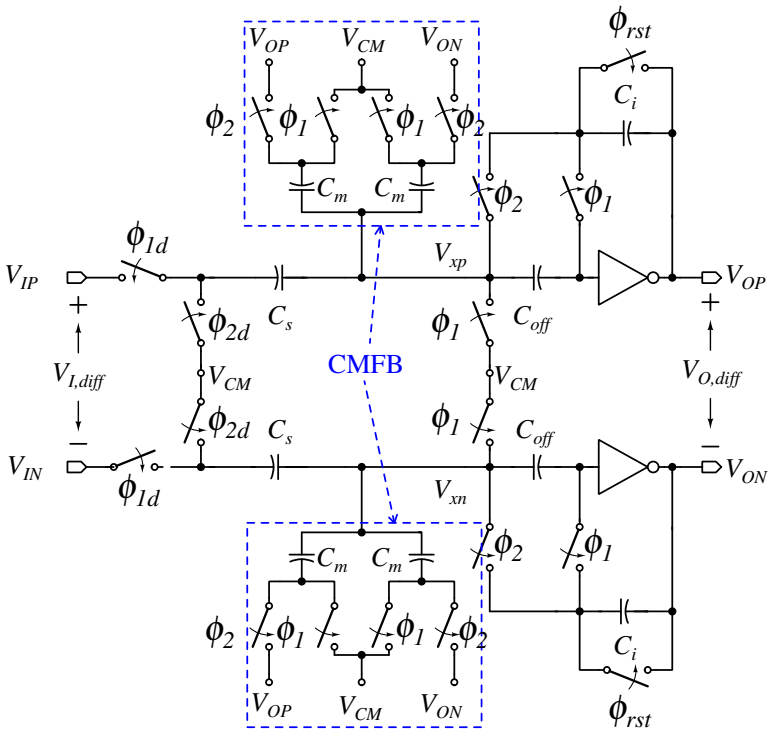

Figure 2.10: A parasitic insensitive pseudo-differential SC integrator (Luo et al. 2013b)

2.4.2.1 Operation of CMFB Circuit

Operation of the CMFB circuit is explained with the help of top half-circuit of the pseudo-differential integrator, shown in Figure 2.10. The CMFB circuit operates in two phases. In ϕ_1 phase, the bottom plates of the two CMFB capacitors (C_m) are connected to the common-mode reference voltage (V_{CM}). In ϕ_2 phase, the bottom

plates are connected to the outputs, V_{op} and V_{on}, of the pseudo-differential integrator. The equivalent half-circuits during the two phases are given in Figure 2.11a and Figure 2.11b respectively.

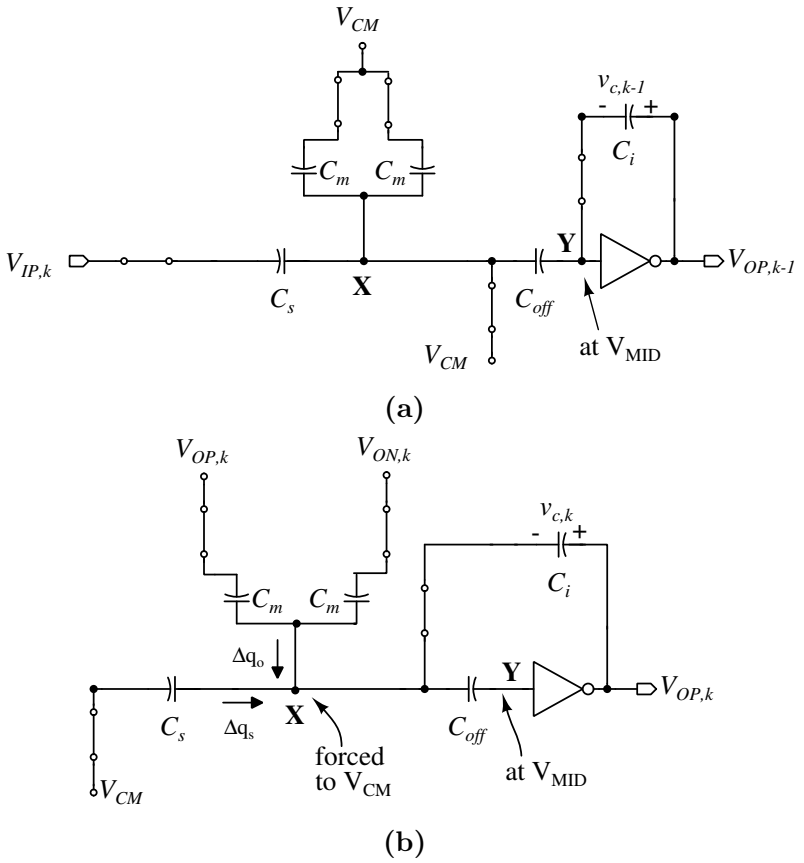

Figure 2.11: Equivalent half-circuit of the differential integrator during (a) ϕ_1 phase (b) ϕ_2 phase

If the IGB-OTA is assumed to have an infinite gain then the input node of IGB-OTA in the integrator circuit will settle to V_{MID} whenever IGB-OTA is connected in a negative feedback. In Figure 2.11, it can be seen that the IGB-OTA is always in negative feedback configuration (in both phases). Therefore, for the differential integrator it can be conveniently assumed that the input of IGB-OTA is always at V_{MID}.

During ϕ_1 phase in the k^{th} cycle, let us assume that the input is fully differential

as defined in (2.52) and (2.53) and is constant (for simplicity).

$$V_{IP,k} = V_{CM} + v_{i,k} \tag{2.52}$$

$$V_{IN,k} = V_{CM} - v_{i,k} \tag{2.53}$$

From Figure 2.11a it can be seen that C_s acquires a charge corresponding to the input $v_{i,k}$ and C_ms are discharged. C_{off} holds the voltage difference between V_{CM} and V_{MID}, and the integrating capacitors hold the charge acquired at the end of $(k-1)^{\text{th}}$ cycle.

During ϕ_2 phase, since C_{off} cannot loose its charge as there is no path for its charge to flow and therefore the node X is maintained at V_{CM}. At node X, the charges on C_s, C_i and C_m's get redistributed among themselves.

The total charge transferred to the top plate of C_i during ϕ_2 phase has two components, Δq_o from the capacitors C_m and Δq_s from C_s. A careful observation reveals that, the component Δq_o is the result of only small-signal common-mode component of the output (differential-mode component from each of the C_ms are effectively cancelled at node X). The component Δq_s correspond to the differential component of the input. Therefore, the circuit can be analysed separately for common-mode and differential-mode components, and the corresponding equivalent circuits are shown in Figure 2.12.

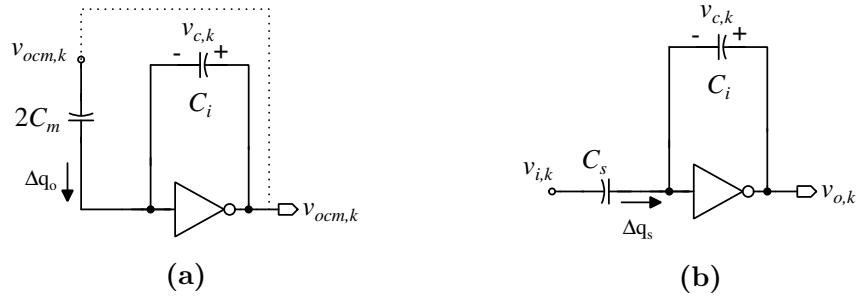

Figure 2.12: Simplified small-signal equivalent half-circuit of the differential integrator during ϕ_2 phase for (a) common-mode (b) differential-mode

Considering Figure 2.12a, the voltage $v_{c,k}$ across C_i due to charge Δq_o is given by.

$$\begin{aligned} v_{c,k} &= \frac{-\Delta q_o}{C_i} \\ &= \frac{2C_m}{C_i} v_{ocm,k} \end{aligned} \tag{2.54}$$

The input of the IGB-OTA is maintained at small signal ground during ϕ_2 (node X is forced to common-mode bias voltage V_{CM}). Therefore one can write,

$$v_{ocm,k} = v_{c,k} \tag{2.55}$$

From (2.54) and (2.55), it can be easily seen that the only possible solution for $v_{ocm,k}$ is that $v_{ocm,k}$=0. Or in other words, even if C_i is assumed to have acquired some common-mode charge during the previous cycle or during phase ϕ_1 of the current cycle, the CMFB network ensures that in ϕ_2 phase all such common-mode charges are removed from C_i.

However it must be ensured that Δq_o should be kept to a value such that it does not overcharge C_i in which case the CMFB loop becomes unstable. Ideally, choosing $2C_m = C_i$ will help in a very quick removal of common-mode charges. However, the effective load on the IGB-OTA increases necessitating the IGB-OTA to have a higher UGB. On the other hand, by choosing $2C_m < C_i$, effective load on the IGB-OTA can be reduced. Accordingly a factor of 0.4 has been chosen for the ratio of $2C_m$ and C_i.

Now, for the charge Δq_s, as per the equivalent circuit shown in Figure 2.12b, it is transferred completely to C_i and thus accumulating on it. The resulting increment in the voltage across C_i is $\frac{-\Delta q_s}{C_i} = \frac{C_s}{C_i} v_{i,k}$.

Noting that node X is maintained at common-mode bias voltage V_{CM}, at the end of ϕ_2 phase, from Figure 2.11b, the output $V_{OP,k}$ can be written as

$$\begin{aligned} V_{OP,k} &= V_{CM} + v_{cp,k} && (2.56) \\ &= V_{CM} + v_{cp,(k-1)} + \frac{C_s}{C_i} v_{i,k} && (2.57) \end{aligned}$$

Similarly for the lower half of the differential integrator, the output $V_{ON,k}$ can be written in the form,

$$V_{ON,k} = V_{CM} + v_{cn,(k-1)} - \frac{C_s}{C_i} v_{i,k} \tag{2.58}$$

From (2.57) and (2.58), it can be inferred that the integrator outputs have a common-mode bias voltage V_{CM} as desired. The differential integrator output has only the differential component and is free from common-mode component.

Having proven the possibility of realizing inverter-based OTA's with gain more than 90 dB with low power and a scheme for the SC-integrator, the next task is to

design IGB-OTA's in one of the CMOS processes and prove its robustness. The next chapter presents the design of IGB-OTA's in 180 nm CMOS process and operating on 1.8 V supply.

Chapter 3

DESIGN OF PROPOSED IGB-OTA FOR BIOMEDICAL AND AUDIO APPLICATIONS

In this chapter, the proposed IGB-OTA has been designed for two applications having different bandwidth requirements.

- **Design-I:**
  The proposed IGB-OTA is designed for biomedical applications. The maximum signal bandwidth is considered to be 2 kHz, covering phonocardiography (PCG). (Webster 2009).

- **Design-II:**
  In this design, the proposed IGB-OTA is targeted for audio applications. The maximum signal bandwidth is taken as 20 kHz (Luo et al. 2013b).

Both the OTAs have been designed in UMC 180 nm standard CMOS process technology to operate on a supply voltage of 1.8 V. For the ease of understanding, UGB is quoted in Hz (i.e., $\frac{\omega_u}{2\pi}$) for the rest of the thesis.

3.1 IGB-OTA DESIGN-I (FOR BIOMEDICAL APPLICATIONS)

In the first design, the proposed IGB-OTA is optimized for biomedical applications. The maximum load capacitance is assumed to be 2.5 pF and the maximum clock frequency (f_{clk}) is considered to be 1 MHz (for an OSR of 250 assuming 2 kHz signal bandwidth). Therefore, one can arrive at the following requirements for the OTA.

- From (2.40), the minimum UGB required for IGB-OTA = 3 MHz.
- From (2.41), the minimum overall transconductance G_m required = 15π μS. So, the transconductance of $M1p$ and $M1n$ transistors required is at least 7.5π μS, assuming these two transistors contribute equally to the overall transconductance.

All the transistors in the proposed IGB-OTA are operated in sub-threshold region to minimize the power consumption. Table 3.1 shows the aspect ratio of all the transistors of IGB-OTA for this design.

Table 3.1: Aspect ratio of transistors for IGB-OTA Design-1

PMOS	$\left(\frac{W}{L}\right)$	N	NMOS	$\left(\frac{W}{L}\right)$	N
M1p	$\left(\frac{1.3}{0.48}\right)$	20	M1n	$\left(\frac{1.2}{0.54}\right)$	4
M2p	$\left(\frac{2.2}{0.36}\right)$	8	M2n	$\left(\frac{1}{0.36}\right)$	2
M3p	$\left(\frac{2.2}{0.36}\right)$	2	M3n	$\left(\frac{1}{0.36}\right)$	2
M4p	$\left(\frac{1.3}{0.2}\right)$	20	M4n	$\left(\frac{1.2}{2.4}\right)$	4
M5p	$\left(\frac{1.1}{0.4}\right)$	10	M5n	$\left(\frac{1.35}{0.36}\right)$	2
M6p	$\left(\frac{1.35}{0.54}\right)$	6	M6n	$\left(\frac{1.1}{4}\right)$	2

W and L are width and length in μm.

N is the number of fingers.

The bias voltages $V_{bias,p}$ and $V_{bias,n}$ are generated from common-mode voltage (V_{CM}). The schematic of the circuit generating these voltages is shown in Figure 3.1. $V_{bias,p}$ and $V_{bias,n}$ are chosen such that transistors $M3p$, $M6p$ and $M3n$, $M6n$ of IGB-OTA are maintained in sub-threshold region. Considering the V_{TH} of transistors,

$V_{bias,p}$ and $V_{bias,n}$ were chosen to be 1.3 V and 430 mV. The transistors of the bias generating circuits are sized to generate the desired bias voltages.

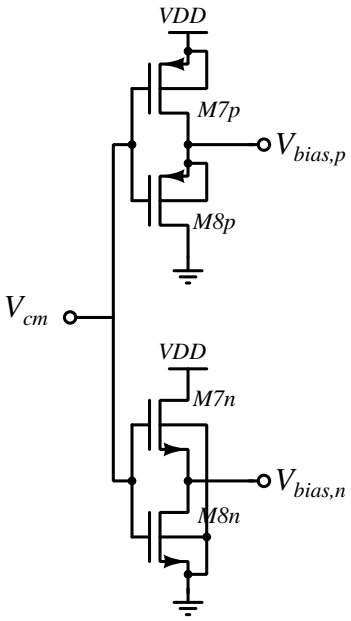

Figure 3.1: Biasing Circuit for IGB-OTA Design-I

The layout of the proposed IGB-OTA along with the biasing circuit is shown in Figure 3.2. Dummy transistors are added to maintain symmetry in the environment seen by each transistor finger. The layout occupies an area of 71.30 μm x 21.04 μm.

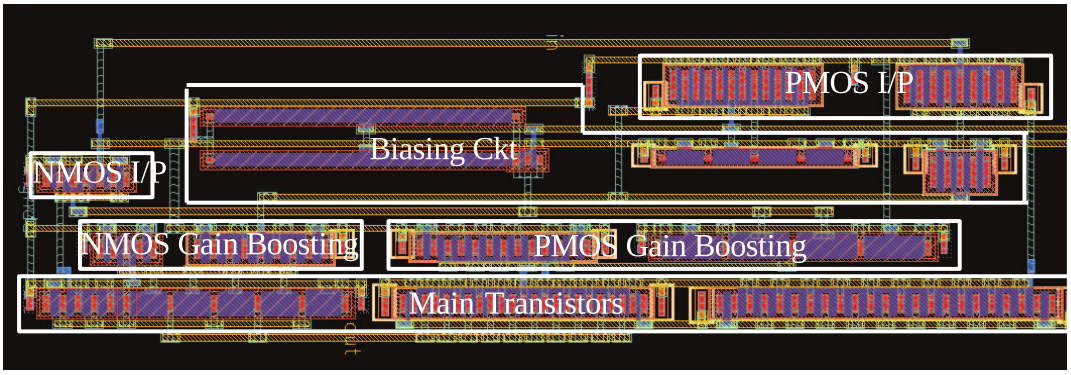

Figure 3.2: Layout of the proposed IGB-OTA for Design-I

3.1.1 Performance of IGB-OTA Design-I

The frequency response of IGB-OTA is shown in Figure 3.3 for a typical process corner, supply voltage and temperature. The DC gain offered by IGB-OTA is 109 dB with a UGB of 5.29 MHz (more than the minimum requirement of 3 MHz). The OTA has a very good phase margin of 81°. Note, this margin is without any explicit compensation.

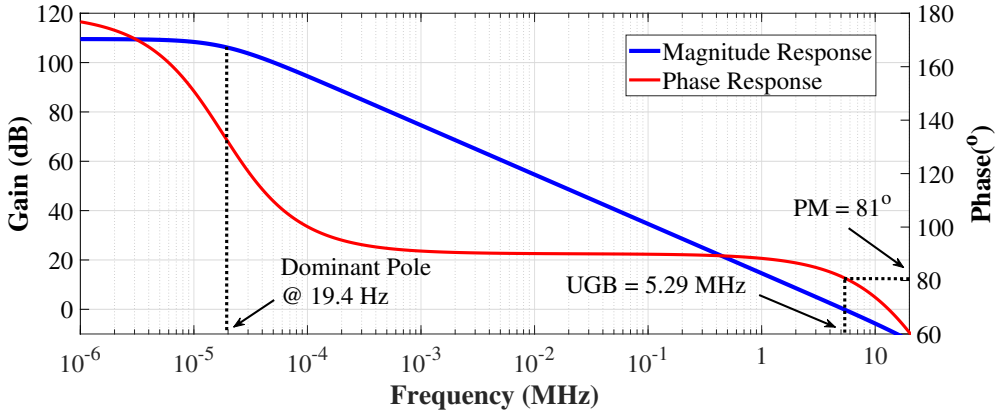

Figure 3.3: Frequency response of the proposed IGB-OTA Design-I for a typical process corner, supply voltage and temperature

The performance of the proposed IGB-OTA across different process corners is evaluated to verify the robustness of the design and the key features are summarized in Table 3.2. From Table 3.2, it can be noted that the proposed IGB-OTA maintained

Table 3.2: Post-layout performance of the IGB-OTA Design-I across process corners

Process Corner	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (μA)
tt	109.3	81	5.29	4.79
ff	108.8	84	7.56	12.85
ss	111.8	72	3.57	2.08
fnsp	101.4	78	4.87	5.48
snfp	112.3	81	5.68	5.30

a dc gain in excess of 100 dB across the process corners. It is also observed that the proposed IGB-OTA offered more than sufficient phase margin across the process

corners. At slow-slow (ss) corner, the UGB degraded by 32 % when compared to a typical (tt) corner. However, the UGB offered is more than the minimum required value of 3 MHz. A three fold increase in the quiescent current consumption is observed at fast-fast (ff) corner when compared to a typical corner. This is due to the fact that the current in the circuit is set by the bias voltages, $V_{bias,p}$ and $V_{bias,n}$, which in-turn is set by the bias generating circuit. Also note that, no adaptive biasing scheme has been used and therefore, $V_{bias,p}$ and $V_{bias,n}$ are bound to change with process, supply voltage and temperature. However, the quiescent current is quite low considering that IGB-OTA is operated at a higher supply voltage of 1.8 V.

Table 3.3: Post-Layout performance of the IGB-OTA design-I at different supply voltages

Supply (V)	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (μA)
1.71 (-5%)	111.1	77	4.15	2.92
1.755 (-2.5%)	110.3	79	4.70	3.72
1.8	109.3	81	5.29	4.79
1.845 (+2.5%)	108.1	82	5.91	6.21
1.89 (+5%)	106.8	83	6.58	8.09

Table 3.4: Post-Layout performance at different temperatures

Temp (°C)	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (μA)
0	113.4	73	5	2.98
27	109.3	81	5.29	4.79
50	97.4	84	5.27	7.82
70	84.6	85	5.22	12.25

The post-layout performance of the proposed IGB-OTA at different supply voltages, for a typical process corner at room temperature, is presented in Table 3.3. It can be observed that IGB-OTA offers DC gain in excess of 106 dB for the temperature range and a UGB in the range 4.15-6.58 MHz with adequate phase margin. However, the quiesent current vary in the range 2.92-8.09 μA.

The post-layout performance of the proposed IGB-OTA at different temperatures for a typical process corner is presented in Table 3.4. The DC gain across the temperature is in excess of 80 dB, which is sufficient for switched capacitor integrators used in delta-sigma modulators.

Since the biasing voltages, $V_{bias,p}$ and $V_{bias,n}$, are generated from the common-mode reference voltage (V_{CM}), it is important to check the performance of IGB-OTA for any variation in V_{CM}. Table 3.5 summarizes the performance of IGB-OTA against the variations in V_{CM} for a typical process corner at room temperature. The performance of the proposed IGB-OTA is found to be robust.

Table 3.5: Post-Layout performance of IGB-OTA Design-I for variations in V_{CM}

V_{CM} (mV)	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (μA)
882 (-2%)	110.3	81	5.34	4.88
891 (-1%)	109.8	81	5.32	4.81
900 (0%)	109.3	81	5.29	4.79
909 (1%)	108.7	80	5.25	4.81
918 (2%)	108.0	79	5.21	4.89

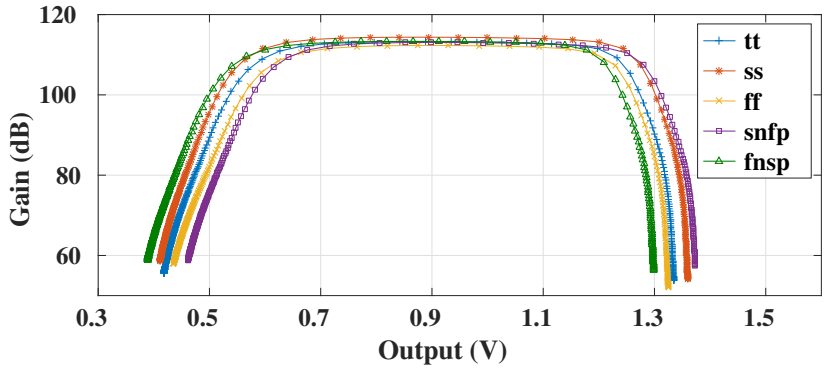

Figure 3.4: Gain vs Output voltage of IGB-OTA Design-I

Figure 3.4 shows the plot of gain versus output voltage of IGB-OTA for different process corners at room temperature. It can be observed that IGB-OTA offers a gain in excess off 100 dB across corners for an output swing of ± 350 mV around $V_{CM} = V_{DD}/2 = 0.9$ V.

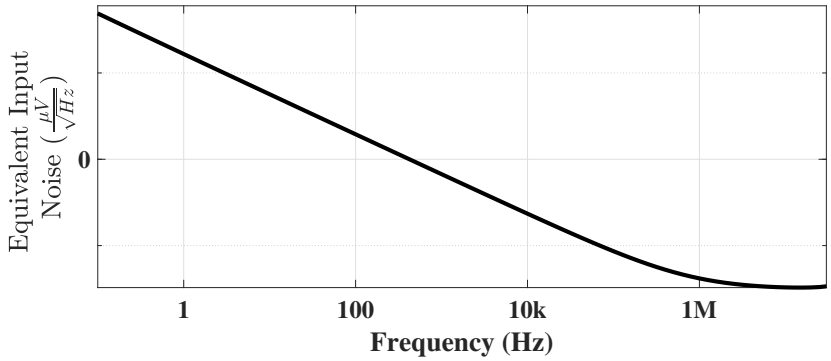

Figure 3.5: Equivalent input referred noise spectrum of IGB-OTA Design-I

Figure 3.5 shows the equivalent input noise spectrum of the proposed IGB-OTA. The total integrated noise of IGB-OTA, over the range 1 Hz to 10 MHz, is found to be 19.76 μV.

3.1.2 Monte Carlo Analysis

A Monte Carlo simulation has been carried out on the layout extracted netlist to verify the robustness of the design against process mismatch. Figures 3.6a - 3.6d show the distribution of DC gain, UGB, PM and I_Q respectively for 500 samples (N) along with their respective mean (μ) and standard deviation (σ). The plots reveal that the proposed IGB-OTA is robust even with local mismatches. The key performance metrics of the proposed IGB-OTA obtained from the post-layout simulations for a typical process corner at room temperature (27°C) are summarized in Table 3.6.

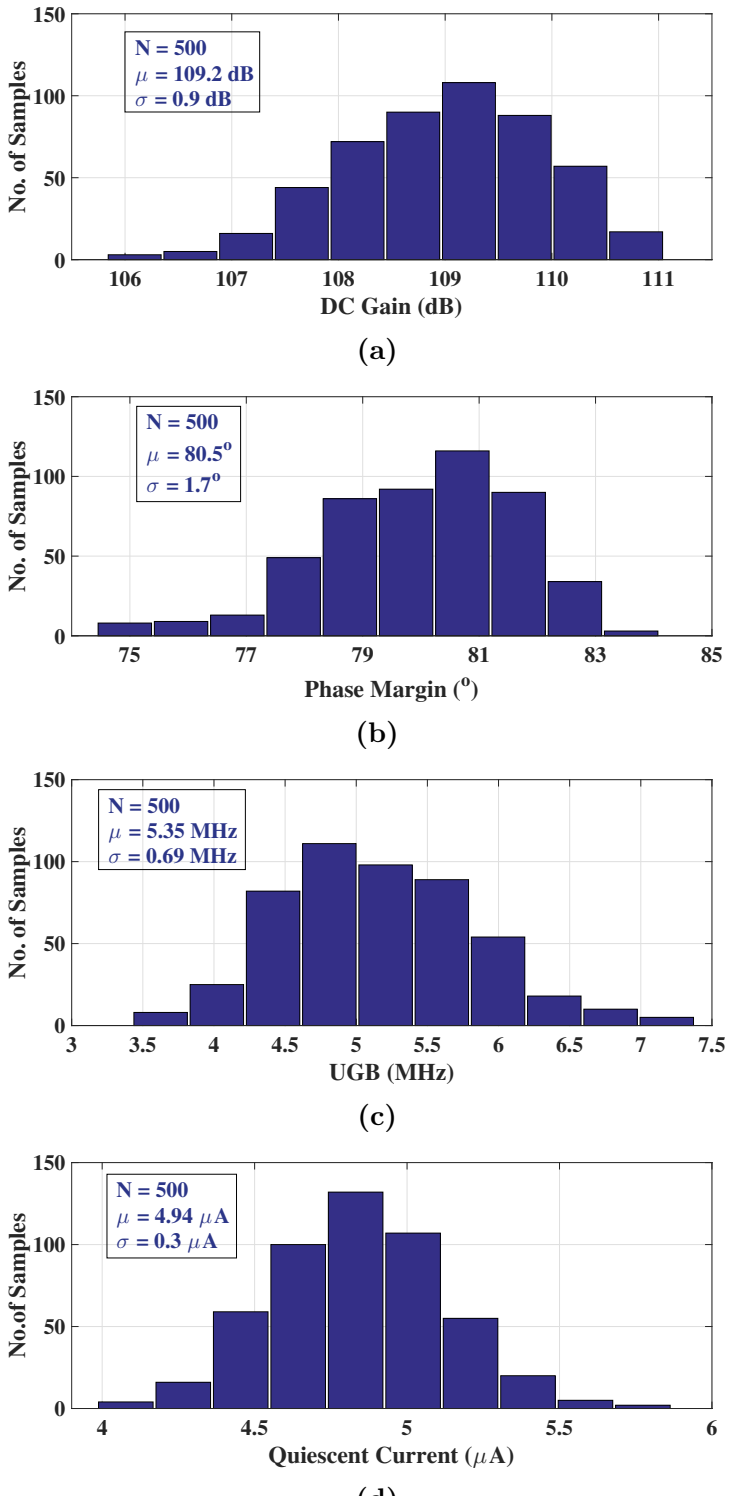

Figure 3.6: Distribution of a) DC Gain b) PM c) UGB d) Quiescent Current (I_Q) for OTA Design-I

Table 3.6: Performance summary of IGB-OTA Design-I

Parameter	**Value**
Technology (nm)	**180**
Supply (V)	**1.8**
DC Gain (dB)	**109.3**
PM (°)	**81**
GM (dB)	**30.2**
UGB (MHz)	**5.29**
Input referred noise (nV/$\sqrt{\text{Hz}}$)	**234 @ 10 kHz**
Integrated Noise (μV) (1 Hz - 10 MHz)	**19.76**
Output Swing (mV) (@ 1% THD)	$\pm$ **442**
Average Slew Rate (V/μs)	**41.3**
I_Q (μA)	**4.79**
Power (μW)	**8.62**
C_L (pF)	**2.5**

3.2 IGB-OTA DESIGN-II (FOR AUDIO APPLICATIONS)

In this section, the proposed IGB-OTA is optimized for audio applications. The maximum load capacitance targeted is 5 pF and a maximum clock frequency (f_{clk}) of 5.12 MHz is chosen (assuming an OSR of 128, i.e. 2×20 kHz×128). Therefore, following requirements on the OTA can be arrived at.

- Minimum UGB required for the OTA = 15.76 MHz, from (2.40).
- Minimum overall transconductance G_m required = 15.76 MHz×5 pF = 78.8 μS, from (2.41). The transconductance of $M1p$ and $M1n$ required is at least 39.4 μS ($G_m/2$)

Table 3.7 shows the aspect ratio of all the transistors of the OTA for this design.

Table 3.7: Aspect ratio of transistors for IGB-OTA Design-II

PMOS	$\left(\frac{W}{L}\right)$	N	NMOS	$\left(\frac{W}{L}\right)$	N
M1p	$\left(\frac{0.55}{0.18}\right)$	54	M1n	$\left(\frac{0.4}{0.24}\right)$	24
M2p	$\left(\frac{1.76}{0.18}\right)$	64	M2n	$\left(\frac{0.36}{0.24}\right)$	24
M3p	$\left(\frac{0.36}{0.25}\right)$	4	M3n	$\left(\frac{0.36}{0.25}\right)$	4
M4p	$\left(\frac{0.55}{0.18}\right)$	54	M4n	$\left(\frac{0.4}{0.24}\right)$	24
M5p	$\left(\frac{0.29}{0.18}\right)$	18	M5n	$\left(\frac{0.24}{2.7}\right)$	2
M6p	$\left(\frac{0.36}{10}\right)$	2	M6n	$\left(\frac{0.36}{10}\right)$	2

W and L are width and length in μm.

N is the number of fingers.

The UGB requirement of this OTA is higher than that of Design-I and also C_L is higher. Therefore, the inverter is required to burn higher power compared to that of Design-I. Another point to note is that, the source followers are also required to burn a higher power as their respective poles have to be place beyond UGB. As a result, the main inverter is required to have a quiescent current of 17 μA. The NMOS and PMOS source followers are required to carry a current of 4.5 μA and 15.5 μA.

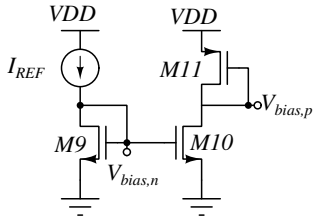

Figure 3.7: Biasing Circuit for IGB-OTA Design-II

For generating bias voltages $V_{bias,p}$ and $V_{bias,n}$, a different strategy has been used for this design. The simple scheme shown in Figure 3.7 uses an external current source reference (I_{REF}) of 250 nA. Use of current source gives a handle to tune the OTA across PVT.

Figure 3.8 shows the layout of the proposed OTA for this design. Dummy transistors are included for better matching. The total area occupied by the layout is 16.8 μm x 140.6 μm.

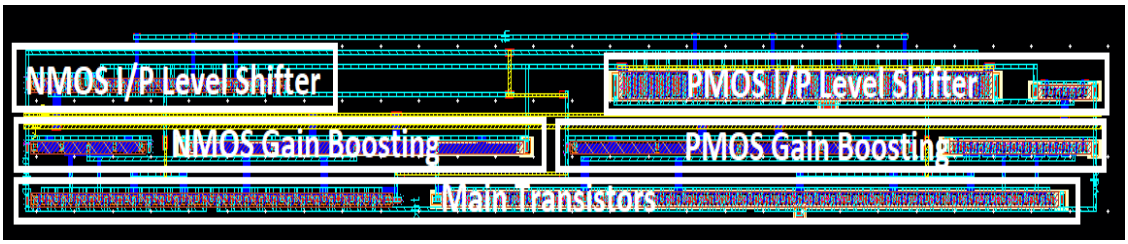

Figure 3.8: Layout of the proposed IGB-OTA for Design-II

3.2.1 Performance of IGB-OTA Design-II

The frequency response of the OTA at typical corner, room temperature and nominal supply voltage is shown in Figure 3.9. The OTA offers DC gain of 96.8 dB with an UGB of 19.4 MHz. The OTA is stable with a phase margin of 86 °.

The performance of the proposed OTA for different process corners at room temperature is presented in Table 3.8. The OTA offers DC gain in excess of 85 dB with a phase margin in excess of 79° for all process corners. However, at *ss* corner, the OTA is found to offer a poor UGB of 1.8 MHz against the desired 15 MHz. The reason for this is the following. At slow corner, the $|V_{TH}|$ of the transistor is higher than the nominal value, while the mobility μ is lower. The result is the increased requirement

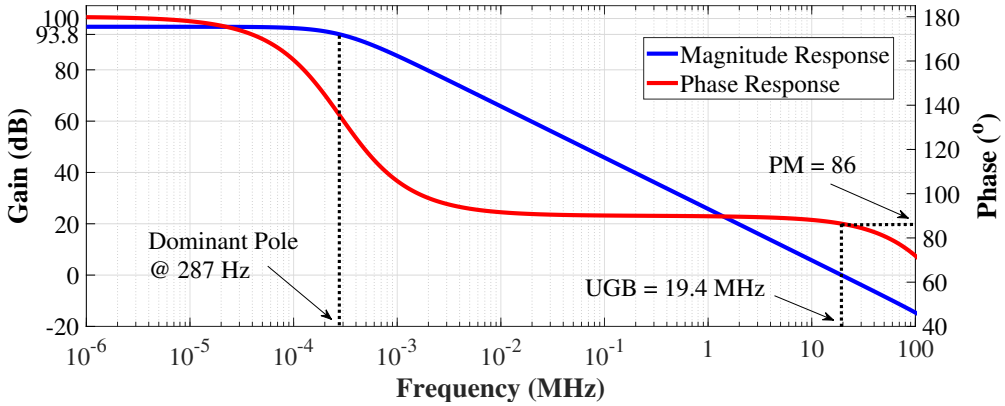

Figure 3.9: Frequency response of the proposed IGB-OTA Design-II for typical process at nominal supply and temperature.

Table 3.8: Post-Layout performance of IGB-OTA Design-II across process corners

Process Corner	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (μA)
tt	96.8	86	19.4	38.4
ff	88.2	79	77.6	132.8
ss	102.6	89	1.8	21.4
snfp	94.6	87	18.6	37.7
fnsp	98.5	86	19.6	38.4

on V_{GS} for a given current. Therefore, the source follower output makes the respective inverter input transistor to starve. At ss corner both NMOS and PMOS transistors of the inverter are starved resulting in a reduction of overall quiescent current (as can be seen from the I_Q in the Table 3.8). The reduced quiescent current of the inverter degrades the UGB. A similar but opposite action takes place in ff corner, where UGB and I_Q increases almost three folds.

Interestingly, at $snfp$ and $fnsp$ corners, there is only marginal degradation in OTA performance. The reason is the following. In these corners, one of the input transistors of the OTA is starved and the other is over biased. However, the mid voltage V_{MID} for the OTA (for the purpose of simulation) being derived from an identical OTA with input-output shorted, the NMOS and PMOS input transistors of

the inverter are biased to carry equal currents (due to averaging action). Effectively, I_Q and UGB almost remains the same as that of tt corner.

The severe degradation in UGB at ss corner is not acceptable as this introduces dynamic error in the SC-integrator, severely degrading the performance of the application in which the OTA is used. Observing that, the reduction in the inverter quiescent current is responsible for degradation in UGB, it can be concluded that if I_{REF} of the bias generating circuit is tuned appropriately, the UGB of OTA can be brought to the desired value. It can be seen that UGB and I_{REF} are inversely related. Figure 3.10 shows the frequency response of the OTA for ss corner before and after I_{REF} tuning. The OTA achieves a dc gain of 100.1 dB and a UGB of 18.1 MHz with a phase margin of 64° when $I_{REF} = \left(\frac{I_{REF,typ}}{10}\right) = 25\,nA$.

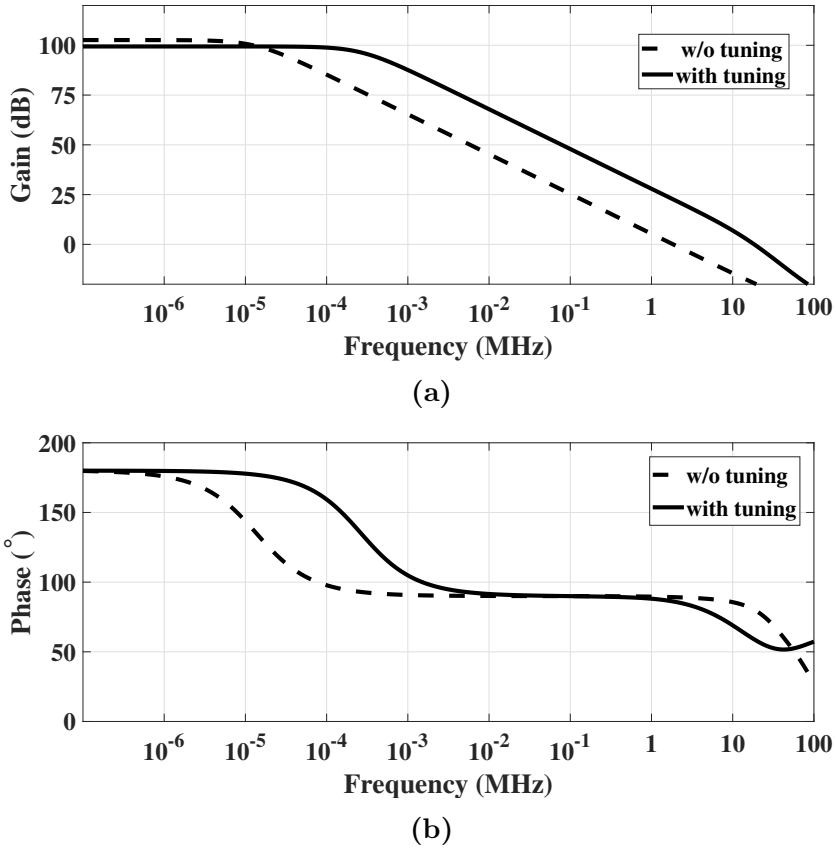

Figure 3.10: (a) Magnitude and (b) Phase response of IGB-OTA Design-II for ss corner with and without tuning I_{REF}

For ff corner, since both I_Q and UGB have increased three folds, one can think

of reducing I_Q by increasing I_{REF}. It is to be noted that, though increasing I_{REF} decreases the inverter current, at the same time it increases the source follower current. Therefore, in effect, the overall change in I_Q is small or negligible. As a result, one has to set the tuning only to this break-even point.

Performance of the IGB-OTA Design-II against supply voltage and temperature variations is presented in Table 3.9 and 3.10 respectively.

Table 3.9: Post-Layout performance of IGB-OTA Design-II for supply voltage changes

Supply (V)	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (μA)
1.71 (-5%)	97.2	88	8.9	27.8
1.755 (-2.5%)	97.0	87	13.4	32.2
1.8	96.8	86	19.4	38.4
1.845 (+2.5%)	96.4	85	27.2	47.3
1.89 (+5%)	95.9	84	36.8	59.7

Table 3.10: Post-Layout performance of IGB-OTA Design-II at different temperatures

Temp (°C)	DC gain (dB)	PM (°)	UGB (MHz)	I_Q (μA)
0	98.2	88	8.7	26
27	96.8	86	19.4	38.4
50	94.9	81	58.9	56.2
70	92	82	67.9	77.6

It can be noted that the OTA offers dc gain in excess of 90 dB along with a good phase margin against supply voltage and temperature variations. However, at supply voltages lower than the nominal, UGB degrades. It can also be seen that above nominal supply the UGB is much more than desired (also the power). Looking at the table, the UGB increases with the supply. If the reference current I_{REF} is made to have a negative coefficient of power supply, the OTA may be made to offer descent UGB over the entire supply range.

Similarly, UGB and I_Q have positive temperature coefficient. Again, by a careful design of circuit generating I_{REF} offering an appropriate negative temperature coefficient, the OTA can be made to offer desired UGB across the temperature range. However, in this thesis, generation of I_{REF} has not been considered.

Figure 3.11 shows the plot of gain versus output swing of the OTA for different process corners. It can be noted that the OTA offers a gain in excess of 80 dB for an output voltage swing of ± 440 mV which is adequate in switched capacitor applications.

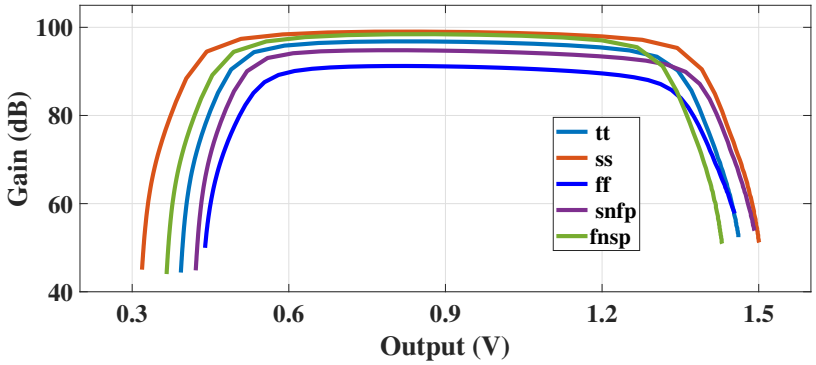

Figure 3.11: Gain vs output swing of IGB-OTA Design-II

Figure 3.12 shows the equivalent input referred noise spectrum of the proposed OTA. The total integrated input noise of the OTA, over the range 1 Hz to 6 MHz, is found to be 79.6 μV.

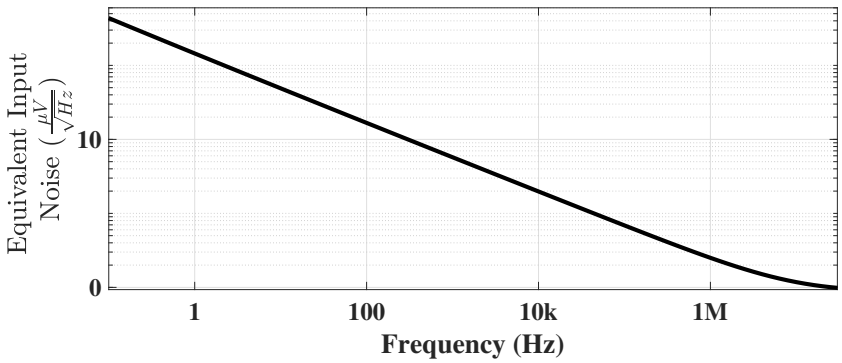

Figure 3.12: Equivalent input referred noise spectrum of IGB-OTA Design-II

3.2.2 Monte Carlo Analysis

Monte Carlo analysis for the OTA has been performed on the layout extracted netlist. The distribution of DC gain, UGB, PM and I_Q are plotted as histogram in Figures 3.13a, 3.13b, 3.13c and 3.13d respectively. Five hundred samples are taken for the simulation. The plots reveal that the proposed OTA is robust even with local mismatches.

The key performance metrics of the proposed OTA obtained from the post-layout simulations for a typical process corner at room temperature (27°C) are summarized in Table 3.11.

Table 3.11: Performance summary of IGB-OTA Design-II

Parameter	**Value**
Technology (nm)	**180**
Supply (V)	**1.8**
DC Gain (dB)	**96.8**
PM (°)	**86**
GM (dB)	**34.2**
UGB (MHz)	**19.4**
Input referred noise (nV/$\sqrt{\text{Hz}}$)	**198 @ 10 kHz**
Output Swing (mV) (@ 1% THD)	**$\pm$ 420**
Average Slew Rate (V/μs)	**45.2**
I_Q (μA)	**38.4**
Power (μW)	**69.1**
C_L (pF)	**5**

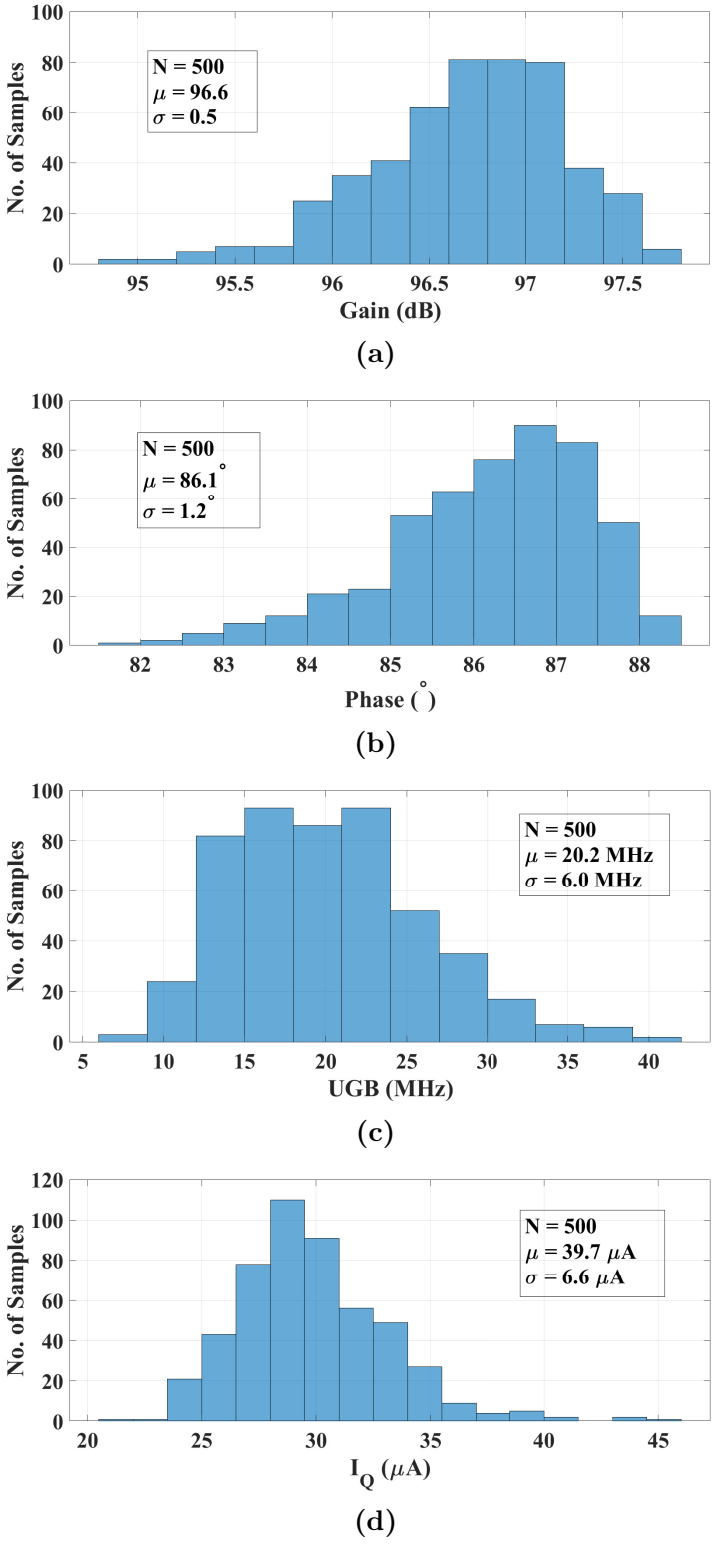

Figure 3.13: Distribution of a) DC Gain b) PM c) UGB d) Quiescent Current (I_Q) for OTA Design-II

3.3 COMPARISON WITH OTHER WORKS

Table 3.12 compares the performance of the proposed OTA with other OTAs operating on 1.8 V reported in literature. The performance of the proposed OTA is also compared with OTA's operating on lower supply voltage and it is presented in Table 3.13. A Figure of Merit (FoM) has been used for comparing the OTAs and is given

Table 3.12: Comparison of proposed OTA with OTA's operating on 1.8 V

	Perez et al. (2009)	Moallemi and Jannesari (2012)	Sutula et al. (2015)	Farsani and Ghaderi (2016)	Pourabdollah (2016)	Sarkar and Panda (2017)	**This Work Design-I**	**This Work Design-II**
Technology (nm)	180	180	180	180	180	180	**180**	**180**
DC Gain (dB)	74.0	77.0	72.0	90.7	67.0	87.7	**109.3**	**96.8**
PM (°)	-	45	50	82	69	74	**81**	**85**
UGB (MHz)	160	475	86.5	995	581	24.8	**5.3**	**19.1**
C_L (pF)	1.75	3	200	0.5	0.25	1	**2.5**	**5**
Power (μW)	362	5100	11900	12600	920	573.5	**8.6**	**69.1**
FoM (kV^{-1})	773	503	2616	71	284	78	**2792***	**2487***
Results Type	SR	SR	SR	PLSR	PLSR	SR	PLSR	

SR - Simulation Results

PLSR - Post Layout Simulation Results

* - Single Ended Design

in (3.1) (Dai et al. 2013). The higher the FoM, the more power efficient is the design.

$$\text{FoM} = \frac{\text{UGB}\,(\text{MHz}) \times \text{C}_\text{L}\,(\text{pF})}{\text{I}_\text{Q}\,(\text{mA})} \tag{3.1}$$

From the Table 3.12, it is evident that the proposed OTA offers the highest dc gain while consuming very low power resulting in a higher FoM. The OTA is found to be power efficient when compared with the other designs. It is also to be noted that, the proposed OTAs offer very good phase margin. In Table 3.13, OTAs for low supply voltages are compared where only the OTAs with power less than 200 μW are considered.

Table 3.13: Comparison of proposed OTA with OTA's operating on lower supply voltage

	Chatterjee et al. (2005)	Dai et al. (2013)	Zuo and Islam (2013)	Abdelfattah et al. (2015)		Kulej (2015)	Cabrera-Bernal et al. (2016)	**This Work Design-I**	**This Work Design-II**
Technology (nm)	180	130	350	65		50	180	**180**	**180**
Supply (V)	0.5	1	$\pm$0.5	0.5	0.35	0.4	0.7	**1.8**	**1.8**
DC Gain (dB)	62	60	88.3	46	43	60	57.5	**109.3**	**96.8**
PM (°)	45	72	66	57	56	70	60	**81**	**85**
UGB (MHz)	10	3.7	11.7	38	3.6	2.5	3	**5.3**	**19.1**
C_L (pF)	20	95	15	3		10	20	**2.5**	**5**
Power (μW)	75	187	197	182	17	24	25.4	**8.62**	**69.1**
FoM (kV^{-1})	1333	1880	891	313	222	422	1653	**2792***	**2487***
Result type	MR	MR	MR	MR	MR		SR	PLSR	

MR - Measured Results

SR - Simulation Results

PLSR - Post Layout Simulation Results

* - Single-ended Design

With the encouraging results of the proposed OTA in terms of its gain, power and robustness, a DTDSM has been designed to prove the suitability of the OTA in audio applications. The next chapter presents the design of DTDSM using the proposed OTA and its simulation results.

Chapter 4

A DISCRETE-TIME DELTA SIGMA MODULATOR FOR AUDIO APPLICATIONS

It is imperative to validate the proposed IGB-OTA architecture for its use in a high performance application. DTDSM is a good application for validating the OTA as SC-integrators are the main functional block of its loop-filter. A DTDSM for audio applications has been designed. This chapter has been dedicated for this purpose. The initial sections give a brief insight into DTDSM architecture and fundamentals. The chapter then explains the design of DTDSM for the audio band using the proposed IGB-OTA and presents its simulation results.

4.1 FUNDAMENTALS OF DELTA SIGMA MODULATORS

A DSM employs oversampling and noise shaping techniques to deliver higher accuracy. A generic architecture of a DSM is presented in Figure 4.1. It is assumed that the input signal is filtered by using an anti-aliasing filter which attenuates the out-of-band frequencies. A sample and hold circuit performs the oversampling operation on the input signal. A loop filter, a quantizer and a DAC in a feedback loop performs

the noise shaping operation. The quantizer introduces quantization noise into the modulator.

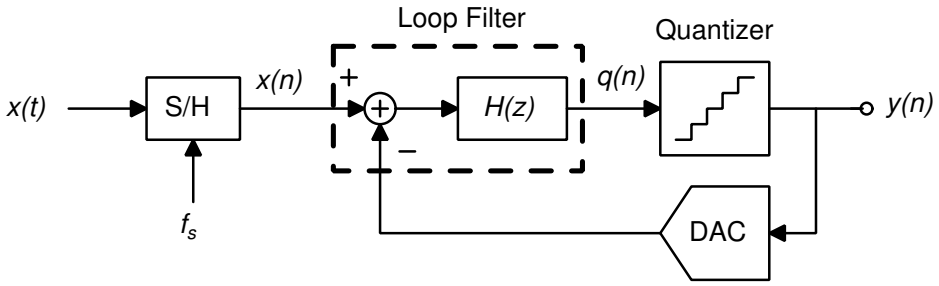

Figure 4.1: Generic architecture of a DSM (José and Del Río 2013)

4.1.1 Quantization Noise

Using a linear additive white noise model for the quantizer, the modulator in Figure 4.1 can be modeled as a two-input (x and e) and one-output (y) linear system as shown in Figure 4.2. $q(n)$ is the input to the quantizer and $e(n)$ is the quantization error introduced by the quantizer. The gain of quantizer is assumed to be unity.

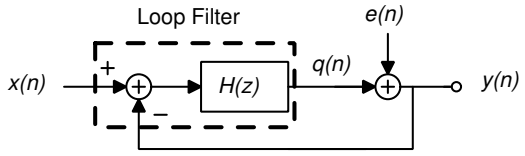

Figure 4.2: Ideal linear model of a DSM (José and Del Río 2013)

Let's assume that the input to an N-bit quantizer, $q(n)$, randomly changes within the range [-Δ/2,+Δ/2] without overloading the quantizer. Δ is a small fraction of the modulator's reference voltage (V_{REF}) which can be expressed as follows.

$$\Delta = \frac{V_{REF}}{2^N} \tag{4.1}$$

Then the quantization noise, $e(n)$, introduced by quantizer can be treated as a random variable with a uniform probability distribution in the range [-Δ/2,+Δ/2] and its probability density function (PDF) and power spectral density (PSD) $S_e(f)$ are illustrated in Figure 4.3a and 4.3b respectively.

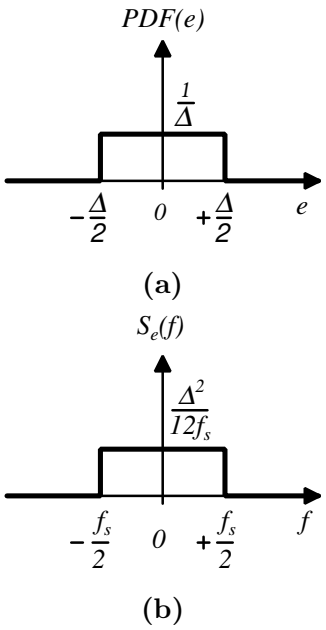

Figure 4.3: (a)PDF and (b) PSD of Quantization noise (José and Del Río 2013)

4.1.2 Oversampling

According to the Nyquist theorem, minimum sampling frequency, with which a signal having a bandwidth f_b can be sampled, is 2 f_b and it is called Nyquist frequency (f_N). The oversampling ratio (OSR) is given by (4.2) and it quantifies, by how much factor, is the sampling frequency greater than the nyquist frequency.

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2f_b} \tag{4.2}$$

To understand the usefulness of oversampling, consider a continuous time signal $x(t)$ having a signal bandwidth, f_b, whose fourier transform is as shown in Figure 4.4a. In general, sampling a signal at frequency f_s produces copies of the signal (called aliases) in the frequency spectrum which are centered around every integer multiple of f_s. Let us consider that the signal $x(t)$ is sampled at nyquist frequency, then the fourier transform would be as shown in Figure 4.4b. In this case, signal bandwidth is equal to half the sampling frequency and therefore the aliases are closely spaced as shown in Figure 4.4b. Now, consider that the signal $x(t)$ is oversampled, i.e., sampled

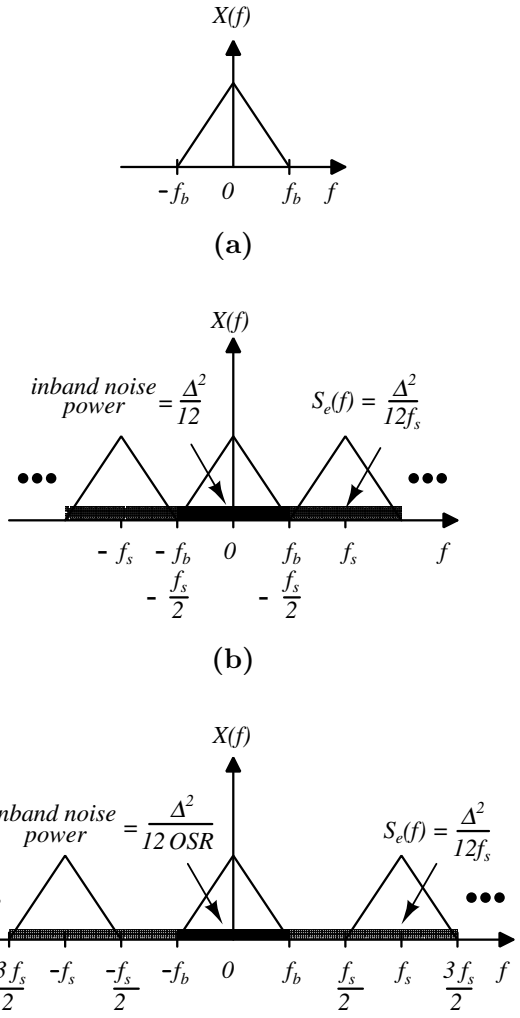

Figure 4.4: Fourier Transform of (a) input signal $x(t)$ (b) $x(t)$ when sampled at nyquist frequency (c) $x(t)$ when sampled at a frequency higher than nyquist frequency (José and Del Río 2013)

at a frequency higher than nyquist frequency, then the fourier transform would be as shown in Figure 4.4c. In this case, signal bandwidth is lower than half the sampling frequency and therefore the aliases are spaced far apart from each other as shown in Figure 4.4b. Therefore, this relaxes the design specifications of anti-aliasing filter and the reconstruction filter since the filter response does not require steep roll-off at band edges. Further, oversampling reduces the inband quantization noise power by a factor of $1/OSR$ as the signal bandwidth is lower than $f_s/2$.

4.1.3 Noise shaping technique

Noise shaping technique pushes the inband quantization noise out of the signal band i.e., it filters out the inband quantization noise such that most of its power lies outside the signal band. A mathematical analysis is provided to gain more insight into the process of noise shaping.

The linear model of the modulator can be described in the z-domain as follows (Schreier et al. 2005).

$$Y(z) = STF(z).X(z) + NTF(z).E(z) \tag{4.3}$$

where $STF(z)$ and $NTF(z)$ stand for the signal and noise transfer functions, respectively and are given by

$$STF(z) = \frac{H(z)}{1 + H(z)}, \quad NTF(z) = \frac{1}{1 + H(z)} \tag{4.4}$$

Note that, if the loop filter is designed such that $|H(f)| >> 1$ within the signal band, then $|STF(f)| \approx 1$ and $|NTF(f)| << 1$; that is, the quantization noise is highly attenuated while the input signal is passed to the output.

The simplest loop filter $H(z)$ that exhibits the desired frequency response is an integrator. So, lets consider a 1st order discrete-time forward-Euler integrator as the loop filter to understand the noise shaping. The transfer function of the integrator in z-domain is described as follows (Johns and Martin 2008).

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{4.5}$$

So, the output of the modulator described in (4.3) leads to

$$Y(z) = z^{-1}.X(z) + (1 - z^{-1}).E(z) = STF(z).X(z) + NTF(z).E(z) \tag{4.6}$$

From the above expression, it can noted that input is replicated at the output with one clock cycle delay. The NTF represents a high pass filter and therefore the quantization noise is high pass filtered, thereby shaping the quantization noise out of signal band as shown in Figure 4.5 The in-band quantization noise power for a DSM

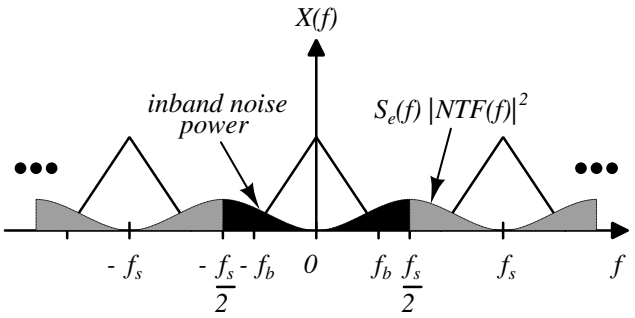

Figure 4.5: Quantization Noise shaping in a DSM (José and Del Río 2013)

can be computed as follows (José and Del Río 2013)

$$\overline{V_e^2} = \int_0^{f_b} S_e(f)|NTF(f)|^2 \tag{4.7}$$

Signal-to-Quantization Noise Ratio ($SQNR$) is a performance metric which quantifies how well the quantization noise is shaped out of the signal band. Assuming that the input is a sinusoidal signal with a peak amplitude A, then the input signal power is given by

$$\overline{V_{sig}^2} = \frac{A^2}{2} \tag{4.8}$$

For a first order DSM, the inband quantization noise power is given as follows (Johns and Martin 2008)

$$\overline{V_e^2} = \frac{\Delta^2}{12}\,\frac{\pi^2}{3(OSR)^3} \tag{4.9}$$

using (4.1) in (4.9) yields

$$\overline{V_e^2} = \frac{V_{REF}^2\,\pi^2}{36\,(OSR)^3\,2^{2N}} \tag{4.10}$$

Therefore, the $SQNR$ can be computed as follows

$$SQNR = \frac{\overline{V_{sig}^2}}{\overline{V_e^2}} \tag{4.11}$$

$$= \frac{A^2}{V_{REF}^2}\,\frac{18\,(OSR)^3\,2^{2N}}{\pi^2} \tag{4.12}$$

$$= P_{in,norm}\,\frac{18\,(OSR)^3\,2^{2N}}{4\,\pi^2} \tag{4.13}$$

which can be expressed in dB as

$$SQNR_{dB} = -3.41 \; + \; 6.02\,N + \; 10log(P_{in,norm}) \; + \; 30log(OSR) \tag{4.14}$$

From (4.14), it is noted that SQNR of a first order DSM is a function of quantizer resolution, OSR and also the input signal amplitude. SQNR of a first order DSM with a 1-bit quantizer (for an input sinusoidal signal amplitude $A = V_{REF}/2$) can be expressed as

$$SQNR_{dB} = 2.61 \; + \; 30log(OSR) \tag{4.15}$$

Figure 4.6 shows the plot of $SQNR$ versus OSR for a 1-bit quantizer. The $SQNR$

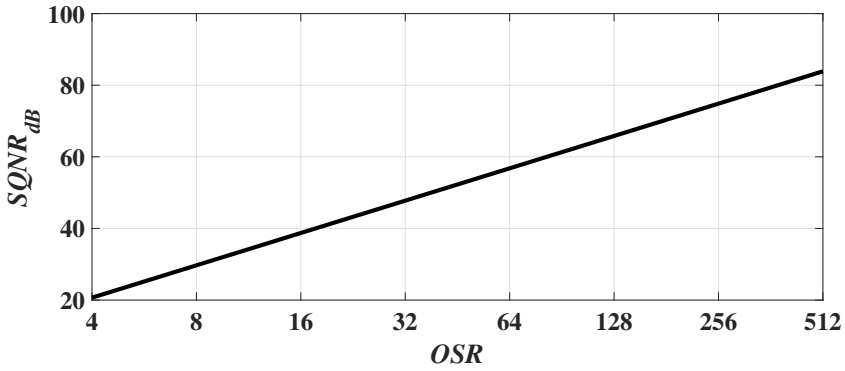

Figure 4.6: $SQNR$ of a first order DSM as a function of OSR

increases by 9 dB for each doubling of OSR. This results in a relatively low $SQNR$, around 74 dB, even for an OSR as high as 256. However, implementing a modulator using a higher OSR requires an OTA with a higher UGB and that comes at the cost of excess power consumption. Using a higher OSR will also increases the dynamic power consumption of the modulator. A higher order DSM can achieve a given SQNR with a lower OSR.

For a L^{th} order DSM, the inband quantization noise power can expressed as follows

$$\overline{V_e^2} = \frac{\Delta^2}{12} \; \frac{\pi^{2L}}{(2L+1)(OSR)^{2L+1}} \tag{4.16}$$

Therefore (4.11) yields

$$SQNR = P_{in,norm}\ \frac{6(2L+1)\,(OSR)^{2L+1}\,2^{2N}}{4\,\pi^{2L}} \tag{4.17}$$

Figure 4.7 shows the plot of $SQNR$ as a function of OSR for a 1-bit DSM of order L (with $A = V_{REF}/2$) and it can be observed that a higher order modulator achieves a given $SQNR$ for a lower OSR when compared to a lower order modulator. However, the disadvantage of using a higher order DSM is the instability of the modulator. The first order and second order modulators are more stable and as the order increases ensuring stability becomes harder.

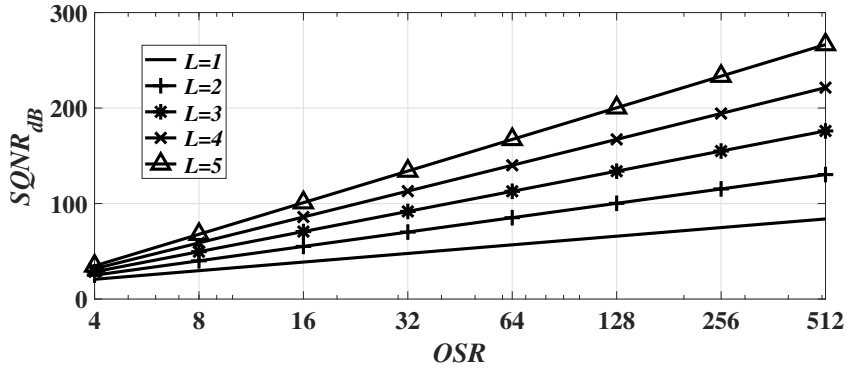

Figure 4.7: $SQNR$ of a L^{th} order DSM with a 1-bit quantizer

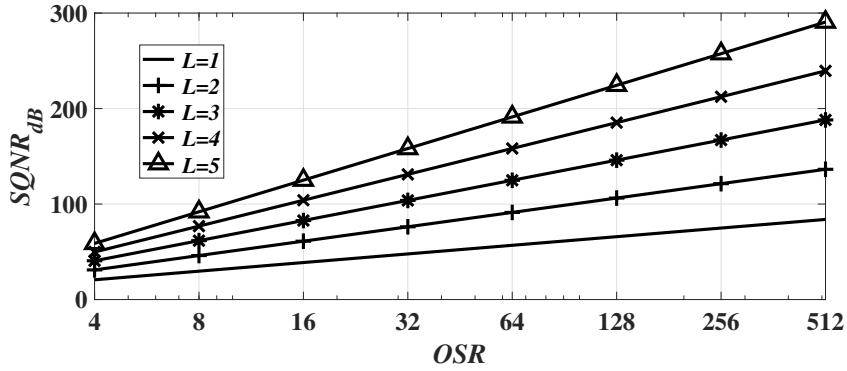

Figure 4.8: $SQNR$ of a L^{th} order DSM with a 2-bit quantizer

An alternate solution to achieve a higher $SQNR$ is to use multi-bit quantizer instead of a 1-bit quantizer. Figure 4.8 shows the plot of $SQNR$ as a function of OSR

for a 2-bit DSM of order N and it can be noted that 2 bit quantizer achieves a given $SQNR$ with a lower OSR. However, this comes at the cost of increased complexity of quantizer design and excess power consumption.

Table 4.1: Comparison of Discrete-time vs Continuous-time DSMs (Cherry and Snelgrove 1999, Schreier et al. 2005, José and Del Río 2013)

Discrete-time DSM	**Continuous-time DSM**
Coefficients are implemented using only capacitors and realized by capacitor ratio's. So, robust over process & temperature variations.	Coefficients are implemented using resistors and capacitors. RC time constant is sensitive to process & temperature variations.
Insensitive to clock jitter	Very sensitive to clock jitter
Common mode feedback circuits (CMFB) can be implemented with passive elements and thereby contributing to a low power design	CMFB require active elements and consumes additional power
Not suitable for low voltage applications due to the issue with turning the switches on and off	Suitable for low voltage applications
Not suitable for high frequency applications since it requires wideband OTA's (may not be feasible) resulting in higher power consumption	Highly preferred for high frequency applications
Modulator design is relatively simple	The design is relatively challenging. Several non-idealities have to be addressed such as clock jitter, excess loop delay, RC time constant variations

4.1.4 Domain of Implementation

DSM can be implemented in discrete-time as well as in continuous-time domain. Table 4.1 summarizes the usefulness and limitations of discrete-time and continuous-time implementations. So, clearly the choice of domain is purely based on the application in which the modulator is intended to used.

Since this research work intends to design a DSM using an inverter-based OTA, a discrete-time domain implementation is chosen.

4.1.5 Filter Topologies

The discrete-time implementations of higher order loop filter can be broadly classified into two categories. They are

- Distributed feedback topology
- Distributed feed-forward topology

Distributed feedback topology:

Distributed feedback topology for implementing higher order loop filter is shown in Figure 4.9. The STF and NTF of an L^{th} order modulator for this topology can be given by

$$STF(z) = \frac{H^L(z)\prod_{i=1}^{L} a_i}{1+\Sigma_{i=1}^{L} b_i H^{L+1-i}(z)\prod_{k=i}^{L} a_k} \tag{4.18}$$

$$NTF(z) = \frac{1}{1+\Sigma_{i=1}^{L} b_i H^{L+1-i}(z)\prod_{k=i}^{L} a_k} \tag{4.19}$$

This implementation topology has multiple feedback paths and therefore ensuring

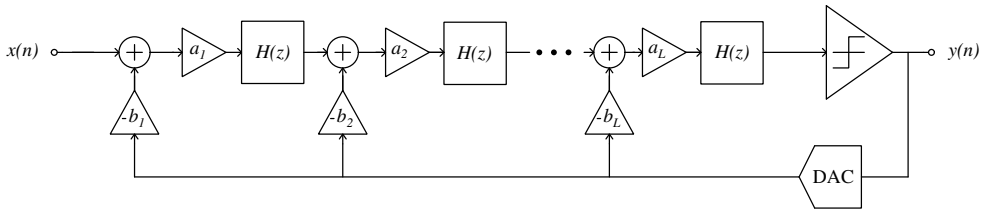

Figure 4.9: Distributed feedback topology for higher order DSM (Schreier et al. 2005)

stability is a challenge. The major disadvantage of this topology is that the first

integrator has to process input signal and therefore requires higher output swing capability. In this topology, there is no freedom to choose STF without altering the NTF. This limitation can be overcome by coupling the input at the outputs of each integrator as shown in Figure 4.10.

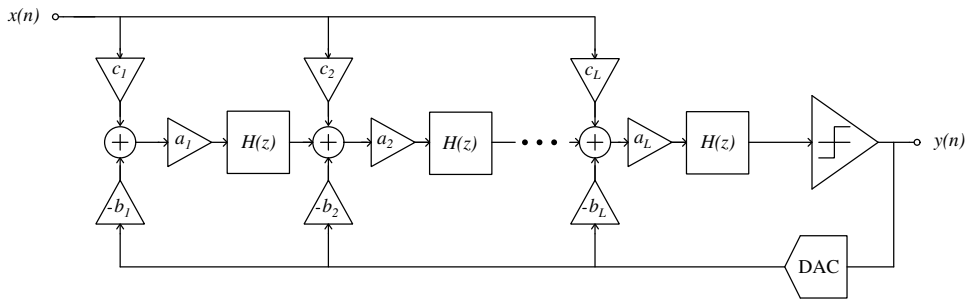

Figure 4.10: Distributed feedback topology for higher order DSM with input coupling (Schreier et al. 2005)

Distributed feed-forward topology:

Higher order filter implementation using distributed feed-forward topology is illustrated in Figure 4.11.

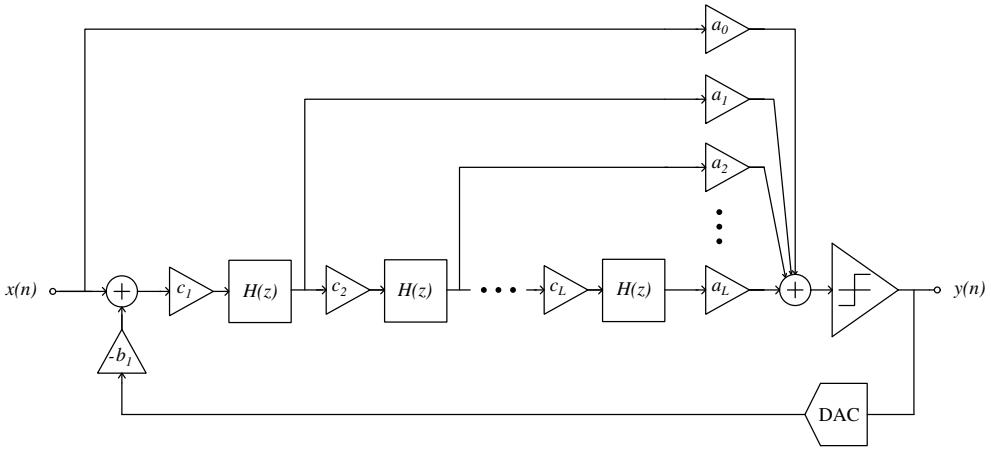

Figure 4.11: Distributed feed-forward topology for higher order DSM (Schreier et al. 2005)

In this topology there is only one feedback path. The STF and NTF of an L^{th}

order modulator for this topology is given by

$$STF(z) = \frac{a_0 + b_1 \sum_{i=1}^{L} a_i H^i(z) \prod_{k=1}^{i} c_k}{1 + b_1 \sum_{i=1}^{L} a_i H^i(z) \prod_{k=1}^{i} c_k} \tag{4.20}$$

$$NTF(z) = \frac{1}{1 + b_1 \sum_{i=1}^{L} a_i H^i(z) \prod_{k=1}^{i} c_k} \tag{4.21}$$

If the feed-forward coefficient a_0 is chosen to be 1, then STF becomes 1. Under such circumstance, this topology offers the best linearity. The main advantage of this is that the integrators process only the quantization noise thereby relaxing the output swing requirements of the integrator. Also, the NTF can be modified without altering the STF (which is equal to 1).

Since this research work targets audio applications which require high linearity, feed-forward topology having $STF = 1$ is chosen.

4.1.6 Performance metrics

The most commonly used performance evaluation metrics of a DSM are listed below (José and Del Río 2013, Pavan et al. 2017).

- **Signal-to-Quantization Noise Ratio (SQNR):**

  It is defined as the ratio of the power of fundamental component to the total uncorrelated in-band noise power (excluding the harmonic components).

- **Signal-to-Noise & Distortion Ratio (SNDR):**

  It is defined as the ratio of the power of fundamental component to the total in-band noise power which also includes all the possible in-band harmonics.

- **Spurious Free Dynamic Range (SFDR):**

  It is defined as the ratio of the power of the fundamental component to the power of the largest spurious component inside the signal bandwidth

- **Dynamic Range (DR):**

  It is defined as a ratio of power of maximum input signal amplitude to the power of input signal at which SNR is 0 dB.

- **Effective number of bits (ENOB):**

  ENOB can be computed from SNDR as follows

$$\text{ENOB} = \frac{\text{SNDR(dB)} - 1.76}{6.02} \tag{4.22}$$

  It basically conveys the maximum bit resolution that a DSM can deliver.

- **Overload Level (OL):**

  It is defined as the maximum input amplitude for which the DSM works correctly without the internal nodes getting saturated. It is typically chosen as the input amplitude for which SNR drops by 6 dB below the peak SNR

4.2 DESIGN OF DSM USING THE PROPOSED IGB-OTA

Typically, for audio applications the performance metrics SNR, SNDR, SFDR and DR are all expected to be more than 80 dB (Chae and Han 2009, Kuo et al. 2010, Zhang et al. 2011, Yang et al. 2012). A 1-bit third order DSM with an OSR of 128 is guaranteed to meet these specifications. A feed-forward topology is chosen for implementing the loop filter of the DTDSM for the following reasons.

- Audio applications demand high linearity and feed-forward topology offers the highest linearity.
- In a feed-forward topology, only the error is processed by the integrators and therefore the output swing requirement on OTA is less stringent.

The block diagram of third order fully feed-forward $\Delta\Sigma$ modulator is shown in Figure 4.12. The modulator is divided into five sub-blocks Int 1, Int 2, Int 3, Adder and the comparator. b_i and c_i are the integrator gains (filter coefficients) and a_i's are the weighting factors of the adder block.

Once the order, OSR, loop filter topology are chosen, then the next step is to choose loop filter coefficients that would help in achieving the desired DSM specifications. One important constraint on the loop filter coefficients is that, for a given set

of coefficients, the integrator output node should not swing beyond the permissible limit.

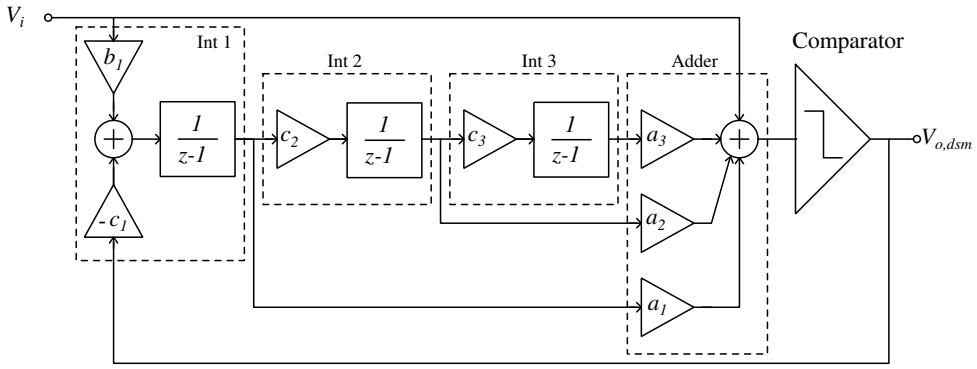

Figure 4.12: Block diagram of 3^{rd} order feed-forward $\Delta\Sigma$ modulator

The proposed IGB-OTA Design-II, to be used in the integrator, has a limited output swing and it offers gain in excess of 80 dB for an output swing of ± 440 mV. Therefore, the voltage swing at all the integrator output nodes has to be limited to within ± 400 mV (with a margin of ± 40 mV). Therefore the chosen loop filter should ensure a stable operation as well as limit the voltage swing at all the internal nodes to within ± 400 mV. The solution for loop filter coefficients which satisfy the above constraints, is not unique. The loop filter should be practically feasible to implement using the chosen filter coefficients.

Accordingly, the loop filter coefficients are found using MATLAB's **Delta-Sigma** toolbox (open source) (Schreier 2020), ensuring loop stability and limiting the signal swing at each integrating node to within 400 mV. A Simulink model of DTDSM has been used to finalize the filter coefficients (Refer Appendix-I) and the loop filter coefficients, so found, are given in Table 4.2.

Table 4.2: Loop filter coefficients of DSM

Coefficient	a_1	a_2	a_3	b_1	c_1	c_2	c_3
Value	1	1	2	0.2	0.2	0.4	0.1

The resulting STF and NTF of the DSM are given in (4.23) and (4.24)

$$STF = 1 \tag{4.23}$$

$$NTF = \frac{(z-1)^3}{z^3 - 2.8z^2 + 2.68z - 0.872} \tag{4.24}$$

4.3 MODULATOR IMPLEMENTATION

The blocks of the modulator shown in Figure 4.12 are operated as follows. $Int\,1$ and $Int\,3$ operate in sampling mode during ϕ_1 phase and in integration mode during ϕ_1 phase. For $Int\,2$, ϕ_2 is the sampling phase and ϕ_1 is the integration phase. Adder block makes the sum of its input signal with weights available during ϕ_1 phase. And finally, the comparator makes a decision during ϕ_1 phase.

4.3.1 First integrator block ($Int\,1$)

The first integrator integrates the input V_i and the output of the modulator (i.e., output of comparator), $V_{o,dsm}$, with gains b_1 and $-c1$ respectively. Figure 4.13 shows the schematic of $Int\,1$. The circuit has been derived from Figure 2.8a. Only one half of the circuit has been shown for the simplicity. Since the gains (coefficients) b_1 and c_1 required are same (0.2), a single capacitor C_{s1} has been used for sampling. The ratio of C_{s1} to C_{i1} is chosen to be 0.2.

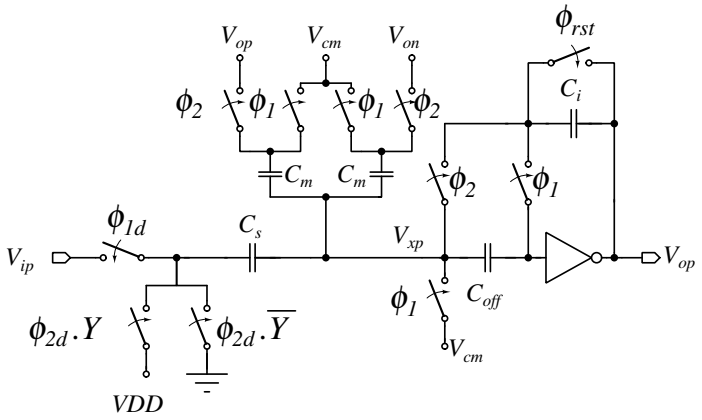

Figure 4.13: Schematic circuit of single-ended first integrator ($Int\,1$)

4.3.2 Second and third integrator blocks ($Int\,2$ and $Int\,3$)

The integrators $Int\,2$ and $Int\,3$ are the same as given in Figure 2.8a with an additional CMFB circuit. C_s and C_i are chosen to have their ratio as 0.4 and 0.1 respectively for $Int\,2$ and $Int\,3$.

4.3.3 Adder block

Adder block adds its input signal with weights utilizing the ϕ_2 phase of the previous cycle and ϕ_1 phase of the current cycle. The result of the addition is available for comparison during ϕ_1 phase of the current cycle. This block has been realized using the schematic shown in Figure 4.14.

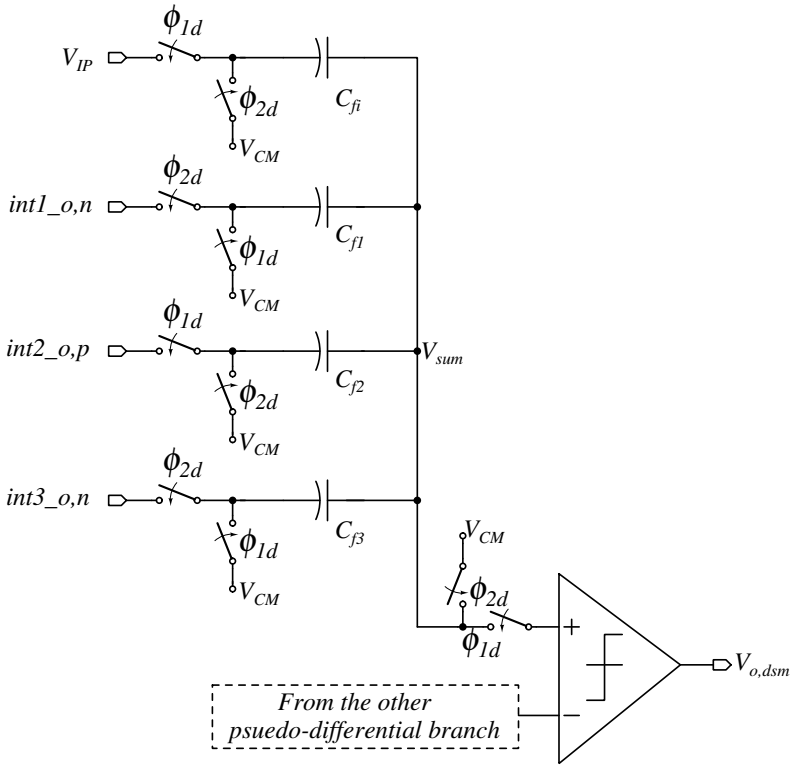

Figure 4.14: Schematic circuit of single-ended adder stage

During ϕ_2 place, capacitors C_{f1} and C_{f3} sample the negative of the outputs of integrators 1 and 3 respectively and the capacitors C_{fi} and C_{f2} are discharged as both the plates are connected to V_{CM}.

During ϕ_1 phase, bottom plates of C_{f1} and C_{f3} are connected to common-mode, C_{fi} is connected to V_{ip} and C_{f2} to the positive output of the integrator 2. Since, the common top plates of the capacitors are floating being connected to comparator input, the charges on the capacitors re-distribute themselves (due to conservation of charge). The resulting voltage at the input of the comparator will be as given in (4.25).

$$V_{sum} = \left(\frac{C_{fi}}{C_{tot}}\right) V_{ip} - \left(\frac{C_{f1}}{C_{tot}}\right) V_{on,int1} + \left(\frac{C_{f2}}{C_{tot}}\right) V_{op,int2} - \left(\frac{C_{f3}}{C_{tot}}\right) V_{on,int3} \tag{4.25}$$

Where, $C_{tot} = C_{fi} + C_{f1} + C_{f2} + C_{f3}$. For a differential architecture, one can rewrite (4.25) as (4.26) resulting in the desired addition operation.

$$V_{sum} = \left(\frac{C_{fi}}{C_{tot}}\right) V_{ip} + \left(\frac{C_{f1}}{C_{tot}}\right) V_{op,int1} + \left(\frac{C_{f2}}{C_{tot}}\right) V_{op,int2} + \left(\frac{C_{f3}}{C_{tot}}\right) V_{op,int3} \tag{4.26}$$

From (4.26), it can be clearly noted that the output of the adder block is the sum of inputs weighted by the respective capacitors but attenuated by the sum of the capacitances. As long as the ratio of capacitors match the ratio of feed-forward coefficients, attenuation is not an issue for a 1-bit comparator. The complete schematic circuit of 1-bit third order DSM is shown in Figure 4.16 and the implementation details of all the circuit elements in the DSM are presented in the following subsections.

4.3.4 Non-overlap clock generation

The SC integrator uses four different clock phases for its operation, as explained in chapter 2. The gate-level schematic of the circuit for generating the four clock phases is shown in Figure 4.15 (Pavan et al. 2017). The delay and non-overlap time required for the clock phases is adjusted by adjusting aspect ratio of transistors of '*' marked inverters.

4.3.5 Switch Implementations

All the switches in the SC integrator, except the input sampling switch, are implemented using transmission gate with two dummy transmission gates as shown in Figure 4.17 (Pavan et al. 2017). The dummies are used to minimize the effect of

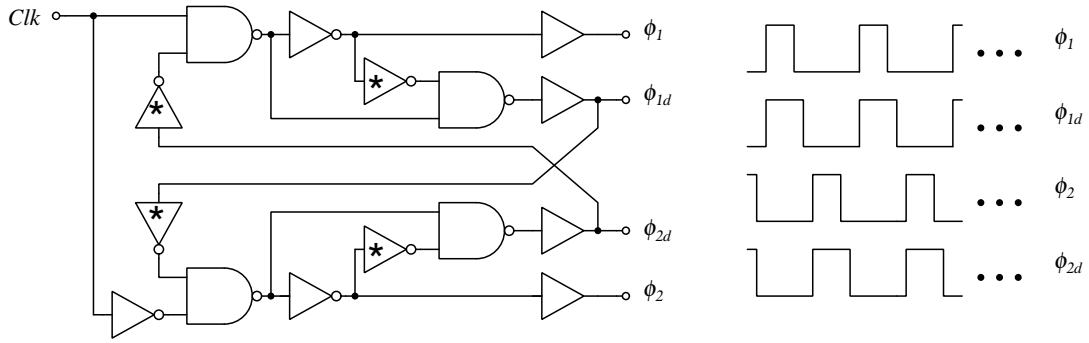

Figure 4.15: Clock generation circuit (Pavan et al. 2017)

charge injection. The transistors in the dummies are sized to be half of the main transistor. The operation of this switch is as follows. When 'CLK' signal is high, the transmission gate is 'ON' and the dummies are 'OFF' and when 'CLK' goes low, the transmission gate turns 'OFF' and the channel charge is taken by the dummies while turning 'ON'. The complementary clock signals are generated from the main clock input (ϕ_{xx}) as shown in Figure 4.18

The input switch of each SC integrator that samples integrators input on to the sampling capacitor is implemented using a boot-strapped switch arrangement (Razavi 2015). This is because, any input dependent charge injection in the integrator degrades the linearity of the DSM. The schematic of the switch is shown in Figure 4.19.

The operation of the boot-strapped switch is as follows.

- When 'CLK' signal is low, $M3$ and $M8$ transistors turn 'ON' and M6 transistor turns 'OFF'. As a result, the switch $M1$, responsible for sampling, will be in 'OFF' state. The capacitor C_2 is charged to VDD through M3 and M5 transistors.

- When 'CLK' signal becomes high, M3 and M8 transistors turn 'OFF' and M6 transistor turns 'ON'. As a result, the gate voltage of M1 transistor will be $V_{in} + VDD$ and this turns 'ON' the switch. Since the gate-to-source voltage of M1 transistor is 'VDD' and is independent of V_{in}, the charge on the sampling capacitor will be free of input dependent charge injection.

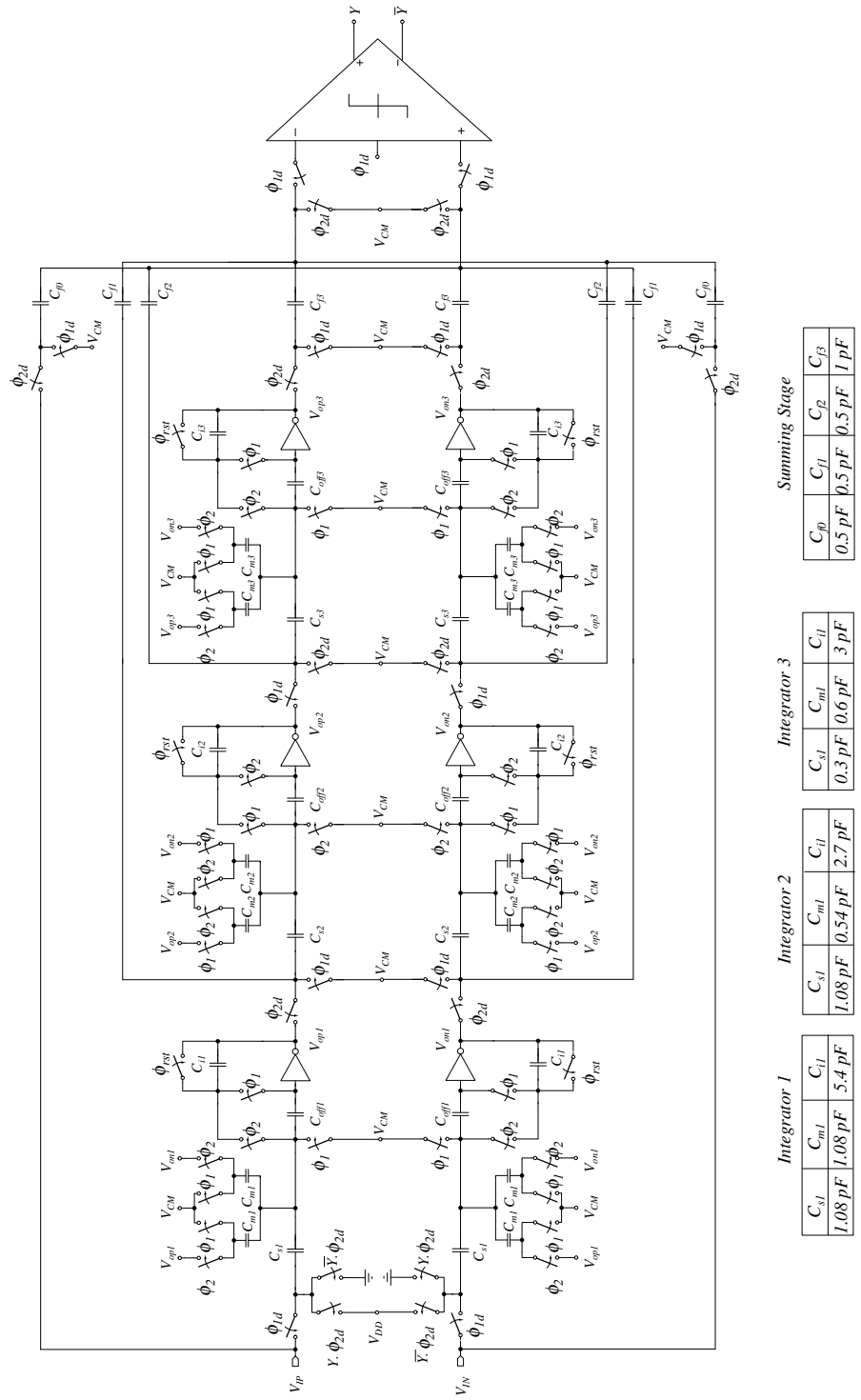

Figure 4.16: Complete schematic circuit of pseudo differential DSM

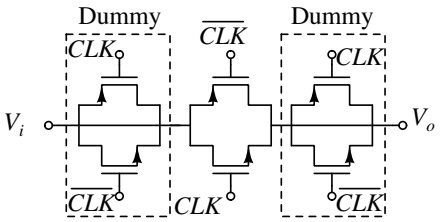

Figure 4.17: Switch with two dummies (Pavan et al. 2017)

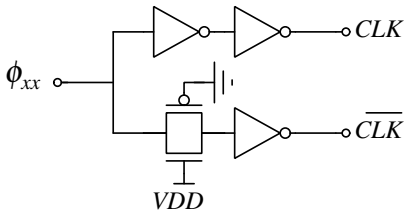

Figure 4.18: Complementary clock generation (Pavan et al. 2017)

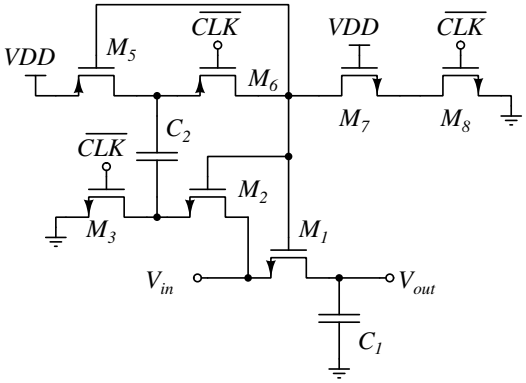

Figure 4.19: Boot-strapped Switch (Razavi 2015)

4.3.6 Capacitor Ratio implementation

The mismatch between capacitors will alter the filter coefficients and therefore a good layout strategy has to be adopted. Capacitances are implemented as integer multiples of unit capacitance and the unit capacitance is implemented in a square shape for best matching (Razavi 2005). Common centroid and inter-digitization techniques are employed for achieving a good match. Figure 4.20, 4.21, 4.22 and 4.23 show the layout scheme used for implementing the capacitors of 1^{st} integrator, 2^{nd} integrator, 3^{rd} integrator and the feed-forward summing stage respectively. C_s, C_i and C_{off} are the sampling, integrating and offset capacitors in a SC integrator circuit respectively.

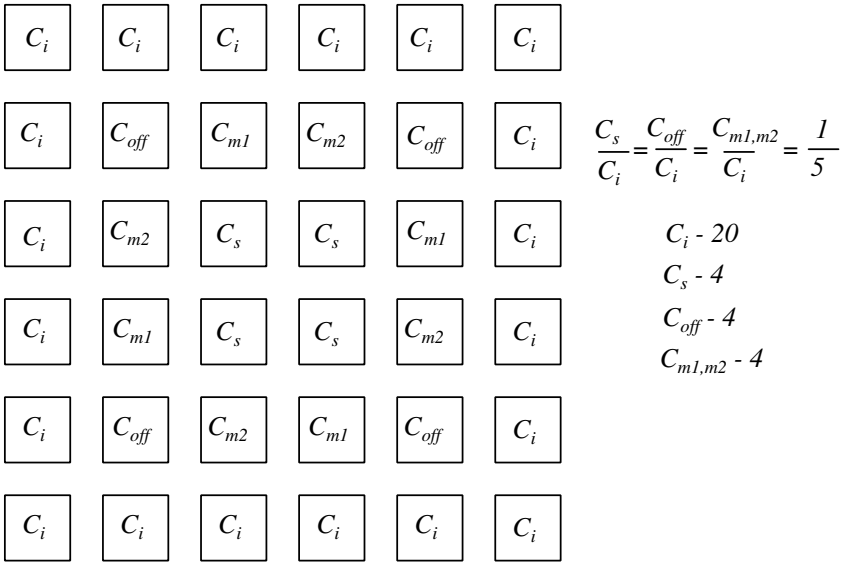

Figure 4.20: Layout scheme of capacitors in 1^{st} integrator

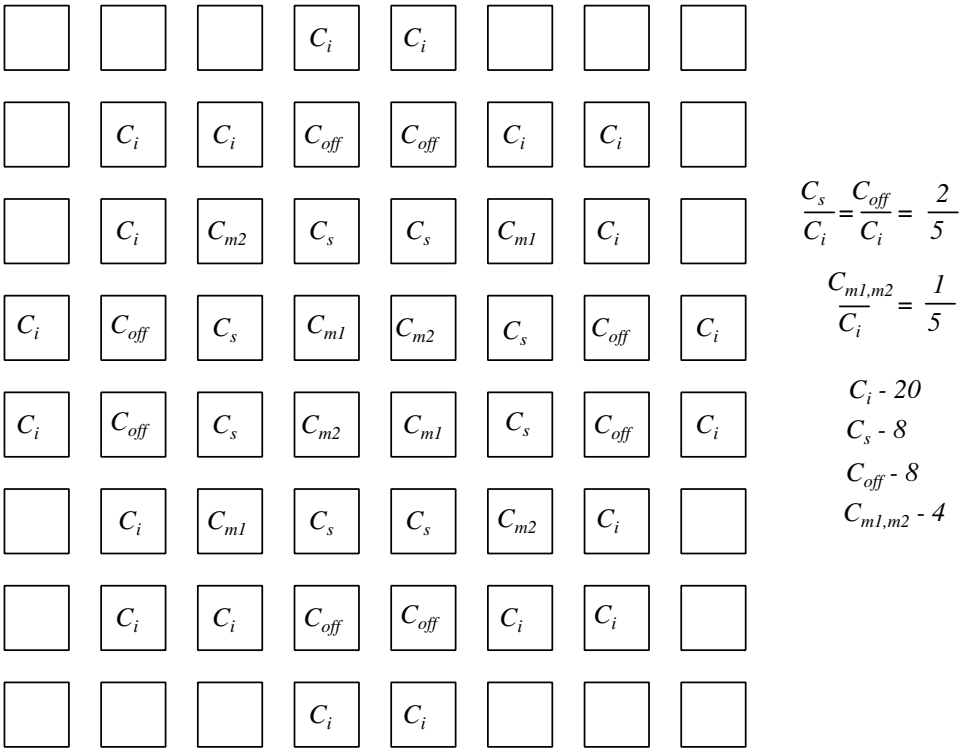

Figure 4.21: Layout scheme of capacitors in 2^{nd} integrator

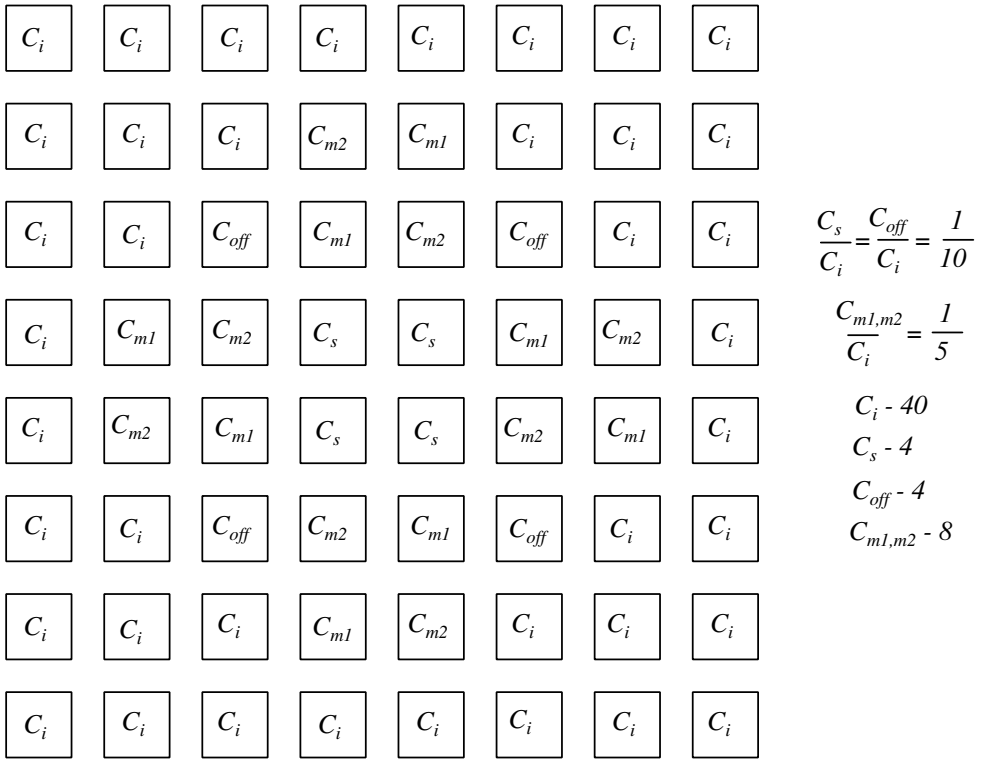

Figure 4.22: Layout scheme of capacitors in 3^{rd} integrator

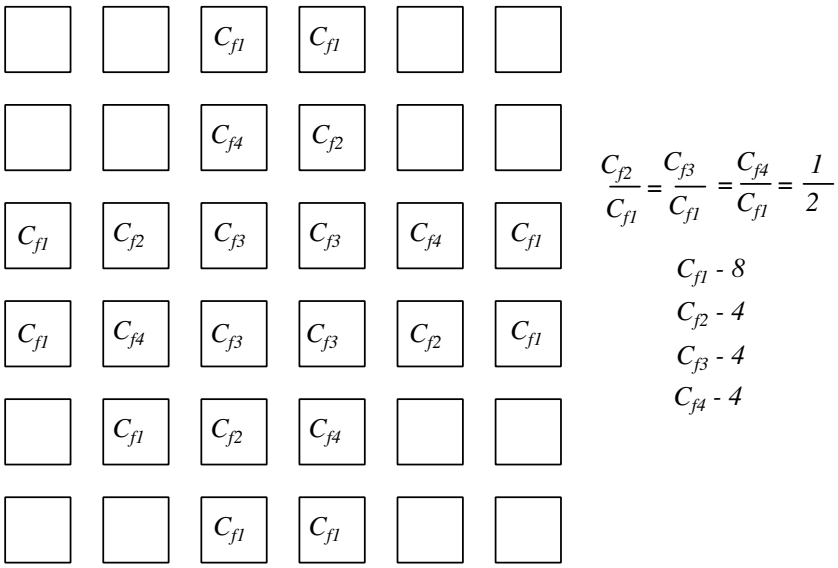

Figure 4.23: Summing stage capacitance implementation

The two identical capacitors implementing common-mode feedback are represented seperately by C_{m1} and C_{m2}, for the ease of placement for matching. C_{f1}, C_{f2}, C_{f3} and C_{f4} are the capacitors implementing the feed-forward summing stage. For a given stage, all the capacitors are realized using a pre-decided unit capacitor.

4.3.7 Quantizer Design

A 1-bit quantizer used in the design of DSM is realized using a dynamic comparator, which are traditionally power efficient. The schematic circuit of the two stage Dynamic Comparator (Van Elzakker et al. 2010) used in this research work is shown in Figure 4.24.

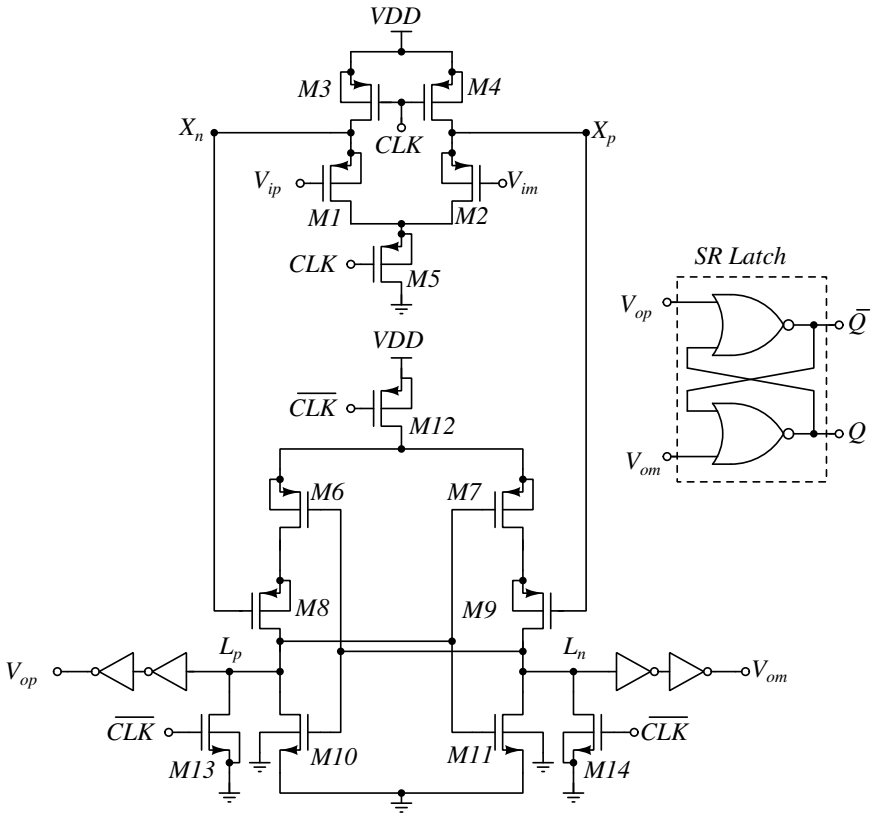

Figure 4.24: Low Power Dynamic Comparator (Van Elzakker et al. 2010)

The first stage formed using transistors $M1 - M5$ is a pre-amplifier with V_{ip} and V_{im} as differential inputs and X_p and X_m as its differential outputs. The second stage

formed using transistors $M6 - M14$ has a simple voltage amplifier and a positive-feedback amplifier to obtain the rail-to-rail output. The differential output from the pre-amplifier stage is fed as input to the second stage through the gate terminals of $M8$ and $M9$. To hold the comparator decision during the reset phase, the differential output V_{op} and V_{om} of the second stage is applied as input to a SR flipflop.

4.3.7.1 Operation of Comparator

The comparator operates in two phases viz-a-viz a reset phase and a comparison phase. The operation of the comparator is as follows.

- **Reset Phase (when 'CLK' signal is at logic '0') :**

  In this phase, nodes X_p and X_m are pre-charged to VDD (through $M3$ and $M4$) and the comparator output nodes V_{op} and V_{om} are reset to 0 V (through $M13$ and $M14$). The SR flipflop holds the last comparator decision during this phase. Also note that transistors $M5$ and $M12$ are turned off in this phase and therefore there is no direct path between the supply rails, resulting in a power efficient design.

- **Comparision Phase (when 'CLK' signal is at logic '1') :**
  During this phase, voltage at pre-charged nodes (X_p and X_n) starts decreasing depending on the input voltages (V_{ip} and V_{im}) and as a result the common-mode voltage at the pre-charged nodes also decreases and the differential voltage increases with time. When the common-mode voltage at the precharged nodes reach a value where $|V_{GS}| > |V_{TH}|$ of transistors $M8$ and $M9$, the voltage amplification in the second stage takes over. As a result, the differential voltage across the nodes L_p and L_m and their common-mode voltage starts increasing. As the common-mode voltage increases gradually, the positive feedback mechanism takes over and resolves them into appropriate logic levels. Once the comparator decision is available, SR flipflop stores that decision.

The sizes of all the transistors used in the comparator circuit are presented in Table 4.3.

A differential voltage ($V_{ip} - V_{im}$) of -100 mV is applied as input to the dynamic comparator operating at a clock frequency of 5.12 MHz. The plots of internal nodes X_p, X_m, L_p and L_m are presented in Figure 4.25.

Table 4.3: Aspect ratio of transistors of the comparator

PMOS	$\left(\frac{W}{L}\right)$	N	NMOS	$\left(\frac{W}{L}\right)$	N
M3	$\left(\frac{0.5}{2}\right)$	4	M1	$\left(\frac{0.5}{2}\right)$	4
M4	$\left(\frac{0.5}{2}\right)$	4	M2	$\left(\frac{0.5}{2}\right)$	4
M6	$\left(\frac{0.5}{2}\right)$	4	M5	$\left(\frac{0.5}{2}\right)$	8
M7	$\left(\frac{0.5}{2}\right)$	4	M10	$\left(\frac{2}{0.18}\right)$	4
M8	$\left(\frac{0.5}{2}\right)$	4	M11	$\left(\frac{2}{0.18}\right)$	4
M9	$\left(\frac{0.5}{2}\right)$	4	M13	$\left(\frac{2.5}{1}\right)$	4
M12	$\left(\frac{0.5}{2}\right)$	4	M14	$\left(\frac{2.5}{1}\right)$	4

W and L are width and length in μm.

N is the number of fingers.

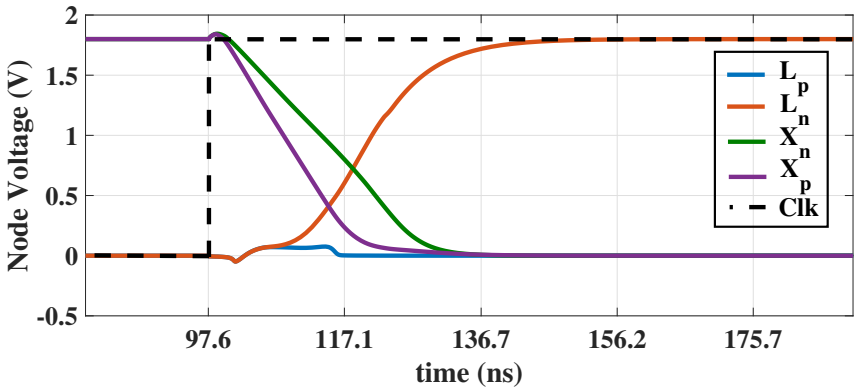

Figure 4.25: Internal nodes of the Comparator during the reset and comparison phase

Since the differential input voltage is negative, current through transistor $M2$ will be higher than that of transistor $M1$. Therefore, the node voltage at X_p decreases relatively faster than the node voltage at X_n. As mentioned earlier, the second stage takes over when the common-mode voltage of X_p and X_m reaches a sufficient value to turn 'ON' the input transistors $M8$ and $M9$ of the second stage. Subsequently, the positive feedback takes over and resolves L_p and L_m into appropriate logic levels i.e. L_p to logic '0' and L_m node to logic '1'.

4.4 SIMULATION RESULTS

The DTDSM is implemented using the proposed IGB-OTA Design-II in UMC 180 nm CMOS technology operating on a supply voltage (VDD) of 1.8 V and common-mode voltage (V_{CM}) of 0.9 V. The layout of the designed DTDSM is presented in Figure 4.26 and it occupies an area of 514 μm$\times$ 778 μm. Figure 4.27 shows the power spectral density (PSD) of the DSM output, when a 1.015 kHz, -6 dBFS input sinusoidal signal is applied. MATLAB's Delta Sigma toolbox (open source) (Schreier 2020) has been used for plotting the PSD and NBW in the plot represents noise bandwidth. Note that the full-scale here is assumed as rail-to-rail voltage i.e., 1.8 V.

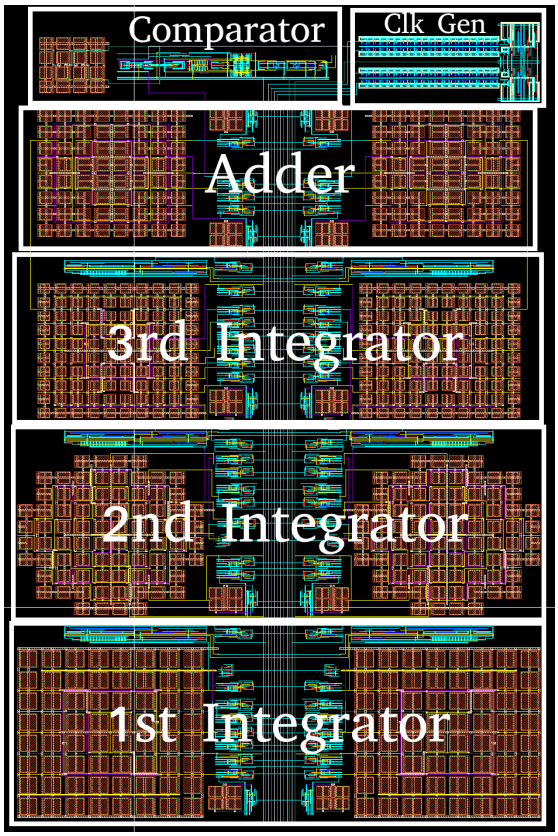

Figure 4.26: Layout of pseudo differential DSM

For simulations, it is common to choose an input frequency such that at-least 10 harmonics fall within the signal band. For audio applications, this amounts to an input frequency around 1 kHz. The actual value of input frequency f_{in} to be chosen is based on the number of points (N) for DFT computation and the clock frequency

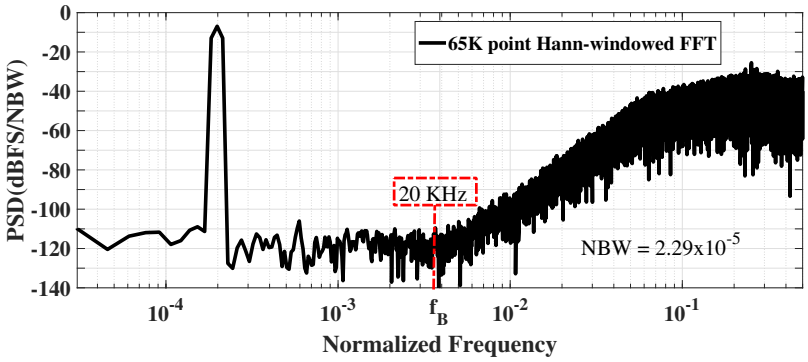

Figure 4.27: PSD of DSM output

(f_{clk}) such that the relation given in (4.27) is valid.

$$\frac{f_{clk}}{f_{in}} = \frac{2^N}{Q} \tag{4.27}$$

where, Q is a number relatively prime to 2^N. N is chosen to be 16 in this work which amounts to 65536 DFT points (or bins). Therefore, it can be found that for a Q of 13, f_{in}=1.015 kHz satisfies the equality given in (4.27).

A large number of bins are chosen for the following reasons.

- The noise power spreads across more number of bins, thereby reducing the noise floor.
- Lower noise floor reduces the spectral leakage into harmonic components during DFT computation.
- It allows windowing technique to be adopted for computing DFT. In order to obtain an accurate spectrum, the designer must choose a window that introduces sufficiently low errors when spectral convolution is performed or in other words, window with a better high-frequency attenuation (side lobe suppression) should be chosen. Hann window provides sufficient protection against noise leakage than a rectangular window (Schreier et al. 2005) and hence it is used for computing DFT.

The plot of SNR & SNDR versus the input amplitude for a 1.015 kHz signal is presented in Figure 4.28. A linearly increasing plot for lower input power shows that

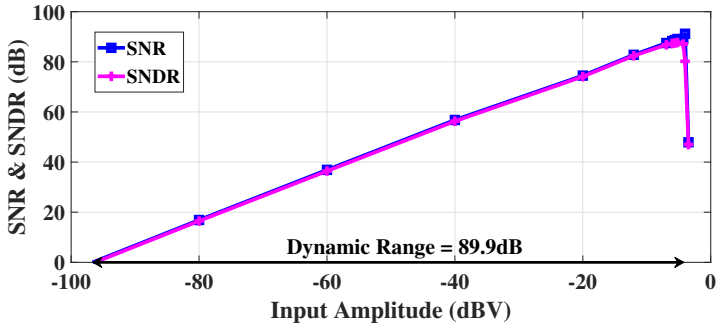

Figure 4.28: SNR & SNDR of DSM output versus the input amplitude

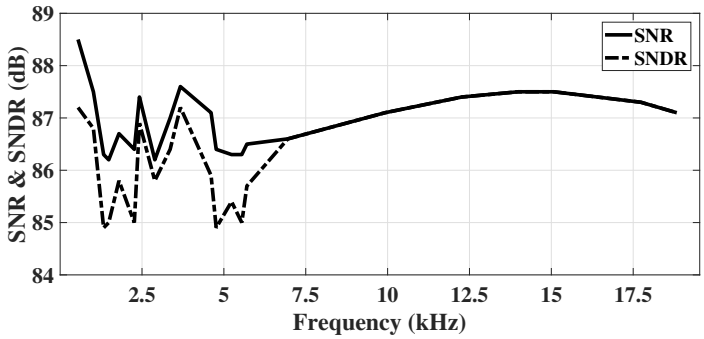

Figure 4.29: SNR & SNDR of DSM output versus the input signal frequency

noise power is almost constant. The plot drops back at higher inputs after reaching a peak value. This is because the distortion terms increase at higher inputs. The input at which the SNR drops below the peak value by 6 dB is called as the Overload Level and is found to be 1.26 V differential. The designed DSM delivers a peak SNR & SNDR of 91.2 dB & 87.7 dB respectively. The dynamic range offered by the DSM is 89.9 dB. Figure 4.29 shows the SNR & SNDR performance against the frequency of input sinusoid with an amplitude of -6 dBFS. It can be noted that SNDR is in excess of 85 dB for the entire audio band, thus offering a robust performance. For above 7 kHz, both SNR and SNDR are found to be almost same. This is because the the dominant third harmonic falls out of the band.

The overall power consumption of the DSM consumes is 570.6 μW when no input is applied, including both static and dynamic power. A breakdown of the power consumption into each block is shown as a pie-chart in Figure 4.30. The 1^{st} stage integrators takes 39 % of the total power. The 2^{nd} and 3^{rd} stage integrators take 26 % each. The dynamic comparator consumes 7 % while the clock generation circuit and

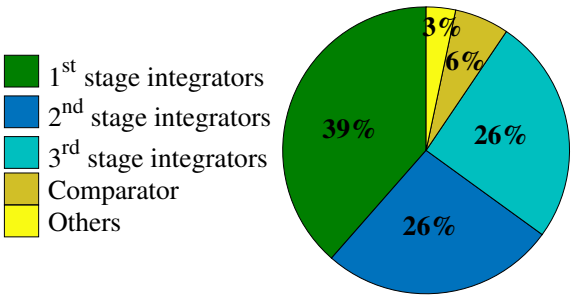

Figure 4.30: Power breakdown of DSM

others consume 6 %.

4.5 PERFORMANCE SUMMARY

The performance of the designed DSM is summarized in Table 4.4 for a typical process corner at room temperature.

Table 4.4: Summary of DSM's performance

Parameter	**Value**
Technology	180 nm
Supply	1.8 V
Architecture	Discrete-time
Bandwidth	20 kHz
OSR	128
Sampling Frequency	5.12 MHz
SNR_{peak}	91.2 dB
$SNDR_{peak}$	87.7 dB
$SFDR_{peak}$	102.0 dB
Dynamic Range	89.9 dB
Overload Level	630 mV
Power Consumption	570.6 μW

4.6 COMPARISON WITH OTHER WORKS

The performance of the designed DSM is compared with some of the works reported in literature and the comparison is presented in Table 4.5.

Table 4.5: Comparison with other works

	Pun et al. (2007)	Kim et al. (2008)	Kuo et al. (2010)	Ismail and Mostafa (2016)	Cardes et al. (2018)	**This Work**
Architecture	CT	DT	DT	CT	CT	DT
Process (nm)	180	130	180	130	130	**180**
Supply (V)	0.5	0.9	1	0.9	1.8	**1.8**
Bandwidth (kHz)	25	24	20	20	20	**20**
OSR	64	128	100	50	500	**128**
SNR (dB)	80	91	87	82	-	**91**
SNDR (dB)	74	89	84	73	77	**88**
DR	-	92	88	83	99	**90**
Power (μW)	300	1500	660	60	560	**571**
FoM_{DR} (dB)	-	137	163	168	174	**165**
FoM_{SNDR} (dB)	153	161	159	158	152	**162**
FoM_{Wa} (fJ/Conv)	1465	1356	1273	410	2419	**695**
Results Type	MR	MR	MR	SR	MR	PLSR

DT - Discrete Time CT - Continuous Time

MR - Measured Results SR - Simulation Results

PLSR - Post Layout Simulation Results

FoM's used for the comparison are given in (4.28), (4.29) (Lee et al. 2016) and

(4.30) (Chae and Han (2009)).

$$FoM_{DR} = DR + 10\,log\left(\frac{Bandwidth}{Power}\right) \tag{4.28}$$

$$FoM_{SNDR} = SNDR + 10\,log\left(\frac{Bandwidth}{Power}\right) \tag{4.29}$$

$$FOM_{Wa} = \frac{Power}{2.Bandwidth.2^{(SNDR-1.76)/6.02}} \tag{4.30}$$

Higher the $\mathrm{FoM_{DR}}$ and $\mathrm{FoM_{SNDR}}$, better is the design. Conversely, design with lower $\mathrm{FoM_{Wa}}$ is better.

It can be observed that the performance of the designed DSM, using the proposed IGB-OTA, is found to be on-par with other works. This validates the usefulness of the proposed OTA in high performance applications.

Chapter 5

ON-CHIP CLASS D AMPLIFIER

Power amplifier is one of the basic building blocks of an audio playback system. CDAs are considered as the choice when efficiency matters. However, non-linearity measured in terms of THD+N is one of the key parameters of CDAs. The in-band noise can be reduced if noise shaping is employed for CDAs. Therefore, CDAs with DSM in the loop are best suited for this performance. But, it is also required that the power loss in the circuit is minimized in order to get a good efficiency.

The IGB-OTA, proposed in this thesis, being proved to be power efficient and one of the candidates for DTDSMs, a CDA has been designed to prove the suitability of the IGB-OTA. This chapter explains the design of an on-chip CDA for driving an $8\,\Omega$ speaker load and proves that the THD+N and efficiency is on par with the similar CDAs found in the literature.

The first section outlines the fundamental concepts of CDA and its conventional open-loop design in brief. The remaining part of the chapter outlines the design of closed loop CDA using DTDSM.

5.1 INTRODUCTION

An audio power amplifier amplifies a low power audio signal (typically of hundreds of micro-watts) to a level suitable for driving a speaker load. The output power varies from application to application. It varies from few hundreds of milli watts for ear/head phones to hundreds of watts for loud speakers. Classically, Class AB power

amplifiers have been the preferred choice of the audio systems designer for a long time. The main reason for this is that these amplifiers are highly linear. But this class of amplifiers has got a major disadvantage that it has a maximum efficiency of only 78% theoretically ($\leq$ 75% practically). That means more than 22% of the input power is lost as power dissipation, compelling the designers to use heat sinks making them bulky. In addition, for battery operated system, this type of amplifier is not suited because of poor efficiency.

Class D power amplifier has 100% power efficiency theoretically ($>$ 80% practically) (Self 2013); which means that most of the input power is delivered to the load. The increased efficiency in a Class-D amplifiers provides two main advantages over Class AB amplifiers. The first advantage is, higher power efficiency, which means that the energy drawn from the battery is almost utilized in the speaker, which translate to longer battery run-time. The second advantage is, low power dissipation which eliminates the need for bulky heat sinks.

However, CDAs suffer from an inherent drawback of poor distortion performance (Self 2013). Recent advances in semiconductor technology have renewed interest in Class-D audio amplifiers as they can be integrated into silicon chips, especially for portable and consumer electronics such as hearing aids, multimedia players, notebook computers, USB hub-powered/wireless speakers, automotive audio amplifiers, etc,. So, the need to squeeze more power capability into a smaller space while generating less heat, has been driving their development over the last few years.

5.1.1 Basic operation of class D amplifier

CDAs are a completely different class of power amplifiers and they operate on an entirely different principle when compared to other classes of amplifiers. The transistors, responsible for power amplification are used as switches which are either ON (saturation region) or OFF (cut-off region). When the output transistor is ON, the drop across the switch is zero (ideally) and when it is OFF, current through the switch is zero. So, in both the cases the VI product is zero implying that there is no power dissipation. Therefore, ideally, efficiency of a class D power amplifier is 100%. Figure 5.1 shows the basic building blocks of an open loop CDA.

The modulator block consists of a comparator which compares the input audio signal with a reference triangular signal. If the input audio signal is greater than

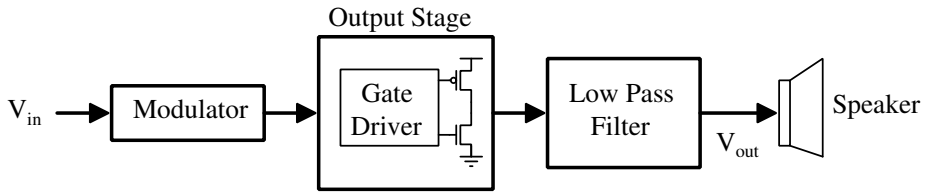

Figure 5.1: Open loop Class D amplifier (Gaalaas 2006)

the reference triangular signal then comparator produces a pulse which lasts as long as the input audio signal is greater than the reference triangular signal and thus a pulse width modulated (PWM) signal is generated by the modulator block as shown in Figure 5.2. This PWM signal is fed as input to the switching output stage. Now, the switching output stage amplifies this PWM signal by a factor of $\frac{V_{rail}}{V_{tri}}$ (Cordell 2011); where V_{rail} is the supply voltage of switching output stage and V_{tri} is the peak voltage of the reference triangular signal. The average of this amplified PWM signal represents the amplified input signal. Therefore, the amplified PWM signal is filtered using a low-pass filter to extract the amplified audio signal and reject the higher frequency components corresponding to the reference triangular signal.

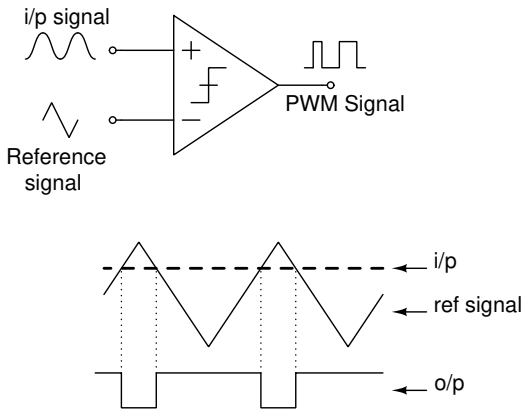

Figure 5.2: Pulse Width Modulator of a Class D power amplifier (Cordell 2011)

Figure 5.3 shows a half bridge configured output stage along with the output filter stage. The output stage has two transistors M_1 and M_2 as switches. M_1 is the high-side switch and M_2 is the low-side switch. When the high-side switch is ON, then the low-side switch is kept OFF and vice-versa. Therefore, choosing M_1 to be a PMOS transistor and M_2 to be a NMOS transistor simplifies the driving scheme. Output at the common-drain point will be the amplified PWM. The inductor, capacitor and

the speaker together form a low-pass filter network which extracts the low frequency components and attenuates the high frequency components of the PWM signal. The

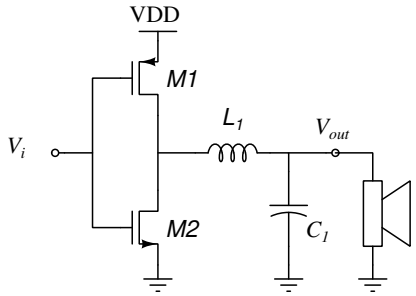

Figure 5.3: Half bridge configured output switching stage (Cordell 2011)

linearity offered by open loop CDA is very poor and therefore negative feedback has been employed in CDAs, as shown in Figure 5.4, to improve the linearity. In addition, with the use of oversampling along with noise shaping, the overall THD+N can be improved to a large extent. Accordingly, DSM based topology has become a widely used choice for implementing CDA's. A block diagram representation of a DSM based CDA is shown in Figure 5.5.

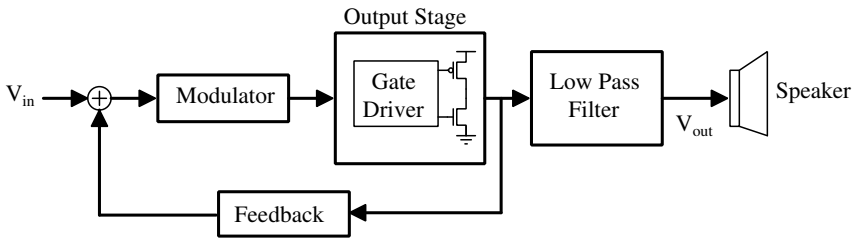

Figure 5.4: Schematic of a feedback CDA (Yu et al. 2009)

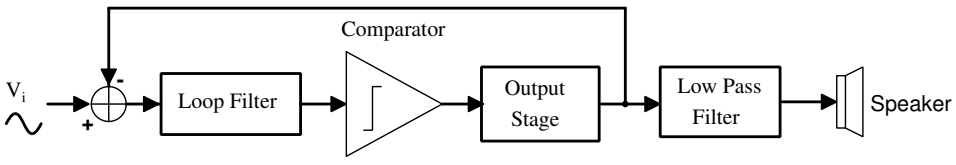

Figure 5.5: DSM based CDA (Cordell 2011)

5.1.2 Performance metrics

The common metrics used for measuring the performance of CDA are given as follows (Cordell 2011).

- **Total Harmonic Distortion (THD):**

  It is defined as the ratio of sum of the powers of the harmonic components inside the signal bandwidth to the power of the fundamental component.

- **Total Harmonic Distortion plus Noise (THD+N):**

  It is defined as the ratio of sum of the powers of the harmonic components inside the signal bandwidth plus the in-band noise power to the power of the fundamental component.

- **Efficiency (η):**

  It is defined as the ratio of total power delivered to the load to the total power consumed and it is expressed in percentage.

5.2 DTDSM BASED CLASS D AMPLIFIER USING THE PROPOSED IGB-OTA

The IGB-OTA Design-II proposed in this research work is found to be a very good candidate for implementing DTDSM. Encouraged with the low power performance of the DTDSM, a DTDSM based Class-D amplifier has been designed using the proposed IGB-OTA Design-II. The focus is on achieving a low power for the control circuit and thereby improving the efficiency. This chapter discusses the design of CDA. A simplified schematic of a DTDSM based CDA is shown in Figure 5.6. The output stage is a Full-bridge (H-bridge) inverter, consisting of two PMOS ($M1p$ and $M2p$) and two NMOS ($M1n$ and $M2n$) transistors, that drives the load which is assumed to be a $8\,\Omega$ speaker. The power stage is driven by the proposed DSM block. However, the feedback is taken from the output of the power stage i.e., $V_{fb,p}$ and $V_{fb,n}$. The feedback loop acts in such a way that the output follows the input with a unity gain.

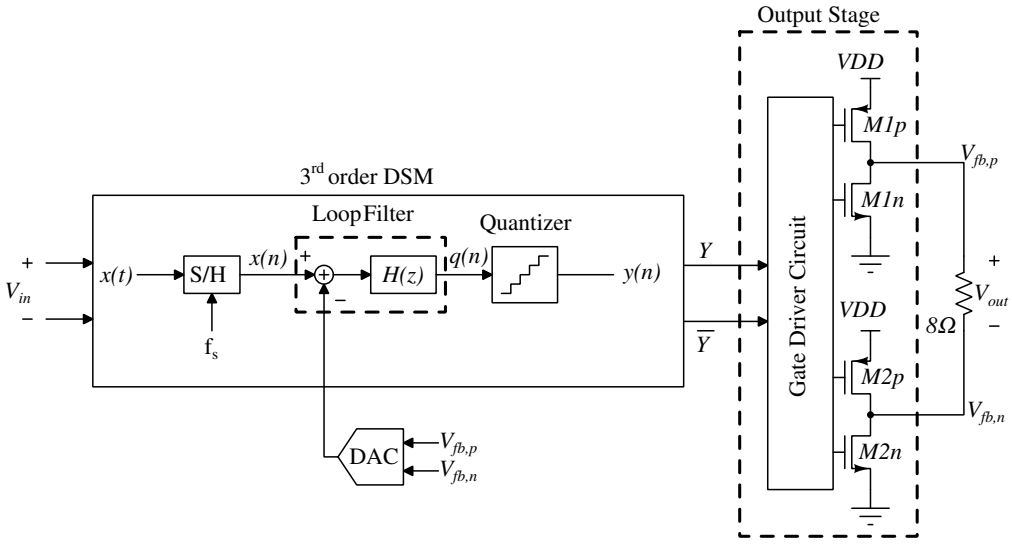

Figure 5.6: $\Delta\Sigma$ modulator based CDA

Desired specifications for DTDSM-based CDA, inferred from the literature (Kang et al. 2008, Noh et al. 2012, Hwang et al. 2014, Colli-Menchi et al. 2014, Chang and Wu 2017), are given in Table 5.1

Table 5.1: Desired specifications for the CDA

Metric	Typical Value
THD+N(%)	< 0.01
DR (dB)	> 85
SNR (dB)	> 80
Load Impedance (Ω)	8
Efficiency (%)	> 90

5.2.1 Design of Power Stage

Consider the H-bridge output stage shown in Figure 5.7a. Transistors $M1p$ and $M1n$ form left leg of the output stage and $M2p$ and $M2n$ form the right leg. Ideally, at any given point of time, a PMOS transistor from one leg and a NMOS transistor from the other leg will be ON. As shown in the figure, when $M1p$ and $M2n$ are ON, the load

current will flow from left to right and the current direction is opposite when $M2p$ and $M1n$ are turned ON. An equivalent circuit for this scenario can be drawn as shown in Figure 5.7b. $R_{on,p}$ and $R_{on,n}$ are the on-state resistances of the PMOS and NMOS transistors respectively. $R_{par,up}$ and $R_{par,down}$ are the effective parasitic resistances appearing in series with PMOS and NMOS transistors respectively. Therefore, the voltage across the load will be less than the ideal expected value of V_{DD}. Or in other words, there are power losses in transistors and parasitic resistances degrading the efficiency.

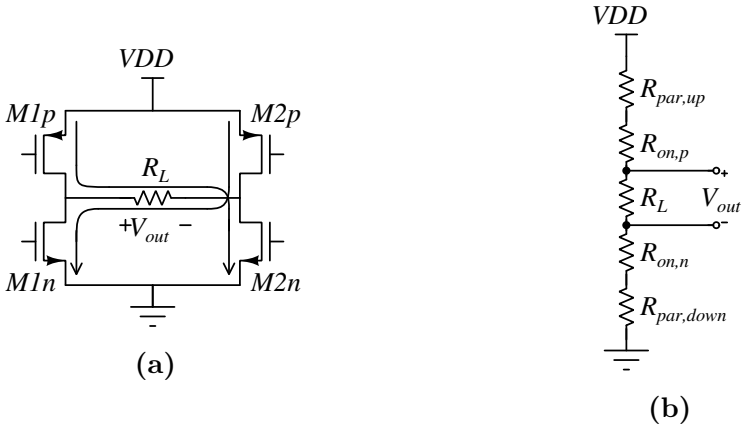

Figure 5.7: H-brige power stage (a) Schematic (Cordell 2011)(b) Equivalent circuit.

The efficiency of the power switches η_{sw} of the circuit shown in Figure 5.7a is defined as the ratio of power delivered to R_L (P_L) and the power drawn from the supply (P_{DD}), which can be written as in (5.1)

$$\eta_{sw} = \frac{P_L}{P_{DD}} = \frac{R_L}{R_{par,up} + R_{on,p} + R_L + R_{on,n} + R_{par,down}} \tag{5.1}$$

The parasitic resistances are predominantly contributed by transistor contacts and via between the metal layers in an on-chip CDA. With a careful layout strategy, $R_{par,up}$ and $R_{par,down}$ can be made negligible to R_L. However, on-state resistances of the transistors cannot be made exorbitantly low. Because, reducing on-state resistance will call for a large transistor size. Large size transistors demand stronger driving stages and thus increasing dynamic losses.

In the targeted CDA, the expected output power is computed to be ≈100 mW for a full-scale peak-to-peak input of 1.26 V for an 8Ω load. Setting the power bud-

get for the power loss in on-state resistances to be about 2.5% of output power i.e. η_{sw} =97.5% and assuming $R_{on,n} = R_{on,p}$, from (5.1), it can be computed that $R_{on,n} = R_{on,p}$ ≈100 mΩ. Accordingly transistors are sized to offer the desired on-state resistance. The sizes of transistors chosen are given in Table 5.2, along with their on-state resistance. Such large sized transistors offer a significantly large input

Table 5.2: Aspect ratio of power transistors of output stage

Transistor	$\left(\frac{W}{L}\right)$	N	On-resistance (mΩ)
$M1p,\ M2p$	$\left(\frac{3.91}{0.18}\right)$	6400	101.2
$M1n,\ M2n$	$\left(\frac{8.12}{0.18}\right)$	640	101.8

W and L are width and length in μm.

N is the number of fingers.

capacitance due to the gate-source capacitance. DSM designed in Chapter 4 is not designed for driving large capacitive loads. Therefore, it is required that output of the DSM be buffered before driving the power-stage transistors. Note, it is desired that PMOS and NMOS power transistors belonging to the same leg of the H-bridge output stage should not be ON simultaneously at any point of time. If both the transistors of a leg are in ON-state then it means that the DC power supply is connected to ground though very small on-state resistances of transistors. This causes a very high shoot-through current to flow through power switches. For the above reasons, a gate driver circuit block in Figure 5.6 is used.

5.2.2 Gate Driver Circuit

There are two identical gate driver circuits (GDC-1 and GDC-2) each driving a PMOS and a NMOS transistors placed diagonally in the H-bridge. GDC-1 takes the output Y from the DSM and drives the transistors M2n and M1p. Similarly, GDC-2 takes its input from $\overline{Y}$ and drives M2p and M1n. Figure 5.8 shows schematic of the GDC. Both the GDC-1 and GDC-2 consists of a non-overlapping circuit and an inverter buffer chain. The inverter chain buffers the outputs of non-overlapping clock generation circuit before feeding them to the corresponding power switches. The buffer chain consists of four inverters connected in cascade. Since the sizes of PMOS and NMOS

power switches are different, the inverter chains are sized accordingly and the sizing of the four inverter for both the power switches are presented in Table 5.3. PMOS transistors are sized twice to that of NMOS transistors in the inverter buffer chain. The gate driver circuit is designed to ensure that PMOS and NMOS of the any given leg are never turned on simultaneously by providing a dead-time of approximately 2 ns (amounting to about 1% of the clock period). The delay introduced by the gate driver circuit is less than 0.5 ns.

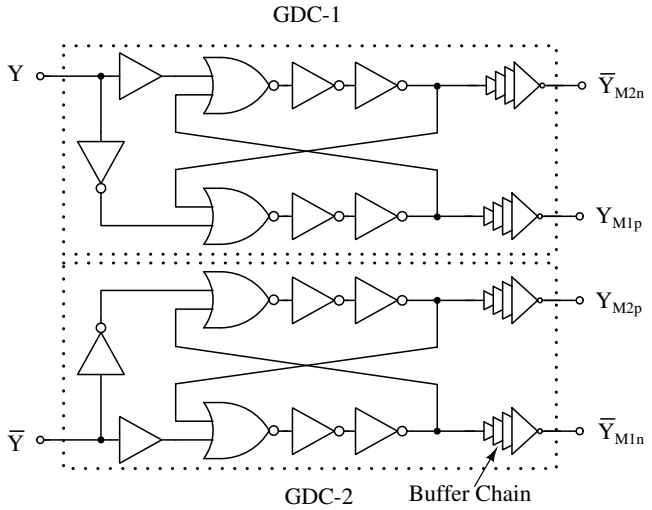

Figure 5.8: Gate driver circuit (Pavan et al. 2017)

Table 5.3: Sizing of inverter buffer chain

Power Switch	PMOS				NMOS			
Inverter	PMOS		NMOS		PMOS		NMOS	
	$\left(\frac{W}{L}\right)$	N	$\left(\frac{W}{L}\right)$	N	$\left(\frac{W}{L}\right)$	N	$\left(\frac{W}{L}\right)$	N
Inv 1	$\left(\frac{0.96}{1}\right)$	1	$\left(\frac{0.32}{1}\right)$	1	$\left(\frac{0.96}{1}\right)$	1	$\left(\frac{0.32}{1}\right)$	1
Inv 2	$\left(\frac{3.91}{0.18}\right)$	10	$\left(\frac{3.91}{0.18}\right)$	5	$\left(\frac{8.12}{0.18}\right)$	4	$\left(\frac{8.12}{0.18}\right)$	2
Inv 3	$\left(\frac{3.91}{0.18}\right)$	80	$\left(\frac{3.91}{0.18}\right)$	40	$\left(\frac{8.12}{0.18}\right)$	24	$\left(\frac{8.12}{0.18}\right)$	12
Inv 4	$\left(\frac{3.91}{0.18}\right)$	560	$\left(\frac{3.91}{0.18}\right)$	280	$\left(\frac{8.12}{0.18}\right)$	100	$\left(\frac{8.12}{0.18}\right)$	50

W and L are width and length in μm.

N is the number of fingers.

5.3 SIMULATION RESULTS

The CDA is designed using UMC 180 nm CMOS technology. It is operated on a 1.8 V power supply. The input is differential riding on a common-mode voltage (V_{CM}) of 0.9 V. A layout of the CDA is shown in Figure 5.9. The total area occupied by CDA is 1.78 mm× 1.3 mm. To handle the large currents in the output stage, the supply rails (VDD and GNDA) and the output node are implemented using wider metal layers with slots for limiting the current density per μm width metric to a permissible value.

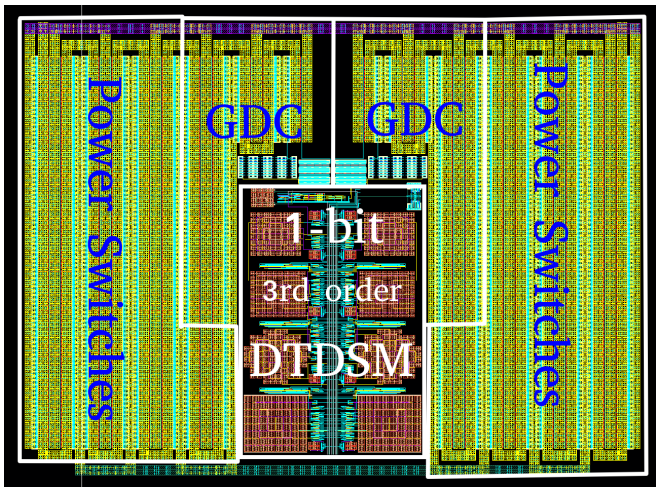

Figure 5.9: Layout of CDA

The CDA is simulated for an excitation of -6 dBFS (1.8 V peak-to-peak differential) having a frequency of 1.015 kHz. Figure 5.10 shows the power spectral density (PSD) of the CDA output so obtained. The CDA is found to offer a peak SNR 90.2 dB and a peak SFDR of 87.5 dB. The dynamic range offered by the CDA is 89.7 dB. Figure 5.11 shows the plot of THD+N versus the input signal amplitude for a 1.015 kHz signal. The CDA is found to offer a best THD+N of 0.005% for an input of 1.2 V peak to peak. The variation of THD+N with input signal frequency for a -6 dBFS input sinusoidal signal amplitude is shown in Figure 5.12 and the performance is found to be robust with THD+N being less than 0.01%. Note that, beyond 7 kHz, THD+N is almost constant due to the fact that the dominant third harmonic component falls out of the band.

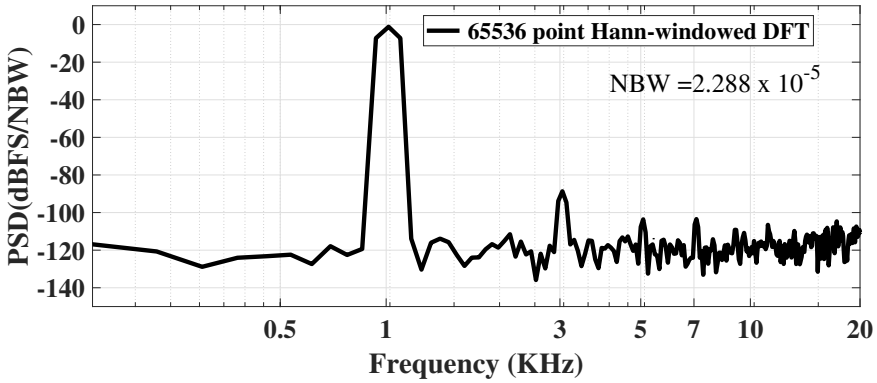

Figure 5.10: PSD of CDA's output

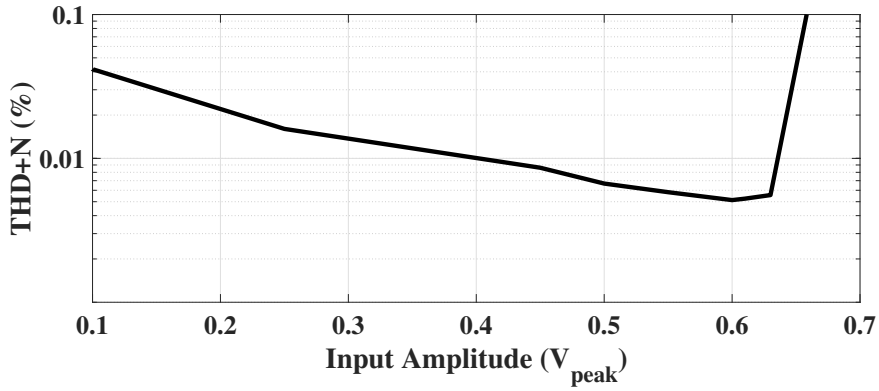

Figure 5.11: THD+N of CDA's output versus the input signal amplitude

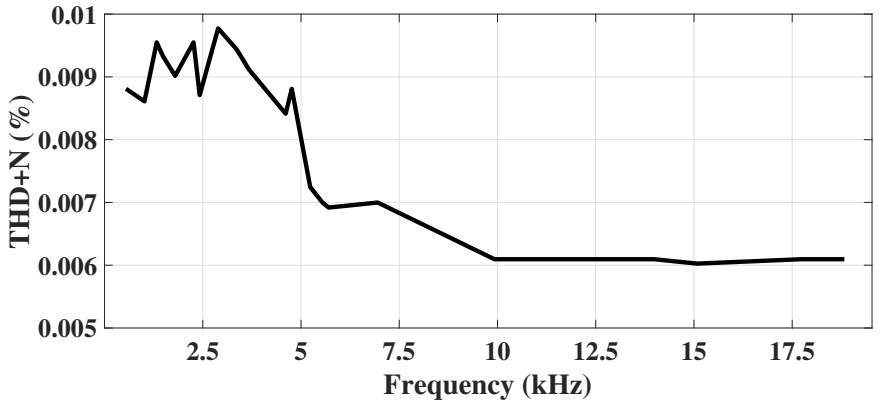

Figure 5.12: THD+N of CDA's output versus the input signal frequency

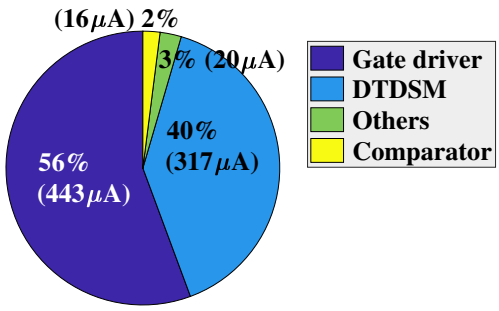

Figure 5.13: Distribution of Quiescent current consumption

The quiescent current consumption of the designed CDA (when no input is applied) is found to be 796 μA and its distribution is shown in Figure 5.13. The performance summary of the class D amplifier is oulined in Table 5.4.

Table 5.4: Summary of CDA's performance

Parameter	**Value**
Technology	180 nm
Supply	1.8 V
Modulator Architecture	Discrete-time $\Delta\Sigma$
Bandwidth	20 kHz
Sampling Frequency	5.12 MHz
SNR_{peak} (dB)	90.2 / 94.5*
$SNDR_{peak}$ (dB)	85.8 / 90.1*
$SFDR_{peak}$ (dB)	87.5
THD_{best} (dB)	-90.7 / -96.3*
$THD+N_{best}$ (dB)	-85.8 / -90.9*
Dynamic Range	89.7 dB
Maximum Output Power	100 mW
Quiescent Current (I_Q)	796 μA
Efficiency	92.3 % @ 100 mW
Load	8 Ω

* - A-weighted

5.4 COMPARISON WITH OTHER WORKS

The performance of the designed CDA is compared with other works and it is presented in Table 5.5.

Table 5.5: Comparison with other works

	Kang et al. (2008)	Noh et al. (2013)	Colli-Menchi et al. (2014)	Hwang et al. (2014)	Chang and Wu (2017)	**This Work**
Architecture	DTDSM	DTDSM	PWM	PWM	DPC	DTDSM
Technology (nm)	180	130	180	180	65	180
Supply Voltage (V)	3	1.2	1.8	1.5	1	1.8
Speaker Load (Ω)	32	160	8	16	32	8
f_s (MHz)	3.2	5	0.5	1	0.384	5.12
SNR (dB)	80	87	88	84	93*	92/97*
THD+N (dB)	-73	-82	-76	-68	-84	-91/-96*
Dynamic Range (dB)	-	87	-	-	95*	90
Power Efficiency (%)	77	97	94.6	90	89	92
Max. P_{out} (mW)	-	1.14	250	20	13.3	100
I_Q (μA)	2567	317	198**	762	875	796
FoM	0.1	39	30	3	16	41
Results Type	MR	MR	MR	MR	MR	PLSR

DPC - Digital to Pulse Conversion PWM - Pulse Width Modulation

* A-weighted ** Single-Ended

MR - Measured Results PLSR - Post Layout Simulation Results

Figure of Merit (FoM) used for comparison is given in (5.2) (Hwang et al. 2014).

$$FoM = \frac{\eta(\%)}{I_Q(mA) * THD + N(\%) * 10^5} \tag{5.2}$$

From the above table it is clear that the designed CDA offers highest linearity (higher THD) and consumes lower quiescent current despite the design not optimized for low power consumption. It achieves a relatively good FoM and thus validating the worthiness of the proposed IGB-OTA in this application.

Chapter 6

CONCLUSIONS AND FUTURE SCOPE

6.1 CONCLUSIONS

Inverter-based OTA's are found to replace traditional OTA's in high performance applications such as data converters, where a higher dc gain . Design simplicity is the unique selling proposition of inverter-based OTA's. However, these inverter-based OTA's are only suitable for low voltage applications (< 1V) because they consume a lot of power when operated on higher supply voltages. This research proposed an architecture for high gain low power inverter-based OTA operating on a higher supply voltage (1.8 V). Cascoding and gain-boosting techniques are employed for achieving a higher dc gain. The proposed OTA architecture does not require frequency compensation for closed loop stability. The proposed OTA has been designed for two applications namely, bio-medical and audio applications. The OTA designed for biomedical applications offered a dc gain of 109.3 dB and a UGB of 5.29 MHz at 81° phase margin (PM) with a capacitive load of 2.5 pF for a typical process corner at room temperature (27°C). The quiescent current consumption of the OTA is 4.79 μA. And the second OTA designed for audio applications offered a dc gain of 96.8 dB and a UGB of 19.4 MHz at 86° phase margin (PM) with a capacitive load of 5 pF for a typical process corner at room temperature. This design draws a quiescent current (I_Q) of 38.4 μA. The FOM validates that the proposed inverter-based OTA is among

the best.

A delta sigma modulator has been designed to validate the suitability of the proposed OTA. A 1-bit third order discrete-time delta sigma modulator using feed-forward topology has been designed for audio applications. It achieves a peak SNR of 91.2 dB and peak THD+N of -87.7 dB along with a dynamic range of 89.9 dB. The modulator consumes 570.6 μW operating on 1.8 V supply. The Figure-of-Merit proves that the modulator is a fitting candidate among similar modulators found in the literature.

Extending further, a Class D audio amplifier has been designed using the 1-bit third order discrete time delta sigma modulator. It offered a dynamic range of 89.7 dB along with a best THD+N of -85.8,dB for 8 Ω speaker load delivering a maximum power of 100 mW while operating on 1.8 V supply. The amplifier is found to be one of the best in its class.

6.2 FUTURE SCOPE

Since the proposed OTA architecture is stable without using any kind of frequency compensation, a two stage OTA design can be attemped to achieve an even higher dc gain. A common-source amplifier could be used as a second stage which will improve the dc gain as well as the output swing.

The performance of the proposed OTA is found to be sensitive to process, voltage and temperature. It is observed that if I_{REF} is made to have a negative coefficient w.r.t power supply and temperature then the performance of the proposed OTA can be made insensitive to process, voltage and temperature. A dynamic bias circuit having a negative coefficient w.r.t power supply and temperature could be designed to compensate the effect of process, voltage and temperature on the performance of inverter-based OTA.

A DSM for biomedical applications using OTA Design-I can be designed. Although, auto-zeroing technique can reduce the low frequency noise, the maximum SNDR that can be achieved will be limited by the low frequency noise. So, use of single-bit higher order modulator will not be a wise choice. A multi-bit quantizer could be beneficial. Research in this direction could be looked at.

Appendix I
MATLAB Psuedo Codes and Simulink model

A-1 MATLAB psuedo code: Generating the filter coefficients of DSM

In this section, MATLAB psuedo code for generating the filter coefficients of a DSM is presented. For starters, download the MATLAB's Delta Sigma Toolbox (Schreier 2020) and set the path correctly. The following code is taken from Schreier et al. (2005).

Following are the input data needed for the code to find the filter coefficients of DSM using MATLAB's Delta Sigma Toolbox.

- form - Topology of filter implementation
- order - order of the loop filter
- osr - oversampling rate
- nz - '1' if zeroes of NTF has to be optimized for maximizing SNR
  '0' otherwise
- lim - limiting factor for the output nodes of all integrators.

Once these input specifications are finalized, the following code can be used for generating the filter coefficients.

```
========================================================================
Designing a 3rd order DSM with an OSR of 128 using feedforward topology.
All the internal nodes have to be limited to 40% of max. available swing.
------------------------------------------------------------------------

                                CODE

------------------------------------------------------------------------
form = 'CIFF';           % Cascade of Integrator with Feed-Forward topology
order = 3;
osr = 128;
lim =0.4;                 % limiting internal nodes to 40% of maximum swing
ntf = synthesizeNTF(order,osr,nz);      % designing NTF based on input specs
[ai,gi,bi,ci] = realizeNTF(ntf,form); % generating filter coefficients from NTF
% Internal nodes are not yet limited to the desired value (i.e., 40%).
% The following code accomplishes that task
ABCD = stuffABCD(ai,gi,bi,ci,form);
[ABCDs,  umax] = scaleABCD(ABCD,2,0,lim);
[a,g,b,c] = mapABCD(ABCDs,form);        % final filter coefficients
========================================================================
```

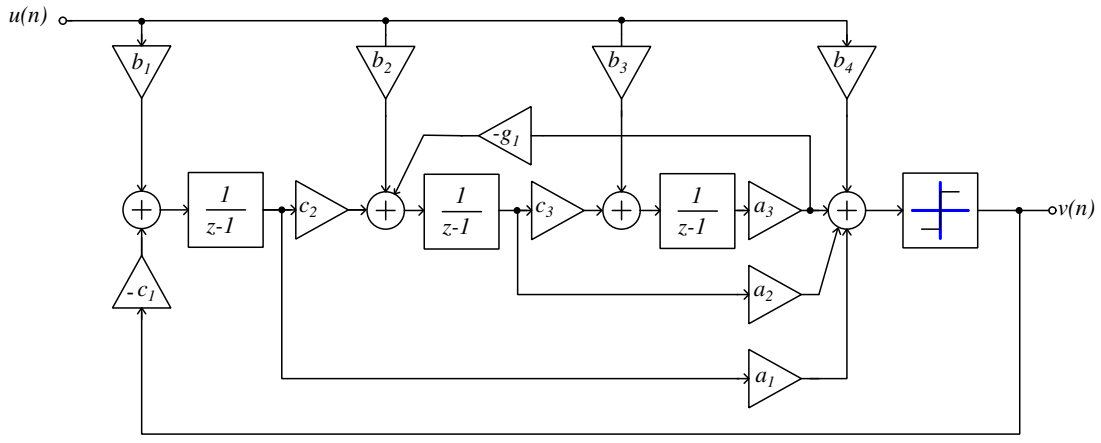

Figure A.1: Cascade of Integrator with Feed-Forward topology

[a, g, b, c] matrix represents the solution for filter coefficients and should be interpreted as shown in Figure A.1.

A-2 Simulink Model of DSM

In this section, the Simulink link model used for verifying the DSM stability for different input amplitudes and frequency is presented.

Figure A.2 shows the simulink model of 3rd order feed-forward topology based DSM.

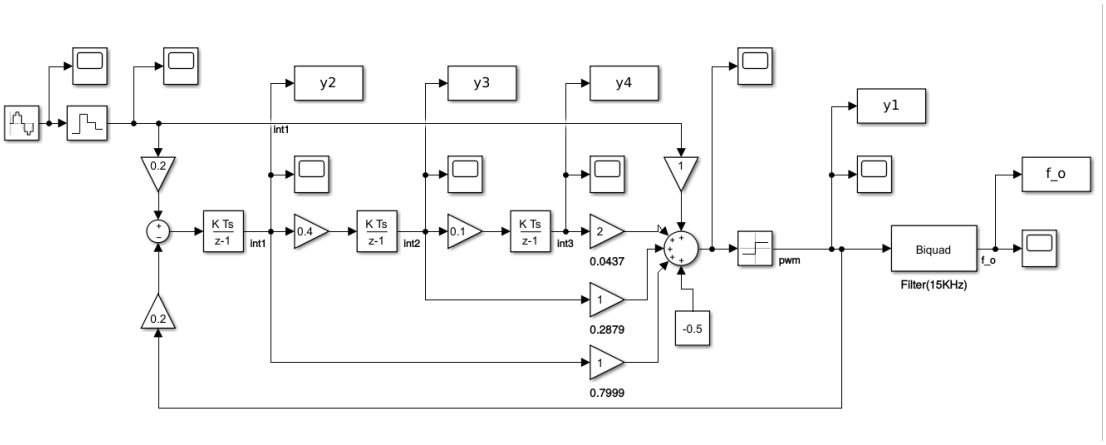

Figure A.2: Simulink model of DSM

The model takes the following parameters as input for simulating the design.

- N - number of FFT points
- fs - sampling frequency
- OSR - oversampling rate
- fin - frequency of input sinusoidal signal
- amp - amplitude of input sinusoidal signal

For more information on setting up the model and simulating the model, watch demo video (File name: Simulink_demo.mp4) available on CD that is attached with the thesis.

A-3 MATLAB psuedo code: Computing the performance metrics (from a time domain signal)

In this section, MATLAB code for finding the performance metrics of DSM/CDA is presented. SNR, SNDR, SFDR, THD, HD3 can be computed using this code. Hann windowing is used for DFT computation. DFT is computed using the code given in Schreier et al. (2005).

Following are the input data needed for the code for computing the performance metrics.

- N - No. of FFT points
- fs - Sampling frequency
- fbin - input frequency bin; used for calculating the input frequency accurately.
- bw - input signal bandwidth
- OSR - oversampling rate
- time domain signal has to stored into y1 variable.

```
========================================================================
                                CODE
========================================================================
% Input specs
N=65536;
fs=5.12e6;
fbin=13;
bw=20e3;
OSR = 128;

% Setting-up the window
w=hann(N,'periodic');
```

```
w1=norm(w,1);
w2=norm(w,2);
NBW = (w2/w1)^2;
nb=3;

% Figuring out the input signal bins, in-band bins, noise bins
fin=(fbin*fs/N);
signal_bins = fbin + [-(nb-1)/2:(nb-1)/2];
dc_bin = 0:1;
inband_bins = 0:N/(2*OSR);
noise_bins = setdiff(setdiff(inband_bins,signal_bins),dc_bin);

% Finding FFT
pwm = y1(length(y1)-N+1:length(y1));
V = fft(w.*pwm)/(w1/2);

% Computing the performance metrics
if 3*fbin < length(inband_bins)
harmonics = (2.*[1:floor(bw/(2*fin))]+1).*fbin;
harm_bins = [harmonics, harmonics-1, harmonics+1];
harm3  = 3*fbin + [-(nb-1)/2:(nb-1)/2];
sndr = dbp(sum(abs(V(signal_bins+1)).^2)/sum(abs(V(noise_bins+1)).^2));
thd = dbp(sum(abs(V(signal_bins+1)).^2)/sum(abs(V(harm_bins+1)).^2));
snr = dbp(sum(abs(V(signal_bins+1)).^2)/(sum(abs(V(noise_bins+1)).^2)
      -sum(abs(V(harm_bins+1)).^2)));
sfdr = dbv(abs(V(fbin+1))/max(abs(V(noise_bins+1))));
hd3 = dbp(sum(abs(V(signal_bins+1))).^2/sum(abs(V(harm3+1))).^2);
else
```

```
harmonics = [];
harm_bins = [];
sndr = dbp(sum(abs(V(signal_bins+1)).^2)/sum(abs(V(noise_bins+1)).^2));
snr = dbp(sum(abs(V(signal_bins+1)).^2)/(sum(abs(V(noise_bins+1)).^2)
      -sum(abs(V(harm_bins+1)).^2)));
sfdr = dbv(abs(V(fbin+1))/max(abs(V(noise_bins+1))));
end
==========================================================================
```

A-4 MATLAB psuedo code: Plotting the output PSD of DSM/CDA using DSM Toolbox

Once the FFT is computed and made available in variable 'V', following code can be used to plot the PSD (taken from Schreier et al. (2005)).

```
============================================
                    CODE
============================================
figure(1); clf;
semilogx([1:N/2]/N,dbv(V(2:N/2+1)));
figureMagic([2/N 0.5],[],[], [-140 0],10,2);
============================================
```

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Publications based on the thesis

This research work has resulted in the following publications:

Conference:

Yajunath Kaliyath and **Tonse Laxminidhi**, A 1.8 V 11.02 μW Single-Ended Inverter-Based OTA with 113.62 dB Gain, *in Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER)*, IEEE, 2016, 237-241.

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Yajunath Kaliyath and **Tonse Laxminidhi**, A 1.8 V 8.62 μW Inverter-based Gain-boosted OTA with 109.3 dB dc Gain for SC Circuits, *IETE Journal of Research*, Taylor & Francis, 2018. https://doi.org/10.1080/03772063.2018.1464968

Yajunath Kaliyath and **Tonse Laxminidhi**, A 90 dB DR, 102 dB SFDR Discrete-time Delta Sigma Modulator for Audio Applications Using a High Gain Inverter-based OTA, *IET Circuits Devices & Systems* (Communicated)

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