INVESTIGATIONS ON HIGH-FREQUENCY TRANSFORMER ISOLATED CLL RESONANT DC-DC POWER CONVERTER FOR RENEWABLE ENERGY APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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D E C L A R A T I O N

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled **"Investigations on High-Frequency Transformer Isolated CLL Resonant DC-DC Power Converter for Renewable Energy Applications"** which is being submitted to the **National Institute of Technology Karnataka, Surathkal** in partial fulfilment of the requirements for the award of the Degree of **Doctor of Philosophy** in Department of Electrical and Electronics Engineering is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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C E R T I F I C A T E

This is to certify that the Research Thesis entitled **"Investigations on High-Frequency Transformer Isolated CLL Resonant DC-DC Power Converter for Renewable Energy Applications"** submitted by **UDAY PATIL** (Register Number, 158035-EE15F09) as the record of the research work carried out by him, is *accepted as the Research Thesis submission* in partial fulfilment of the requirements for the award of degree of **Doctor of Philosophy.**

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ABSTRACT

Renewable energy sources have been the most promising substitute for conventional energy sources and are employed worldwide due to their cleanliness and sustainability. The power generated by using renewable energy sources is highly fluctuating as it depends on the environmental conditions and other operating conditions. A power conditioning unit comprising of DC-DC converter is required to convert this fluctuating power into a usable constant power. There is an increase in the demand of DC-DC power converters with compact size, higher power density and higher conversion efficiency for the applications involving wide variations in input voltage and load. These converters are also used in applications where electrical isolation is required. The intent of this research is in finding a suitable soft-switching DC-DC power converter topology and investigating on its performance for the applications in renewable energy generation.

In this dissertation, literature review on various resonant power converter topologies and gating control scheme is carried out. The full bridge CLL resonant converter topology and fixed frequency gating scheme are chosen for the study. Three different converter topologies with suitable gating scheme were proposed and examined in detail. The first converter presented is a high-frequency transformer isolated CLL resonant DC-DC power converter operated with phase-shift gating scheme and modified PWM gating scheme. Modeling, analysis, design, simulation and experimental results of the converter are presented. Theoretical and experimental results are compared and performance of the converter when operated with both the gating schemes is analysed.

A high-frequency isolated full bridge zero-voltage-transition (ZVT) CLL resonant DC-DC converter operated with a modified PWM gating scheme has been

proposed. Various modes of operation of the converter are described using typical operating waveforms and equivalent circuit diagrams. Analysis, design, simulation and experimental results are presented and discussed. The proposed converter is able to provide ZVS for all the inverter switches for entire variations in input voltage and loading conditions.

A three-phase interleaved full bridge CLL resonant DC-DC converter with fixed frequency modified PWM gating control has been proposed for medium to high power applications. Modeling and analysis of the converter is presented and the design procedure using a design example is explained. The designed converter is simulated using PSIM software to predict the performance of the converter for variations in input voltage and load conditions. The converter operates in ZVS for all the inverter switches with minimum input voltage and only one switch loses ZVS in each bridge/module for higher input voltages.

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Chapter 1

INTRODUCTION

The dissertation presents investigations on high-frequency transformer isolated full bridge CLL resonant DC-DC power converter topologies for renewable energy applications. The research findings described in this dissertation contribute to select a suitable, compact and efficient DC-DC soft-switching converter topology that can be used as a power electronic interface between the utility grid/load and renewable energy sources (e.g., fuel cells and solar energy). Detailed modeling, analysis and design is done for the proposed converter topologies. PSIM simulation is carried out and the experimental prototype is built in the laboratory to substantiate theoretical performance predictions.

The introduction of the chapter is given in Section 1.1. The general characteristics and properties of renewable energy sources such as fuel cells and solar energy are described in Section 1.2 and Section 1.3 of this chapter respectively. Section 1.4 explains DC-DC power conversion. The switching mechanism of the DC-DC converter and the soft-switching techniques are given in Section 1.5. The motivation and objectives of this dissertation are discussed in Sections 1.6 and 1.7, respectively. The outline of the dissertation is given in Section 1.8.

1.1 Introduction

Increase in energy consumption due to the rapid growth in population and industrial expansion has significantly given rise to the environmental issues that must be confronted. There is a huge dependence on many conventional energy sources that are depleting in nature. Power generation using these energy sources leads to increased

greenhouse gas emissions and is hazardous to the environment by creating air pollution. Besides the antagonistic issue of global warming, there is a necessity for a reduction in the burning of fossil fuels to accomplish sufficient air quality. The development of an efficient and environmentally friendly power generation is becoming increasingly significant in today's era. Renewable energy sources are the most attractive substitute for conventional (non-renewable) energy sources which have an adverse consequence on the environment and are exhaustible. Renewable energy sources such as wind, solar, hydro and energy conversion technologies such as fuel cells are potential energy sources for providing efficient, clean and eco-friendly electrical power. Power generation using fuel cells has an additional benefit of providing continuous power in all seasons as long as the fuel continuity is sustained. Wind and solar power are intermittent, as these energy sources are much dependent on climatic conditions. The power electronic interface of the renewable energy sources with the utility grid/load is shown in Fig. 1.1.

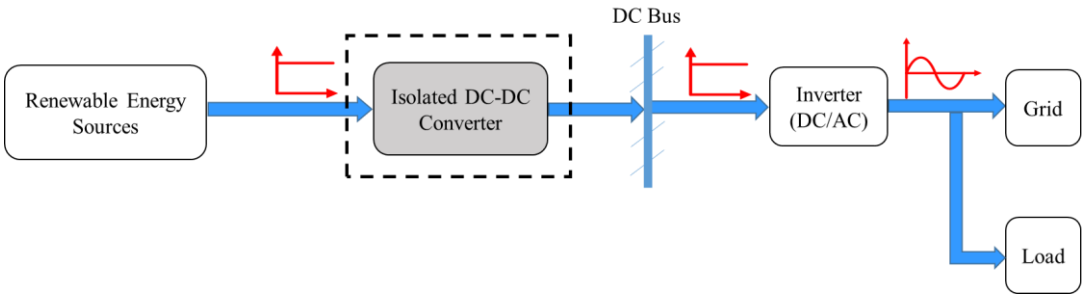


Fig. 1.1: Block diagram of power electronic interface of renewable energy sources with the utility grid/load.

The power generated using renewable energy sources is highly fluctuating due to its dependence on environmental conditions. To convert this varying power into a usable constant power, a power conditioning unit is required. DC-DC converters are one of the important component of this power conditioning unit. The pulse width modulated (PWM) DC-DC converters used for regulating the output voltage suffer from switching losses due to hard-switching. These switching losses increase

significantly with high switching frequency resulting in low efficiency. To overcome this drawback, several resonant DC-DC converter topologies have been proposed in the literature (Arazi et al. 2018; Bhat 1995a, 1997b; Bonde and Tamhane 2018; Ching-Jung Tseng and Chern-Lin Chen 1998; Cho et al. 1994; Chuang et al. 2011a, 2012, 2014; Gautam and Bhat 2013; Johnson and Erickson 1988; Kazimierczuk and Wang 1992; Krishnaswami and Mohan 2009; Lin et al. 2017; Morrison 1992; Oruganti and How 1993; Steigerwald 1988; Wang et al. 2005; Wu et al. 2017a, 2008). The resonant DC-DC converter as shown in Fig.1.2, can withstand the variation in input voltage and load while providing soft-switching features. High-frequency switched full bridge resonant DC-DC converters are extensively used for power applications that have an advantage of reduced size of magnetics and filters.

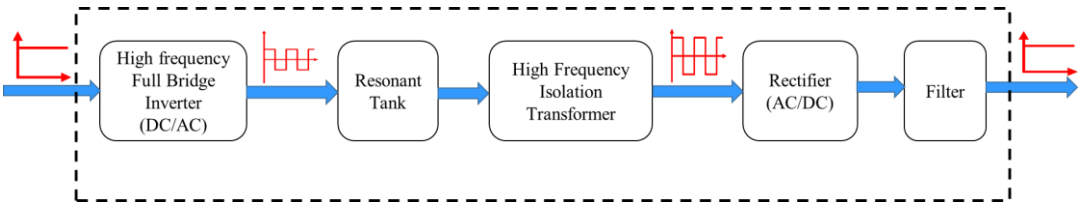


Fig. 1.2: Block diagram of an isolated resonant DC-DC converter.

1.2 Introduction to Fuel Cells

Fuel cells are electrochemical devices that convert chemical energy of a fuel directly into electrical energy and heat by oxidizing hydrogen, resulting in power generation with high efficiency and low environmental impacts. Fuel cells can produce electricity continuously for as long as fuel and oxygen are supplied.

1.2.1 Voltage and Current Characteristics of Fuel Cell

The actual cell potential is decreased from its ideal potential because of several types of irreversible losses such as activation-related losses, ohmic losses, mass transport-related losses. These losses are often referred to as polarization or overvoltage. Of these polarizations, only the ohmic losses actually behave as

resistance. The V-I diagram (Edition and Virginia 2004; Monti et al. 2002; Rathore 2008) generally for low temperature fuel cells with the effects of the three loss categories are illustrated in Fig. 1.3. In the region of activation polarization for a very small increase in current the voltage drops rapidly. These losses depend on the electrocatalyst material and microstructure, chemical reactions and partially on the current density. Voltage decreases linearly with increasing current in the region of ohmic polarization. This region is the normal operating region of fuel cells. Ohmic losses are caused by ionic resistance in the electrodes and electrolyte, electronic resistance in current collectors, electrodes, interconnects and contact resistances. In the region of transportation polarization, voltage starts to collapse rapidly when current exceeds a certain critical value. These losses depend strongly on the reactant activity, electrode and current density. This critical point of the V-I characteristic represents the maximum limit of safe operation for the cell. With the significant losses, the fuel cell may get damaged for a long duration of operation in this region.

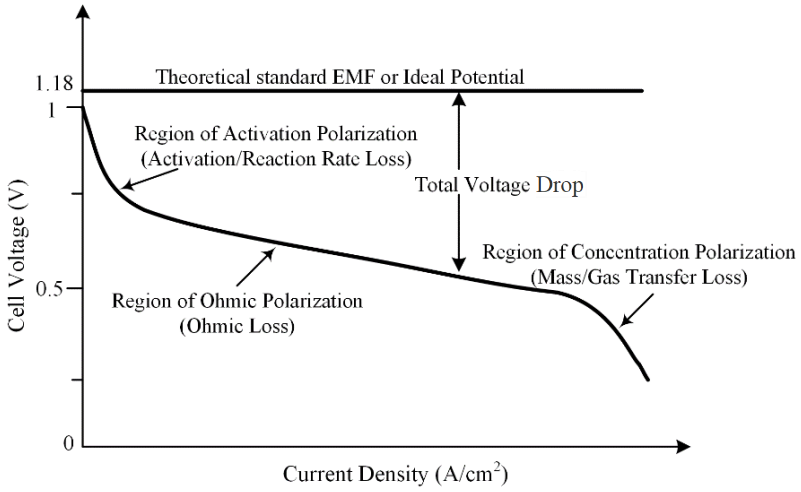


Fig. 1.3: V-I characteristics of the fuel cell.

1.2.2 Voltage and Current Characteristics at Different Rate of Fuel Flow

The fuel cells produce electrical power which is variable as it depends on the pressure of hydrogen and oxygen gases. Fig. 1.4 depicts the voltage-current characteristics of the fuel cell at different rate of fuel flow taken into account (Krein et al. 2004; Rathore 2008). The flow of fuel should be adjusted to give the absolute match for a given electrical load. This causes two problems. The flow rate of fuel cannot be adjusted quickly as the load because the internal chemistry (stoichiometry) must reach equilibrium well before the cell can support change in load. If the electrical load increases too quickly, it could drive the curve over the critical point exceeding maximum power transfer and overheating of the fuel cell stack with extra losses. The dynamics of fuel flow and diffusion of reactants are such that the time constant ranges from several seconds to several minutes for different fuel cell technologies.

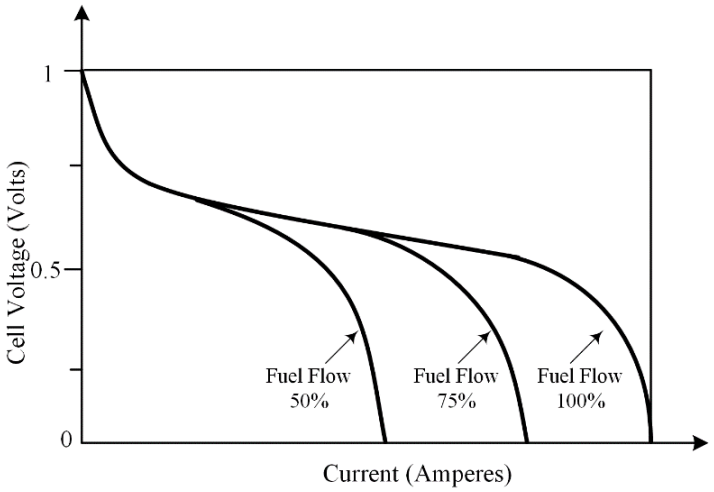


Fig. 1.4: V-I characteristics of the fuel cell at different rates of fuel flow.

1.3 Introduction to Solar Power Generation

Solar energy is one of the most attractive means of renewable power generation. Sizing of the power supply grid plays a significant role in supplying electricity in a distant region at a fair price. Therefore, photovoltaic (PV) systems are an excellent

option for low to medium power levels in remote areas due to the simple scaling of the input power source (Enslin 1990; Singh 2013). The energy conversion efficiency primarily depends on the power-generating PV panels. It is the outcome of numerous efficiencies of the cascaded device, as the energy is transmitted from the sun via the PV system, the regulators, the battery, cabling and an inverter to supply the ac load (Piegari and Rizzo 2010). Weather conditions also influence efficiency, which depends non-linearly on the irradiation level and temperature. The I-V characteristics of a typical PV module for different irradiances (G) at a temperature of 25° C is shown in Fig. 1.5. The PV system power output is proportional to the insolation levels determined in every angular location on the surface of the solar cell. Since solar energy often depends on temperature and panel voltage, maximum power from the solar array needs to be obtained. Various strategies for maximizing output power were suggested and developed (Ali et al. 2020; Bazzi and Krein 2011; Poulek and Libra 2000). Many investigations have been made to modify the solar tracking system to increase the efficiency of the system.

1.3.1 Modeling of Photovoltaic Cell

The semiconductor unit called as a photovoltaic cell is used for the electrical transformation of solar light and the phenomenon is termed as 'Photovoltaic effect'. PV cells are clustered into large units called PV modules, which are attached to form PV arrays. In order to size a solar photovoltaic array, cells are arranged in a series-parallel combination for the required energy (Ko et al. 2018). Depending on the operative conditions and field factors such as the irradiation values, sun's geometric position, and environmental temperature, the electrical power produced by a solar photovoltaic range fluctuates (Ikegami et al. 2001; De Soto et al. 2006). A solar cell is a non-linear device and can be signified as a current source model as depicted in Fig. 1.6. The equivalent circuit of PV cell includes the current source I_{ph} is the PV cell current, I_d is the diode's reverse saturation current, R is the load connected, R_s and R_{sh} are the PV cell's intrinsic series and shunt resistances.

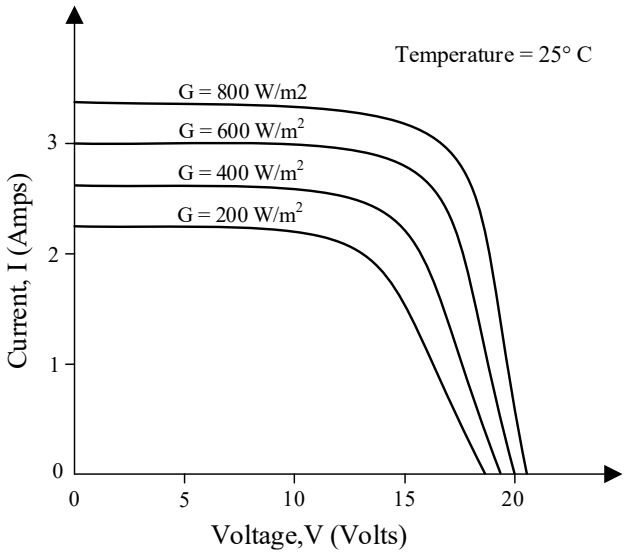


Fig. 1.5: I-V characteristics of a typical PV module.

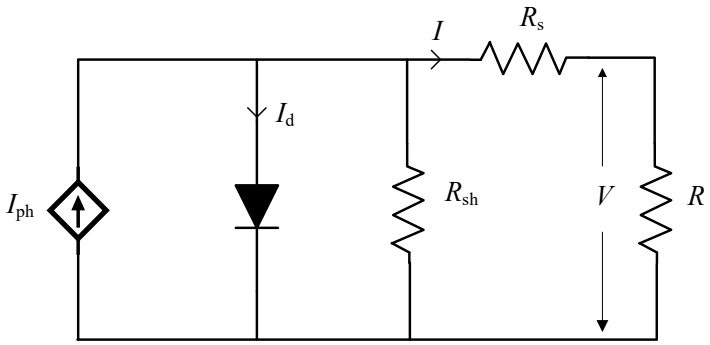


Fig. 1.6: Simplified equivalent circuit of a photovoltaic cell.

The typical I-V characteristics of a PV array is given by the following equation:

$$I = N_p I_{ph} - N_p I_d \left[exp\left(\frac{qV}{kTAN_s} - 1 \right) \right]$$

where, $\boldsymbol{V}$ is the output voltage (V) of the PV array, $\boldsymbol{I}$ is the output current (A) of the PV array, $\boldsymbol{I_d}$ is the reverse saturation current of the cell, $\boldsymbol{q}$ is the charge of an electron (q = 1.60217662 × 10^{-19} C) , $\boldsymbol{N_s}$ is the number of series connected cells, $\boldsymbol{N_p}$ is the number of parallel connected modules, $\boldsymbol{A}$ is the ideality factor of pn junction, $\boldsymbol{k}$ is the boltzmann's constant (k = 1.38064852 × 10^{-23} joule per kelvin), $\boldsymbol{T}$ is the temperature of the cell.

1.4 DC-DC Power Conversion

DC-DC converters are the power electronic circuits which are used in most of the power conditioning systems to convert a dc voltage to a different dc voltage level. DC-DC converters are broadly classified as follows:

1.4.1 Linear Voltage Regulator

The linear voltage regulator is used to convert the dc voltage level to a lower dc voltage level as shown in Fig.1.7. The transistor base current is adjusted accordingly to regulate the output dc voltage over a range of zero to rated output voltage v_d. The variations in line and load are compensated by adjusting base current to regulate the output voltage. The transistor is made to operate in a linear region which acts as a variable resistor to control the output, which results in low efficiency. Linear voltage regulators can handle only low power levels (typically below 20 W) and have very low power density because they require low-frequency (50 or 60 Hz) line transformers and filters which are relatively large and bulky.

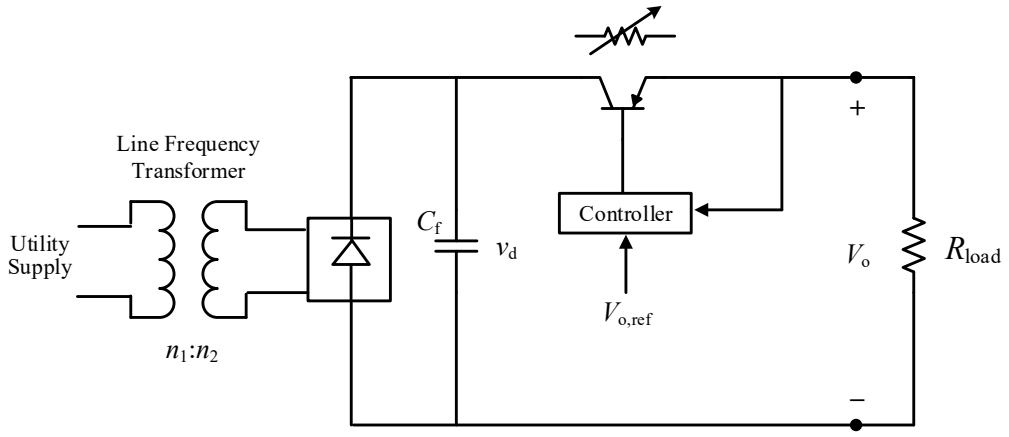


Fig. 1.7: Linear voltage regulator.

1.4.2 Switched Mode Converters

In these converters, pulse width modulation (PWM) is used for the output voltage regulation. The output voltage is controlled by changing the duty ratio of the power semiconductor switches. These converters are hard switched circuits that suffer from high switching losses. It also limits the use of these converters at high-frequency switching because they result in higher switching losses and higher switching stresses. The switching losses increase with the switching frequency which results in low efficiency and difficulty in dissipating the heat from the semiconductor switches. Some of the examples of switched mode DC-DC converters are: buck converter, boost converter, buck-boost converter, cuk converter etc. Switched mode converters with isolation are flyback converter, forward converter, half bridge converter, full bridge converter (see Fig. 1.8) etc.

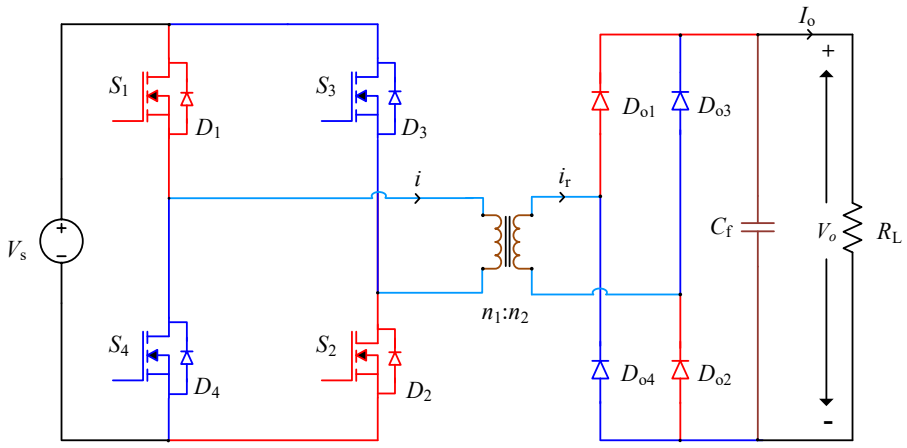


Fig. 1.8: Full bridge switched mode converter.

1.4.3 Soft-Switching Converters

The operation of the switch mode PWM converters exhibits some drawbacks such as higher switching losses and electromagnetic interference (EMI) problems due to hard-switching. These inadequacies become more significant when a high-frequency operation is considered in an effort to increase the power density with the decrease in

the size of magnetics and filters. Hence to overcome these issues, different converter topologies have been developed which offer soft-switching. The soft-switching techniques such as, zero voltage switching (ZVS) (Lin et al. 2008; Pinheiro and Barbi 1993; Safaee et al. 2015; Wu et al. 2008) and zero current switching (ZCS) (Li and Xu 2017; Mousavi and Moschopoulos 2014; Wang et al. 2005; Wang 2005) are used to reduce the switching losses which in-turn increases the efficiency of the converter. One such approach to create these soft-switching techniques is by using resonant converters. The resonant converters are based on an LC resonant tank which creates a high-frequency oscillatory current, making the semiconductor devices to switch with zero voltage or zero current, resulting in low switching losses and stresses. Soft-switching converters constrain the switching of the power semiconductor devices to time intervals when the voltage across the switch or the current through the switch is nearly zero.

1.5 Switching Mechanism

1.5.1 Hard-Switching

Imperfect switching is a major contributor to power loss in the converters. Switching devices absorb power when they are made to turn-on or turn-off when both voltage and current are non-zero. The simultaneous presence of the voltage across the switch and current through it during switching causes a certain amount of power to dissipate within the device. The voltage and current characteristics of hard-switching is shown in Fig. 1.9. The power device has to withstand high voltage and current simultaneously which causes high switching losses and stresses. These losses are very significant for high switching frequency converters which result in low efficiency and thus require large heat sinks. Furthermore, hard-switching creates sharp changes in voltage and current (*dv/dt* and *di/dt*), producing electromagnetic interferences (EMIs).

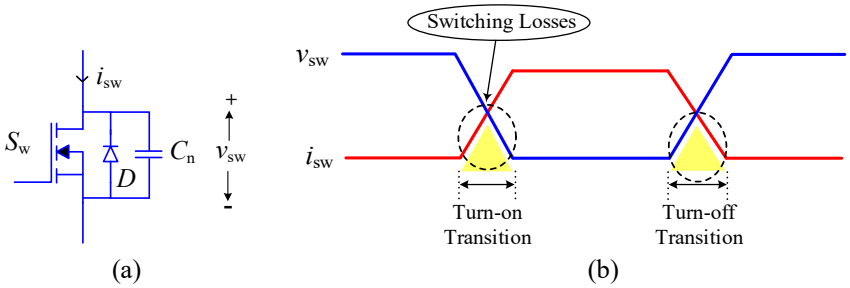


Fig. 1.9: (a) Typical MOSFET device with snubber. (b) Waveforms of switch voltage (v_{sw}) and current (i_{sw}) during hard-switching.

1.5.2 Soft-Switching

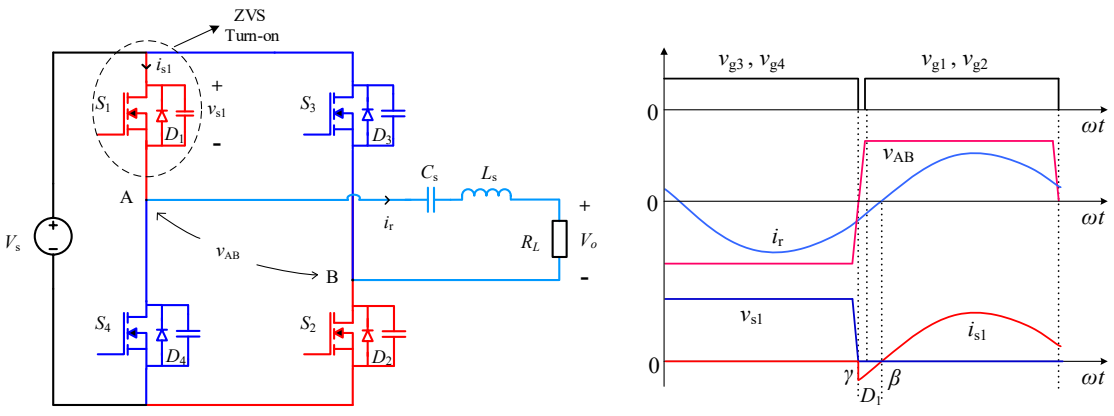
Soft-switching is used to reduce the switching losses in converter. Reduced switching losses result in a smaller size of heat sinks and a notable increase in the efficiency of the converter. The switching power loss is reduced by making either current or voltage zero during the switching transitions. The voltage and current waveforms during soft-switching process are shown in Figs. 1.10-1.11. In earlier days, lossy snubbers or RCD snubbers were usually added to the power circuits so that the switching losses can be reduced to some extent. But with the high switching frequency operation, the switching losses still remain more significant reducing the efficiency of the converter. Hence, to have better efficiency, LC resonant tank circuits are included in the converter to reduce switching losses. The use of LC resonant tank creates oscillatory (usually sinusoidal) current and/or voltage waveforms so that zero voltage switching (ZVS) or zero current switching (ZCS) soft-switching features are created for the switching devices. The operation of the converter at high-frequency reduces the size of magnetics and filter but increases switching power loss; hence soft-switching techniques such as ZVS and ZCS are used to reduce switching losses, electrical stresses and EMIs which in-turn increases the efficiency of the converter. The ZVS and ZCS techniques used for soft-switching are explained in the following sections.

1.5.3 Zero Voltage Switching

The resonant tank circuit is used for most of the converters to accomplish soft-switching features. The resonant tank is a combination of inductors and capacitors

which are used to create an oscillatory current. The voltage across the switch is made to zero during the turn-on instant for obtaining ZVS. To attain ZVS, the converter is to be designed to operate in lagging power factor (PF) mode (above resonance). The resonant current i_r lags the inverter output voltage v_{AB} [see Fig. 1.10(b)]. This can be achieved by selecting the operating switching frequency of the converter above the resonant frequency while designing.

The full bridge resonant converter shown in Fig. 1.10(a) is used to explain the operation of ZVS. The typical waveforms of voltage v_{s1} across the switch S_1 and current i_{s1} through it are shown in Fig. 1.10(b) to describe ZVS operation. When the gating signals v_{gs3} and v_{gs4} are removed and since the resonant current i_r cannot change instantaneously, the direction of the current is maintained through antiparallel diodes D_1 and D_2. It is observed in Fig. 1.10(b) that at the instant $\omega t = \gamma$ the diode D_1 becomes forward biased with the negative current i_r flowing through it. Before the instant $\omega t = \beta$, the switch S_1 is given with a gating pulse v_{gs1}. However, the switch does not turn-on since the antiparallel diode D_1 is still conducting. At $\omega t = \beta$, when the current flowing in the antiparallel diode D_1 becomes zero, since the gating signal for S_1 is already given, the switch S_1 turns on conducting the positive current. Since the antiparallel diode of the switch S_1 was conducting just before the switch conducts, ZVS turn-on of the switch is achieved. Hence, turn-on switching losses are eliminated.



(a) (b)

Fig. 1.10: ZVS mechanism. (a) Full bridge resonant converter (b) Waveforms of voltage across and current through switch S_1.

1.5.4 Zero Current Switching

The full bridge series resonant converter with the resonant tank of inductance L_r and capacitance C_r is shown in Fig 1.11(a). The sinusoidal current is created using the resonant tank of the converter and ZCS of the inverter switches can be achieved. If the current through the switch is zero at the instant of switch turn-off (i.e., removal of gating signal) then it is said to be ZCS. To attain ZCS, the converter is to be designed to operate in leading PF mode (below resonance). The resonant current i_r leads the inverter output voltage v_{AB} [see Fig. 1.11(b)]. This can be achieved by selecting the operating switching frequency of the converter to be below the resonant frequency. The typical waveforms of voltage v_{s1} across the switch S_1 and current i_{s1} through it are shown in Fig. 1.11(b) to describe ZCS operation. At the instant $\omega t = \gamma$, current i_{s1} goes to zero and later tend towards negative forward biasing the antiparallel diode D_1. The diode D_1 conducts with the negative current from the instant γ to β as shown in Fig. 1.11(b) and S_1 is made to turn-off by removing a gating pulse v_{gs1} at this instant($\omega t = \beta > \gamma$) to achieve ZCS. Hence, turn-off switching losses are eliminated.

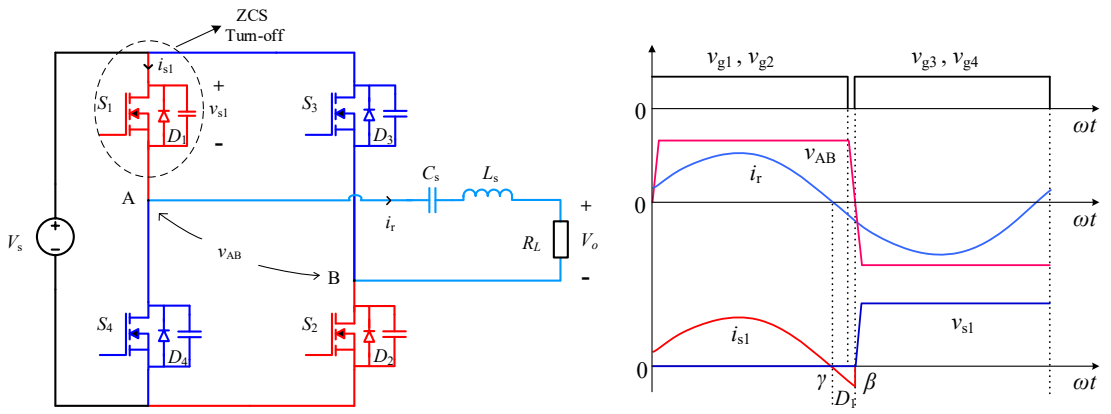


Fig. 1.11: ZCS mechanism. (a) Full bridge resonant converter (b) Waveforms of voltage across and current through switch S_1.

1.6 Motivation for the Work

A power conditioning unit is required to convert the fluctuating power from the renewable energy sources into a constant power. Resonant converters are the most attractive DC-DC converters used in power conditioning unit as they provide low switching losses, stresses and EMIs, resulting in high efficiency. High-frequency operation of the resonant converters results in reduced size and weight of the converter which is advantageous in most of the renewable energy applications. Maintaining soft-switching over the entire operating range of input voltage and load variations in fuel cell based power generation is a challenge due to wide variations in the fuel cell stack voltage which depends on the rate of fuel flow. In today's rapidly growing semiconductor technology, the work done till now on power converters appears limited and requires further work to be done. This necessity has been the motivation for this dissertation to take up the research on high-frequency full bridge resonant converter for applications with wide variation in input voltage and loading conditions.

In the literature, there are number of converter topologies described for the utility interfacing. However, there is limited systematic performance evaluation of the chosen front-end converter topology with the different gating control schemes for the applications involving wide variations in input voltage and loading conditions. This missing part motivated for this dissertation. The full bridge CLL resonant converter gives good performance (Asa et al. 2015; Chakraborty et al. 1999; Tschirhart and Jain 2008) and the investigations done on full bridge CLL resonant DC-DC converters is limited. The CLL resonant converter topology incorporates the advantageous features of both SRC and PRC resulting in; (i) good light load efficiency (ii) better voltage regulation. Hence, high-frequency transformer isolated full bridge CLL resonant network topology is chosen in this study. The high-frequency CLL resonant DC-DC converter with capacitive output filter applied with regular phase-shift and modified PWM gating scheme is proposed and investigations are performed in Chapter 3 of this dissertation. The detailed modeling and the steady-state analysis of the converter is

carried out. The soft-switching of the converter is achieved for wide variations in loading conditions.

Maintaining soft-switching over the entire operating range of variation in input voltage and load is a major challenge for the present application. The converter loses soft-switching feature at higher input voltages. This missing part motivated for the further research and the selected converter has been configured with zero-voltage-transition (ZVT) auxiliary circuit as proposed in Chapter 4 of this dissertation. The proposed converter topology is able to provide soft-switching for an entire range of variations in input voltage and loading conditions. This converter topology can be used for medium power applications.

In the single-phase bridge converters, the power handling capability is limited and if any of the switches of the converter fails, the power transfer is stopped. This missing step motivated for further research. The three-phase interleaved CLL resonant converter with fixed frequency modified PWM gating control is proposed in Chapter 5 of this dissertation. The three identical full bridges along with CLL resonant tank on the primary side of high-frequency (HF) transformer are connected in parallel as interleaved structure.

In generating the power from renewable energy sources, the output voltage is highly fluctuating. The DC-DC converters as a significant part of the power electronic interface play an important role in conditioning power to provide constant output voltage. Compact and high efficient converters maintaining soft-switching for variations in input voltage and load are the necessities required for these renewable energy applications. The research work is directed towards the high-frequency CLL resonant DC-DC power converter operated with fixed frequency control. The proposed converter topologies can be effectively used for the renewable energy applications.

On the basis of motivations discussed, the objectives of the dissertation are set and discussed in the following Section.

1.7 Objectives

Based on the motivations for the work on the chosen research topic, the following objectives are set:

1. To propose a fixed frequency phase-shift and modified PWM gating scheme applied to a high-frequency transformer isolated CLL-type resonant DC-DC power converter for wide variations in input voltage and load and to perform the following.
   a) Mathematical modeling b) Steady state analysis c) Design and, d) Simulations
2. To build the experimental prototype of the converter indicated in objective #1 and verify the performance with theoretical predictions.
3. To propose a zero-voltage-transition (ZVT) circuit to the resonant converter indicated in objective#1 and analyse the performance.
4. To build an experimental prototype of the converter indicated in objective #1 with ZVT circuit and verify the performance with theoretical predictions made in objective #3.
5. To propose an interleaved operation of the converter indicated in objective#1 and analyse the performance through simulations.

The research work is done to accomplish the set objectives and the outcomes are presented in the dissertation. The outline of the dissertation is stated in the next Section.

1.8 Outline of the Dissertation

The research outcome of the set objectives is presented in three chapters [3, 4, and 5] of the dissertation. The description of the layout of the dissertation is as follows:

Chapter 2 describes the literature review on soft-switching resonant converters for renewable energy applications. Various resonant converter topologies are studied and their advantages and disadvantages are defined. The need for ZVT auxiliary circuit in the resonant converter to turn-on the switches with zero voltage switching is discussed. The gating control scheme to regulate the output voltage of the resonant

converters is described. The selection of the resonant converter topology and gating control scheme is explained in detail. The proposed resonant converter should be able to operate with soft-switching for wide variations in input voltage and loading conditions.

In chapter 3, a high-frequency CLL resonant DC-DC converter operated with phase-shift and modified PWM gating scheme is described. Different modes of operation of the converter with both the gating schemes are described and studied in detail. Detailed modeling and the steady-state analysis of the converter is performed by using fundamental harmonic approximation approach. PSIM simulation is carried out and the experimental prototype is built to substantiate theoretical performance predictions. The simulation and experimental outcomes are presented and compared. The converter provides ZVS to all the switches at minimum input voltage for wide variations in load. At maximum input voltage, the converter when applied with phase-shift gating scheme loses ZVS for two switches whereas the converter when applied with modified PWM gating scheme loses only one switch resulting in better efficiency. Hence, modified PWM gating scheme is more advantageous than normal phase-shift gating scheme for the converter with application of variations in input voltage and loading conditions.

In chapter 4, high-frequency isolated full bridge ZVT CLL resonant DC-DC converter is presented. The CLL resonant converter fed with normal phase-shift gating scheme requires two ZVT auxiliary circuits to assist all the main switches to turn-on with ZVS. The usage of two auxiliary circuits in the converter causes conduction losses and also increases the cost and complexity of the converter. Whereas, the ZVT CLL resonant converter proposed in this chapter, fed with modified PWM gating scheme requires only one ZVT auxiliary circuit to provide ZVS for all the main switches. The ZVT auxiliary circuit helps the switch losing ZVS to turn-on with ZVS which reduces the switching losses in-turn enhances the efficiency of the converter. Various operating modes of the converter with ZVT auxiliary circuit are described in detail with the help of typical operating waveforms and equivalent circuit diagrams. The procedure for

optimum design and typical design curves are described. The PSIM simulation results for various operating conditions are presented. The theoretical and simulation results are validated with the help of an experiment and the results are presented.

Chapter 5 describes the three-phase interleaved CLL resonant converter applied with a fixed frequency modified PWM gating scheme. The interleaved operation of the proposed converter is explained with the key waveforms and detailed modeling and analysis are carried out. The choice of optimum parameters of the converter design is described. The PSIM simulations is carried out to substantiate theoretical predictions of the converter for various operating conditions. The interleaving technique has several advantages such as, the converter can deal with high power level, low output ripple current, reduced stress on the switches, high conversion efficiency and partial load can be supplied in case of a fault in any of the phases of the converter.

Chapter 6 gives a summary of the research contributions of the dissertation with the conclusions and suggestions for future work.

Chapter 2

LITERATURE REVIEW ON SOFT-SWITCHING RESONANT CONVERTERS

For medium (<10 kW) and high-power (10 kW – 100 kW) applications, high-frequency full bridge resonant converters can be widely used to have a compact and efficient converter for power conditioning (Agamy et al. 2016, 2015; Dincan et al. 2019). Introduction to various resonant converter topologies and different gating control schemes is presented in this Chapter.

The organization of this chapter is as follows: Introduction of resonant converters and description of various topologies is given in Section 2.1. The different gating control schemes used to regulate the output voltage of the converter are explained in Section 2.2. The selection of converter topology and gating control scheme for the study is described in Section 2.3. Conclusion is given in Section 2.4.

2.1 Resonant Converters

Increasing demand for saving energy and requirement of reduction in the size of power converters have increased significant research and efforts in developing high power density and high efficiency resonant converters (Bhat 1992; Cho et al. 1994; Chuang et al. 2011b; Ivensky et al. 1999a; Jang and Jovanović 2004; Kazimierczuk and Wang 1992; Oruganti and How 1993; Rajagopalan et al. 1990; Redl et al. 1994; Steigerwald 1988; Wang 2006). The resonant converter topologies are formed by using different combinations of inductors and capacitors. Proper designing of the converter that can make the current through inductor and capacitor to oscillate/resonate will help in attaining soft-switching of the converter switches. Soft-switching process comprises

of zero-voltage switching (ZVS) and/or zero-current switching (ZCS) techniques. These soft-switching techniques avoids simultaneous occurrence of voltage and current thereby the switching losses are eliminated. Hence, use of resonant converters with high-frequency switching operation leads to the following advantages:

- High efficiency
- Reduced size of magnetics and filters
- Low EMIs
- Reduced stresses on the switches
- High power density

The isolated high-frequency (HF) resonant converters are an essential component of power conditioning unit in grid interfacing. The basic structure of the resonant converter includes HF switched inverter, resonant tank, HF transformer, diode rectifier and filter as shown in Fig. 1.2. These converters are used to regulate the output power for variations in input voltage and loading conditions. Various switching strategies are applied to resonant converters to vary the duty ratio for controlling the output voltage along with soft-switching features. The resonant converter topologies are broadly classified in the following Sections:

2.1.1 Series Resonant Converters

The series resonant converter (SRC) (Daneshmand et al. 2017; Daryaei et al. 2019; Ivensky et al. 1999b; Kazimierczuk and Wang 1992; Lu et al. 2008; Sabate and Lee 1991; Safaee et al. 2016; Steigerwald 1988; Wu et al. 2017a) has its resonant tank which is composed of capacitor C_s and inductor L_s connected in series as shown in Fig. 2.1. The advantage of the series resonant converter is that the currents in the power devices decrease as the load decreases. This allows the device conduction losses to decrease as the load decreases, thus maintaining high light-load efficiency. Another advantage of this converter is that the series resonant capacitor C_s on the primary side will act as a dc blocking capacitor.

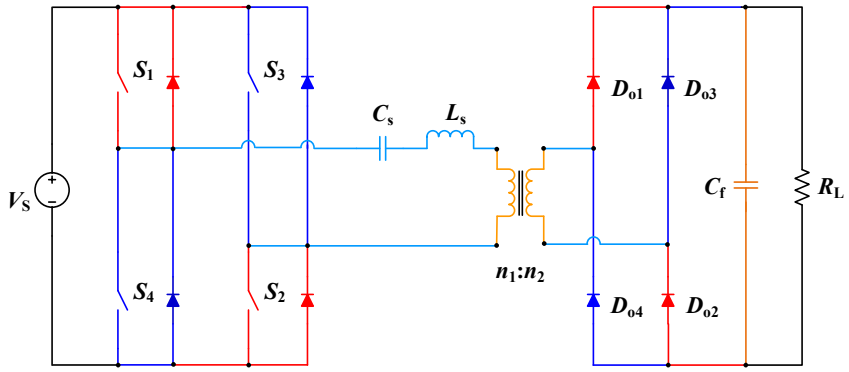


Fig. 2.1: Series resonant converter.

The series-resonant converter has the disadvantage that the output voltage cannot be regulated for the no-load case. The output dc filter capacitor of the converter must carry high ripple current. This is a significant disadvantage for applications with low output voltage and high current (Steigerwald 1988). For this reason, series resonant converter with capacitive filter is considered suitable for high-output-voltage low-output-current applications.

2.1.2 Parallel Resonant Converters

The parallel resonant converter (PRC) (Bonache-Samaniego et al. 2017; Ghahderijani et al. 2017; Haskew and Nelms 1994; Hsu et al. 2017; Johnson and Erickson 1988; Kim et al. 2018; Oruganti and How 1993) includes resonant tank comprising of series connected inductor L_s and parallel connected capacitor C_p as shown in Fig. 2.2. The parallel resonant converter is able to control the output voltage at no-load by varying the switching frequency. The parallel resonant converter is suitable for low-output-voltage high-output-current applications. This is due to the fact that the dc filter on the low-voltage-output side is an inductor that limits the ripple current and therefore output capacitors capable of carrying very high ripple currents are not required.

As the load decreases, the switching frequency increases to regulate the output voltage. But the peak current in the resonant tank circuit in PRC remains relatively constant. As a result of this, the conduction losses in switches and in reactive

components remain constant even during reduced load. Hence, PRC suffers from poor light-load efficiency.

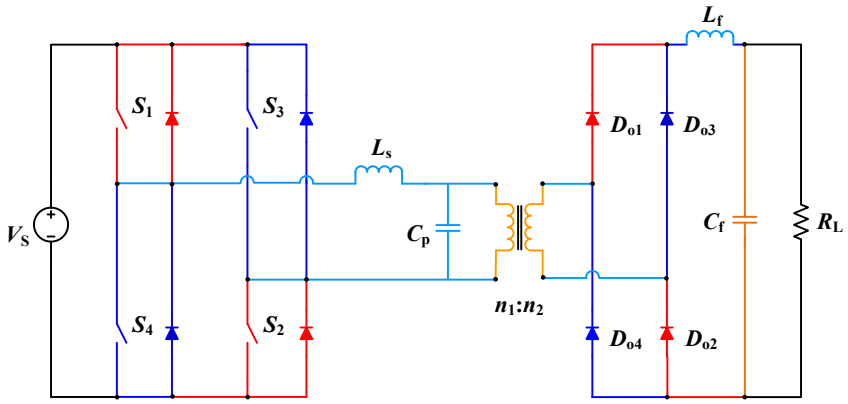


Fig. 2.2: Parallel resonant converter.

2.1.3 Three Element Resonant Converters

The three-element topologies like LCC, LCL, CLL are reported in literature (Asa et al. 2015a; Bhat 1993, 1997a; Borage et al. 2009; Chen et al. 2015; Doradla 1995; Hu et al. 2014a; Selvaperumal and Rajan 2012; Severns 1992; Tan and Ruan 2016). Three element resonant converter topologies effectively use the parasitic components of transformer and switches which increases the performance of the converter. The converters are designed to operate for wide variations in input voltage and loading conditions while providing soft-switching features.

2.1.3.1 Series-Parallel Resonant Converters (LCC Resonant Converter)

The series-parallel resonant converter (Belaguli and Bhat 2000; Bhat 1993; Chen et al. 2006; Chia and Sng 2009; Chuang et al. 2011a; Ivensky et al. 1999a; Morrison 1992; Sosa et al. 2009) shown in Fig. 2.3 utilizes the best characteristics of the series and parallel resonant converter while eliminating their disadvantages of light-load regulation and load independent current in resonant tank respectively. The peak switch current should reduce with the load, decreasing the conduction losses in the

switches to keep the light-load efficiency of the LCC resonant converter high. Hence, it is advantageous to choose the converter components such that the full-load value of Q [$Q = \omega_s.L_s/R_L$] is around 4 or 5. For these values of Q, the converter seems basically as a series resonant converter where the peak current in the resonant circuit will decrease as the load reduces. Further decrease in load will make the LCC resonant converter to resemble the characteristics of parallel resonant converter and henceforth the current in the resonant circuit and switching devices no longer decreases with load. As the LCC resonant converter involves the parallel capacitor, the converter adopts characteristics of parallel resonant converter regulating at no-load conditions.

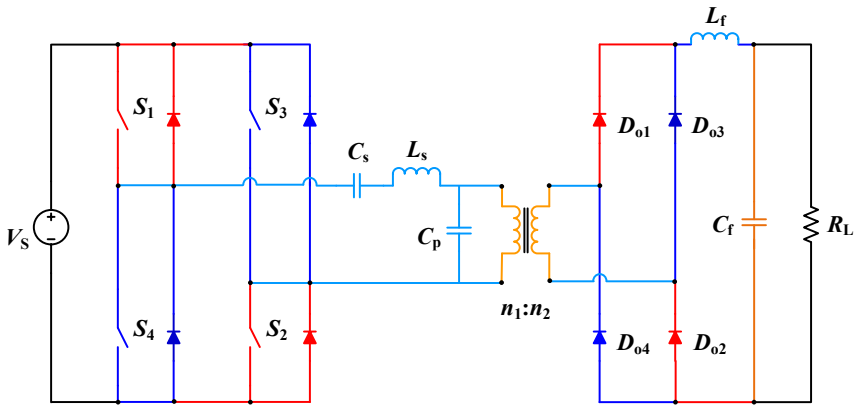


Fig. 2.3: Series-parallel resonant converter.

2.1.3.2 Modified-Series Resonant Converter (LCL-Type Resonant Converter)

The modified-series or LCL-Type resonant converter is shown in Fig. 2.4. In an effort to resolve the issue of voltage regulation of series resonant converter, modified-series (LCL-Type) resonant converters were reported (Beiranvand et al. 2012; Bhat 1995b, 1997a; Doradla 1995; Du and Bhat 2015; Yang et al. 2016). In this topology of the resonant converter, series connected capacitor (C_s) and inductor (L_s) are inter-connected with the parallel inductor (L_p), forming the resonant network as shown in Fig. 2.4. The leakage and magnetizing inductances of high-frequency transformer are profitably used in this converter. As part of the parallel inductor, the magnetizing inductance of the high-frequency transformer may be used and leakage inductance of

high-frequency is considered as a part of the series inductor. To regulate the output voltage of the converter, only a slight variation in switching frequency is required as compared to the series resonant converter for wide variations in load.

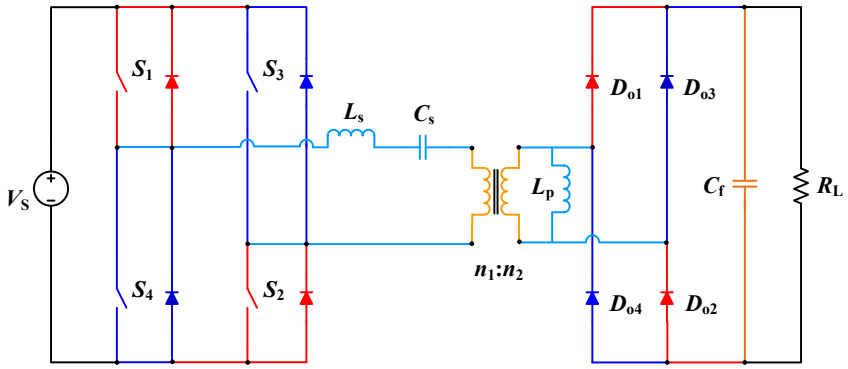


Fig. 2.4: LCL resonant converter.

2.1.3.3 CLL Resonant Converter

The capacitor-inductor-inductor (CLL) resonant converter topology reported in (Asa et al. 2015a; Chakraborty et al. 1999; Chen et al. 2015; Huang et al. 2011; Tschirhart and Jain 2008) is also a three-element resonant converter as shown in Fig. 2.5. The beneficial features of both series resonant converter and parallel resonant converter are integrated in CLL resonant converter. The leakage inductance of the transformer can be beneficially used as a part of series resonant inductance. The regulation of output voltage of the converter from full-load to no-load and good light-load efficiency are the main advantages of CLL resonant converter. These converters are designed to work for wide variations in loading conditions while offering soft-switching capability to the converter switches.

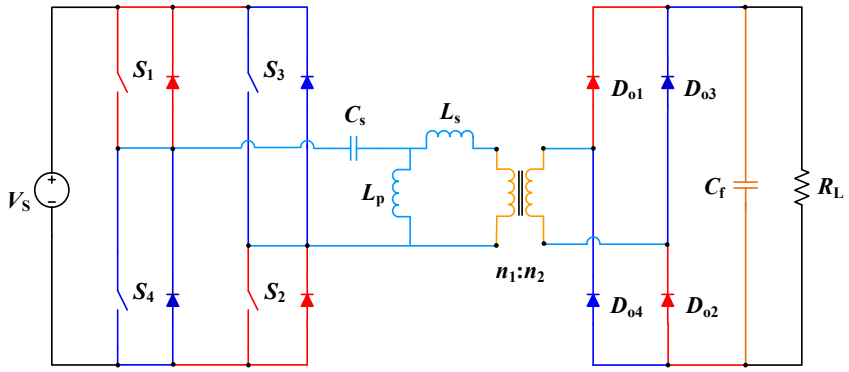


Fig. 2.5: CLL resonant converter.

2.1.4 Zero Voltage Transition Resonant Converter

The resonant converters may lose soft-switching capability of the switches for variations in input voltage and loading conditions. The switch losing ZVS turn-on can be made to operate with ZVS by adding zero-voltage-transition (ZVT) auxiliary circuit (Ching-Jung Tseng and Chern-Lin Chen 1998; Gautam and Bhat 2012; Guichao Hua et al. 1994; Jung-Goo Cho et al. 1998; Martins et al. 2005; Tarzamni et al. 2017; Wang 2006) in the converter. A new family of ZVT PWM converters was described (Guichao Hua et al. 1994); these converters with LC resonant tank operate with soft-switching for entire load and input voltage ranges with minimum current and voltage stresses. The ZVT buck and ZVT boost PWM converters are shown in Fig.2.6. The converter can achieve ZVS of the switch by using ZVT auxiliary circuit connected in parallel with the main switch. The additional ZVT auxiliary circuit consists of an auxiliary switch (S_a), diode (D_a), resonant inductor (L_r) and resonant capacitor (C_r). But the full bridge converter in this family of converters (Guichao Hua et al. 1994) requires two auxiliary switches, two resonant tanks and large losses as the resonant tanks are operated twice in an operating cycle. The full bridge ZVT PWM converter (Cho et al. 1994) although requires only one resonant inductor and operates only for one cycle, but it still requires two auxiliary switches to achieve ZVS for all the main switches which increase the cost and size of the converter. The ZVT converter (Wu et al. 2008) is operated at an extremely high duty ratio to achieve high step-up voltage gain. However, the voltage

gain and the efficiency are limited due to the constraining effect of power switches, diodes, and the equivalent series resistance (ESR) of inductors and capacitors. Moreover, the extremely high duty ratio operation will result in a severe reverse-recovery problem. The ZVS PWM switch cell (Wang 2006) provides ZVS features for different non-isolated DC-DC converters. There is a limit on the voltage gain that can be achieved using a buck-boost or a boost converter. It is not desirable to operate the boost or the buck-boost converter at a very high duty ratio because of very high capacitor current ripple. Thus, the solution is to go for isolated topologies for getting the high voltage gain in between the battery and the DC bus (Bhattacharya et al. 2009). In such topologies, any voltage gain can be achieved by setting the turns ratio of the transformers or the coupled inductors. A full bridge DC-DC PWM converter with auxiliary ZVT circuit given in (Hamdad and Bhat 2001), this series resonant converter lacks voltage regulation at light-load and has low efficiency. During wide variations in input voltage and load conditions, the converters are configured with a ZVT auxiliary circuit to achieve ZVS for all the switches of the converter.

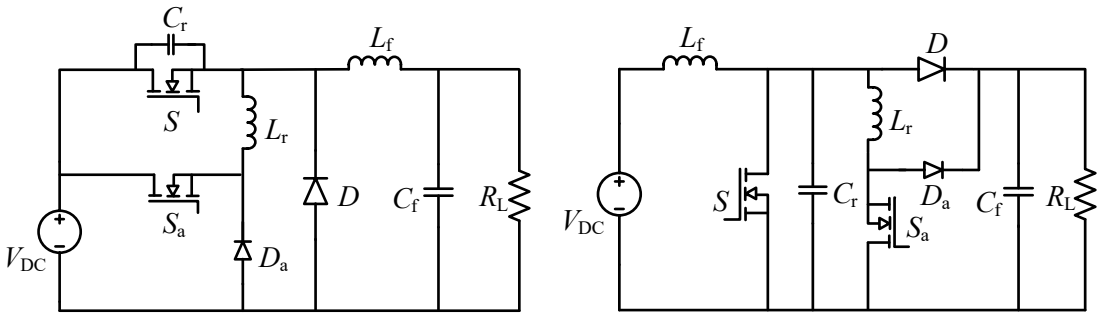


Fig. 2.6: ZVT PWM resonant converters. (a) ZVT buck converter. (b) ZVT boost converter. (Guichao Hua et al. 1994).

2.1.5 Parallel Dual Series Resonant Converter

In high power applications, it is important to maintain the component stress of the converter within certain limits. The conventional resonant converter faces the

drawback of high switch current on the resonant components. In order to overcome this problem, the integration of two resonant conversion units could be a good approach in which power is shared between two resonant networks so that the stresses on the resonant components are minimized.

The parallel connected dual series resonant converter is operated with sinusoidally-modulated fixed frequency phase-shift gating scheme (Rajagopalan et al. 1990; Tahavorgar and Quaicoe 2019; Wu et al. 2018). The converter topology with two half-bridges with dual series resonant network interconnected in parallel on primary side of high-frequency transformer is shown in Fig. 2.7. The output voltage of the converter is controlled by varying the phase-shift between the gating signals given to the switches. The converter is able to offer ZVS to all the switches of the two half bridges. Due to the phase-shift given between the gating signals of half bridge switches, the resonant current in the two resonant network differs making difficulty in the design of heat sink. Furthermore, the peak switch current is exceedingly high even at zero output leading to poor efficiency of the converter. Therefore, interleaved or multiphase converters can be used in high power applications which offer good performance.

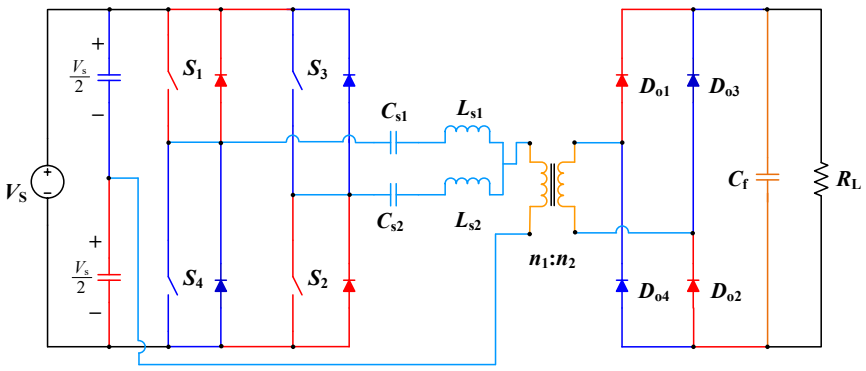


Fig. 2.7: Fixed frequency parallel dual series resonant converter.

2.2 Gating Control Scheme

As the load or input voltage changes, the output voltage is regulated by various switching strategies. For many applications, the voltage should be kept constant to work

reliably. The most commonly used method for regulation of the output voltage is to vary the frequency of gating signals given to the switches of the converter. And the other method is to keep the frequency fixed, while varying the duty ratio of the gating signal or to phase-shift the gating signal given to the gate terminal of the converter switches to control the output voltage.

2.2.1 Variable Frequency Gating Scheme

Conventional converters are regulated by varying switching frequency (Johnson and Erickson 1988; Kazimierczuk and Wang 1992; Severns 1992; Steigerwald 1988) to control the output voltage. The control circuit is used to vary the frequency of pulses given to the switches of the converter as per the requirement of the output voltage to be controlled. However, this variable frequency control produces electromagnetic interference (EMI) and problems associated with the design of filters and magnetics. Also, the effective use of parasitic components of transformers and switches is difficult with variable frequency control (Bhat 1992; Czarkowski and Kazimierczuk 1993; Kazimierczuk and Wang 1992; Redl et al. 1994). Due to these problems, fixed-frequency phase-shift control is chosen against variable frequency control.

Furthermore, the switching frequency during below resonance operation of the two-element resonant converter (i.e., series resonant converter and parallel resonant converter) may go to a very low value at light-loads to regulate the output voltage, which results in increased size of magnetics and filters. Also, the converter may work in discontinuous current mode at lower switching frequencies which causes increased stress on the components of the converter. The switching frequency is increased high to control output voltage at light-loads in the above resonance mode operation of the converter. This high frequency increases copper and core losses in the magnetic parts of the converter.

2.2.2 Fixed Frequency Gating Scheme

A fixed-frequency gating scheme has been used in most of the converters for power control to overcome the issues related to variable frequency control (Czarkowski

and Kazimierczuk 1993; Hamdad and Bhat 2001; Tschirhart and Jain 2008). The power generated by using renewable energy sources is highly fluctuating in nature. Hence, to convert this varying power into a usable constant power, a fixed frequency gating scheme is used for most of the resonant power converters. In this fixed frequency gating scheme, the output voltage can be controlled by pulse width modulation (PWM) gating scheme or phase-shift gating scheme. In, PWM gating scheme the width of the gating signals given to the switches of the converter is varied to regulate the output voltage. Whereas, in phase-shift gating scheme, the gating signals given to the switches is 180 degrees width with fixed frequency. The output voltage is controlled by varying the phase-shift angle between the gating signals given to the switches of the converter. Thus, the pulse-width of the inverter output voltage is varied to regulate the output voltage for changes in input voltage and loading conditions. The fixed frequency phase-shift gating scheme provides ease in designing magnetics and filters of the converter. The disadvantage of this gating scheme is that the converter loses soft-switching capability at light-load conditions and for variations in the input voltage resulting in higher switching losses which in-turn reduces the efficiency of the converter.

2.3 Selection of Converter Topology and Gating Control Scheme

The PWM DC-DC converters used for controlling the output power suffer from higher switching losses due to hard-switching (Bu et al. 1997; Kazimierczuk and Wang 1992; Steigerwald 1988). Converters are operated with high switching frequency to reduce the size of magnetics and filters so that higher power density is achieved. However, the switching losses significantly increase with high switching frequency resulting in low efficiency. Hence, to overcome this disadvantage, high-frequency resonant DC-DC power converter topologies have been developed. Resonant converters can be designed to have soft-switching, which reduces the switching stresses, switching losses and electromagnetic interference (EMI). Since renewable energy generation system has a wide variation in its output voltage, the resonant

converters should be able to maintain soft-switching to achieve high performance for wide variations in load and input voltage of the converter.

The basic two-element resonant DC-DC converter topologies are the series resonant converters (SRCs) and parallel resonant converters (PRCs). The SRC provides good efficiency but the regulation of voltage at the light-load is difficult and is not possible at no-load conditions (Chuang et al. 2009; Glaser et al. 1994; Gonzalez et al. 2001; Ivensky et al. 1999a; Kazimierczuk and Wang 1992; Lee et al. 2014; Steigerwald 1988). However, PRC provides better voltage regulation but suffers from poor efficiency at light-load (Bu et al. 1997; Gautam and Bhat 2013; Gonzalez et al. 2001; Ivensky et al. 1999a; Steigerwald 1988). Hence, to overcome these disadvantages, modified three-element resonant converter topologies i.e., series-parallel (*LCC*) resonant converters, modified-series (*LCL*) resonant converters and capacitor–inductor–inductor (*CLL*) resonant converters were developed. The LCC resonant converters resemble the characteristics of the PRC at light-load conditions depicting the reduction in the efficiency. The improvement in light-load efficiency of the LCC converter is still not sufficient. The LCL and CLL resonant converters provide best performance as compared to others. The investigations done on full bridge CLL resonant converters is limited and hence high-frequency transformer isolated full bridge CLL resonant converter topology is used in this study. The CLL resonant converters overcome the downsides of SRC, PRC and LCC resonant converters and incorporate advantageous features of SRC, PRC, and LCC resonant converters by maintaining high efficiency at light-load conditions and provides good voltage regulation.

Regulation of resonant converters is generally carried by varying switching frequency (Bu et al. 1997; Kazimierczuk and Wang 1992; Steigerwald 1988). But the variable frequency control produces EMI and its problematic to design filters and magnetics. These problems can be overcome by using fixed-frequency control to regulate the output voltage of the resonant converter. While regulating the output voltage of the converter for wide variations in input voltage and loading conditions with fixed frequency gating scheme, the soft-switching features of resonant converters may

be lost. Hence, ZVT auxiliary circuits are used in the converters to make the switches to operate with ZVS. This results in improving the efficiency of the converter.

For medium to high power applications, the conventional single-phase converters are difficult to use as the power rating will be limited and large filter capacitors are required. The parallel dual series resonant converter is used for high power rating as shown in Fig. 2.7, which can reduce stress on the resonant tank elements but the converter gives low performance at light-loads. Hence, the single-phase resonant converters can be connected in parallel to form interleaved or multi-phase resonant converter which can be employed for medium to high power applications. The interleaved resonant power converters possess beneficial features such as low output ripple and higher power handling capacity with good efficiency.

2.4 Conclusion

A literature review on soft-switching resonant power converters used in renewable energy applications is presented. The merits and demerits of various resonant converter topologies are discussed. The gating control schemes to regulate the output voltage of the converter are explained. Based on the motivations and literature review, high-frequency full bridge transformer isolated CLL resonant converter topology and fixed frequency gating scheme are chosen for the study. The resonant converter topologies with fixed frequency gating control scheme for the applications with wide variations in input voltage and loading conditions are proposed in the following three chapters.

Chapter 3

HIGH FREQUENCY CLL RESONANT DC-DC CONVERTER OPERATED WITH PHASE-SHIFT AND MODIFIED PWM GATING SCHEME: ANALYSIS, DESIGN AND IMPLEMENTATION

In this Chapter, a high-frequency full bridge CLL resonant DC-DC converter operated with phase-shift gating scheme (PGS) and modified PWM gating scheme (MGS) is proposed. Detailed modeling and steady-state analysis of the converter is performed by using fundamental harmonic approximation approach. The optimum design of the converter is described with the help of design curves for a sample converter of 200 W rating operated with a switching frequency of 100 kHz. PSIM simulation is carried out and the experimental prototype is built to substantiate theoretical predictions. The performance of the converter when operated with PGS and MGS is studied using PSIM simulations and verified experimentally for variations in input voltage and loading conditions. Also, the performance study of the designed converter under step changes in load is carried out through PSIM simulations. The power-loss breakdown analysis of the designed converter operated with PGS and MGS is performed, and the summary of comparison of results is presented. The converter topology provides highest efficiency when operated with minimum input voltage for all loading conditions as all the inverter switches turn-on with ZVS.

3.1 Introduction

The DC-DC converters are operated with high a switching frequency to reduce the size of magnetics and filters. However, the switching losses and EMI significantly increases with high switching frequency resulting in low efficiency. Hence, to overcome this disadvantage, high-frequency resonant DC-DC converter topologies have been developed which reduces switching losses, electromagnetic interference (EMI) and increase the power density and efficiency of the converter (Bu et al. 1997; Chuang et al. 2009; Glaser et al. 1994; Gonzalez et al. 2001; Kazimierczuk and Wang 1992; Lee et al. 2014).

Regulation of output voltage is difficult in the series resonant converters (SRCs) (Gonzalez et al. 2001; Kazimierczuk and Wang 1992; Steigerwald 1988; Tan and Ruan 2016) at no-load (NL) conditions and the parallel resonant converters (PRCs) given in (Bu et al. 1997; Gonzalez et al. 2001; Steigerwald 1988) suffer from poor light-load efficiency. The CLL resonant DC-DC converters (Asa et al. 2015a; Chakraborty et al. 1999; Chen et al. 2015; Huang et al. 2011; Tan and Ruan 2016) overcome the downsides of SRC, PRC and LCC resonant converters by maintaining high efficiency at light-load conditions and provide good voltage regulation. The CLL resonant tank has an attractive property of inherently adjusting its circulating current while maintaining ZVS (Tschirhart and Jain 2008). This feature of the converter makes it distinctive as compared to other topologies. Variable frequency control (Bhat 1997a; Glaser et al. 1994; Kazimierczuk and Wang 1992) is conventionally applied to the converter for regulation of output voltage but suffers from the point of complexity in designing the magnetics and filters. It is also difficult to effectively use the parasitic components of transformers and switches with variable frequency control. Hence, a fixed-frequency PWM or phase-shift gating scheme (PGS) is preferred to overcome these difficulties. The fixed-frequency PGS (Bhat 1997a; Chuang et al. 2011b; Hua et al. 2016; Koo et al. 2005; Lo et al. 2011; Lu et al. 2008) applied to a resonant converter for the output power control offers zero voltage switching (ZVS) to all the main switches for a wide range of loading conditions. But when the higher input voltage is

applied to the converter, two switches of the full bridge lose ZVS which results in lower efficiency. The fixed-frequency asymmetrical PWM gating scheme (Lin et al. 2017; Mangat et al. 2004; Tschirhart and Jain 2008) is applied to the converter to control the output voltage but this scheme of gating produces higher rms current and turn-off current which increases the losses. Hybrid modulation control strategies based on the combination of frequency modulation and phase-shift modulation have been proposed in (Li et al. 2019, 2018; Wang et al. 2019; Yudi et al. 2018) to have a narrow range of frequency operation. Different hybrid control strategies are analysed and suggested in (Hu et al. 2013; Sun et al. 2017; Vu and Choi 2018) to increase the converter performance. However, these control methods have high turn-off currents for the primary switches and complex control algorithms (Wei et al. 2020). Also, hybrid control strategies involving variable frequency control still suffer from problems such as, poor EMI, low power density, high conduction losses and complex design of magnetics and filters. To further narrow the switching frequency, several topologies based on modifications to the configuration of an LLC converter are proposed (Hu et al. 2013; Sun et al. 2017; Vu and Choi 2018). But these topologies involve additional switches which operates with hard-switching increasing switching losses, cost and complexity of the circuit. The modified PWM gating scheme (MGS) (Bhat and Fei Luo 2003; Hamdad and Bhat 2001; Harischandrappa and Bhat 2014) applied to full bridge resonant DC-DC converter offers ZVS to all the main switches for variations in load with minimum input voltage, and only one switch loses ZVS with maximum input voltage as compared to two switches with PGS (Koo et al. 2005; Lo et al. 2011; Lu et al. 2008). Hence, MGS resulting in better efficiency as compared to PGS without any additional cost. The operation of the converter in lagging power factor (PF) mode has a benefit of attaining ZVS naturally at the turn-on instant of the switches. Hence, the converter is made to achieve ZVS by functioning it in above resonance or lagging PF mode which is attained by keeping the switching frequency more than the resonant frequency of the converter.

The organization of this chapter is as follows: Section 3.2 describes the converter circuit configuration and operational principle with PGS and MGS. Detailed analysis

and modeling of the CLL converter circuit topology are explained in Section 3.3. Section 3.4 illustrates the design procedure using a flowchart, and obtaining the design trade-off in selecting the optimized converter design parameters is explained. Section 3.5 describes the PSIM simulation results. Experimental results are obtained and compared with theoretical results and discussed in Section 3.6. Conclusion is given in Section 3.7.

3.2 Circuit Configuration and Principle of Operation

The full bridge high-frequency CLL resonant DC-DC converter under investigation is depicted in Fig. 3.1. The topology of the circuit comprises of a DC input voltage V_s which represents the power from a renewable energy source followed by HF switched inverter, the resonant tank comprising of capacitor C_s, inductors L_r and L_t, HF isolation transformer, output diode rectifier, capacitive output filter C_f and resistive load R_L. The capacitor C_s is in series with a transformer that blocks the DC component avoiding the core saturation. The converter operated with PGS and MGS with its modes of operation is analysed.

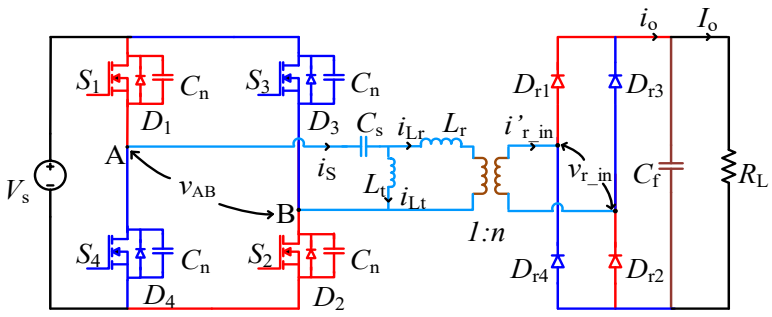


Fig. 3.1: Schematic of high-frequency full bridge CLL resonant DC-DC converter.

3.2.1 Operating Modes with Phase-Shift Gating Scheme

The operation of the converter applied with the PGS is described with the operating waveforms and equivalent circuit diagrams as shown in Figs. 3.2 and 3.3 respectively. The gating pulse to the switches S_2 and S_3 are shifted by an angle β with

respective to the gating signals of the switches S_1 and S_4 as shown in Fig 3.2. The converter output voltage V_o is regulated by varying the value of β. This gating scheme provides two zero voltage intervals in the inverter output square wave voltage v_{AB} in each cycle. The operating modes of the converter when applied with PGS are detailed below:

(i) Mode-I (Operation with minimum input voltage):

When the minimum input voltage is applied, the value of β is smaller and the rectifier input current i_{r_in} is continuous and resonant current i_s lags the inverter output voltage v_{AB} resulting in Mode-I operation of the converter as shown in Fig. 3.2. Here, all the switches operate with ZVS turn-on for wide variations in loading conditions. The equivalent circuits for different operating states of Mode-I are shown in Fig. 3.3.

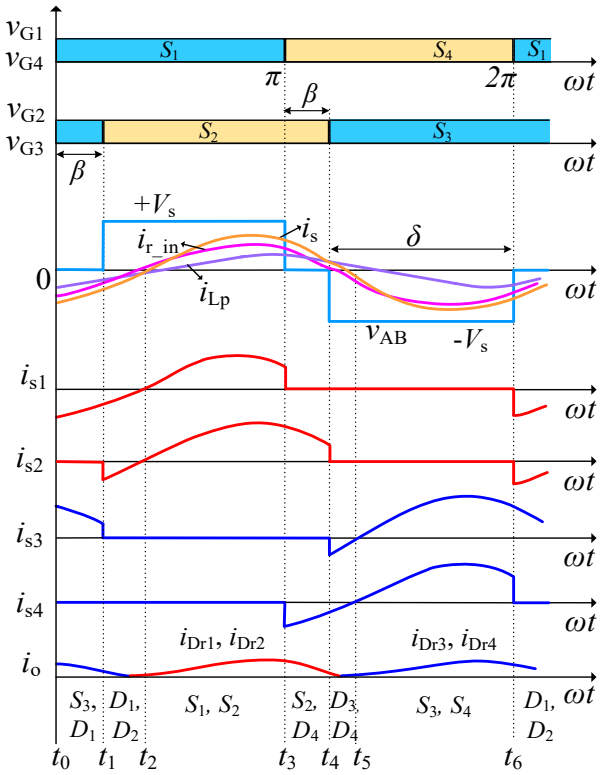


Fig. 3.2: Phase-shift gating scheme and operating waveforms of the converter when applied with minimum input voltage (Mode I).

Different states of operation depending on the devices conducting in Fig. 3.2 are explained in the following:

State I *($t_0 < t < t_1$) [Fig. 3.3(a)]:* In this state, the inductor current continues to follow in the same direction of the previous state ($t_5 - t_6$). The switch S_3 and antiparallel diode D_1 conducts freewheeling the resonant current i_s. The inverter output voltage v_{AB} remains zero during this state. The secondary rectifier diodes D_{r3} and D_{r4} will be conducting supplying the load.

State II *($t_1 < t < t_2$) [Fig. 3.3(b)]:* The gating signal to the switch S_3 is made to turn-off at instant t_1. Now the antiparallel diode D_2 starts conducting with D_1 following the same direction of current i_s. The v_{AB} changes from zero to $+V_s$. The secondary rectifier diodes D_{r3} andD_{r4} stop conducting whereas D_{r1} and D_{r2} start to conduct.

State III *($t_2 < t < t_3$) [Fig. 3.3(c)]:* Now the current i_s changes its direction making the main switches S_1 and S_2 to turn-on and diodes D_1 and D_2 to turn-off. The ZVS turn-on of the switches S_1 and S_2 are achieved as the antiparallel diodes D_1 and D_2 were conducting in prior to the switches S_1 and S_2.

State IV *($t_3 < t < t_4$) [Fig. 3.3(d)]:* The gating signal to the switch S_1 is removed to make it turn-off at instant t_3 and the resonant current is in the same direction, which makes antiparallel diode D_4 to come in conduction with S_2. The v_{AB} changes from '$+V_s$' to zero and the secondary rectifier diodes D_{r1} and D_{r2} remain conducting.

State V *($t_4 < t < t_5$) [Fig. 3.3(e)]:* At the instant t_4, the switch S_3 is made to turn-on by applying the gating signal. As the current direction remains same as the previous state, antiparallel diodes D_3 and D_4 start to conduct connecting with the input dc power supply. The v_{AB} changes from zero to '$-V_s$'. The secondary rectifier diodes D_{r1} and D_{r2} stop conducting whereas D_{r3} and D_{r4} start to conduct.

State VI *($t_5 < t < t_6$) [Fig. 3.3(f)]:* As the direction of the resonant current i_s changes, the switches S_3 and S_4 start conducting. The conduction of the antiparallel diodes D_3

and D_4 before the conduction of switches S_3 and S_4 results in ZVS turn-on of S_3 and S_4. The v_{AB} remains as '-V_s' and secondary rectifier diodes D_{r3} and D_{r4} continue to conduct.

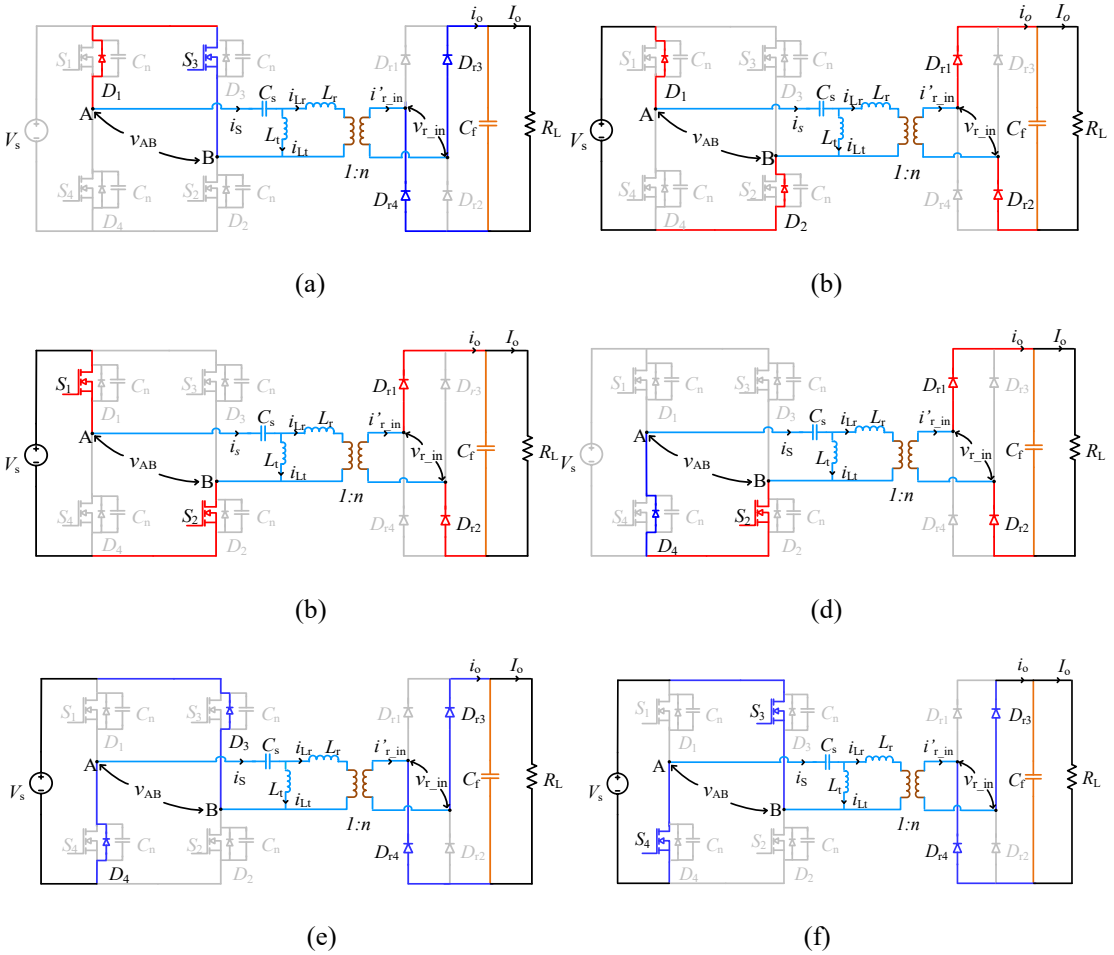


Fig. 3.3: Equivalent circuits for different operating states of Mode-I when operated with PGS. (a) State I. (b) State II. (c) State III. (d) State IV. (e) State V. (f) State VI.

(ii) Mode-II (Operation with maximum input voltage):

The pulse-width 'δ' decreases with an increase in the input voltage and/or at reduced loading conditions. For maximum input voltage, the value of β increases (or δ reduces) which increases zero voltage duration of the inverter output square wave voltage v_{AB}. The current i_s leads the inverter output voltage v_{AB} resulting in Mode II operation of the converter which causes switches S_2 and S_3 to turn-on without ZVS as

shown in Fig. 3.4. The operation of the converter in State II and State V in Mode-I are replaced by State II' and Stage V' of Mode-II respectively and the other states remain the same as in Mode-I.

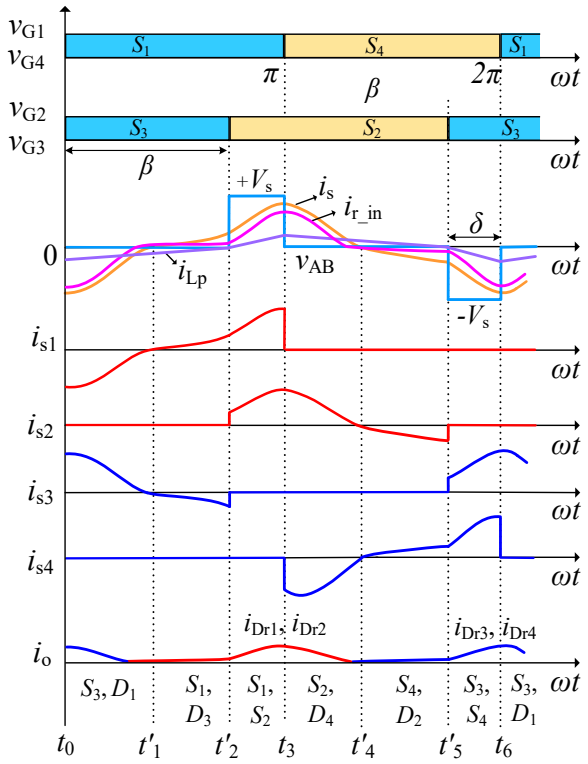


Fig. 3.4: Phase-shift gating scheme and operating waveforms of the converter when applied with maximum input voltage (Mode II).

State II' *($t'_1 < t < t'_2$) [Fig. 3.5(a)]:* The resonant current i_s changes its direction while v_{AB} is still zero at the end of time instant t'_1 resulting in conduction of S_1 and D_3. The current freewheels in the path S_1–resonant tank–D_3. At the end of this state i.e., at instant t'_2, as switch S_2 is given with the gating signal it turns on without ZVS.

State V'$(t'_4 < t < t'_5)$ *[Fig. 3.5(b)]:* In this state, the direction of resonant current i_s changes at the time instant t'_4 making S_4 and D_2 to conduct. At time instant t'_5, as the switch S_3 is given with the gating signal, it turns on without ZVS as there is no antiparallel diode conducting before the switch conducts.

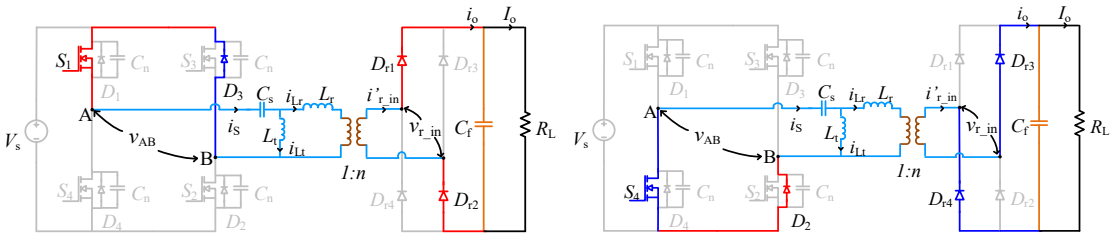


Fig. 3.5: Equivalent circuits for different operating states of Mode-II when operated with PGS. (a) State II'. (b) State V'.

3.2.2 Operating Modes with Modified PWM Gating Scheme

In MGS, the gating pulses of the switches S_2 and S_4 are snipped by an angle β and are added to the switches S_3 and S_1 by the same angle β respectively. The converter output voltage V_o is regulated by varying the value of β. This gating scheme provides only one zero voltage duration in the inverter output square wave voltage v_{AB} in each cycle. The operating waveforms with MGS are shown in Fig. 3.6.

(i) Mode-I (Operation with minimum input voltage):

When the converter is applied with the minimum input voltage, the value of β is smaller and the rectifier input current i_{r_in} is continuous and parallel inductor current i_{Lp} changes its direction, which results in Mode I operation of the converter as given in Fig. 3.6. Each operating state in Mode I is described with the help of equivalent circuits depicted in Fig. 3.7. Here in this Mode-I, all the switches operate with ZVS for varying load conditions.

State I *($t_0 < t < t_1$) [Fig. 3.7(a)]:* In prior to this state, the gating signals for switches S_3 and S_4 are removed which makes them turn-off. The resonant current i_s cannot change instantaneously hence the antiparallel diodes D_1 and D_2 conduct to maintain the same current direction. The input current to the rectifier i_{r_in} is continuous and the v_{AB} changes from $-V_s$ to $+V_s$. The secondary rectifier diodes D_{r3} and D_{r4} stop conducting where D_{r1} and D_{r2} start to conduct.

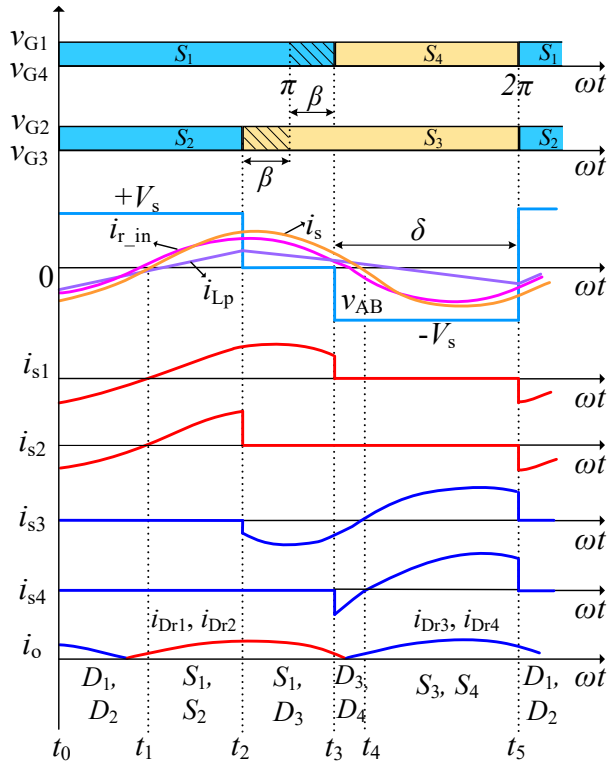


Fig. 3.6: Modified PWM gating scheme and operating waveforms of the converter when applied with minimum input voltage (Mode I).

State II *($t_1 < t < t_2$) [Fig. 3.7(b)]*: The sinusoidal resonant current i_s decreases and the current direction changes making the diodes D_2 and D_1 to turn-off and switches S_2 and S_1 to turn-on. The ZVS turn-on of the switches S_2 and S_1 are achieved as the antiparallel diodes D_2 and D_1 were respectively conducting prior to the switches S_2 and S_1. Voltage v_{AB} remains as $+V_s$ and the output rectifier diodes D_{r1} and D_{r2} conduct.

State III *($t_2 < t < t_3$) [Fig. 3.7(c)]:* In this state, the gating signal to the switch S_2 is removed and makes it turn-off. As the resonant current remains in the same direction, the diode D_3 turns on. The resonant current freewheels in the path S_1– resonant circuit – D_3 making v_{AB} as zero. The stored energy in the tank circuit elements is transmitted to load through rectifier diodes D_{r1} and D_{r2}.

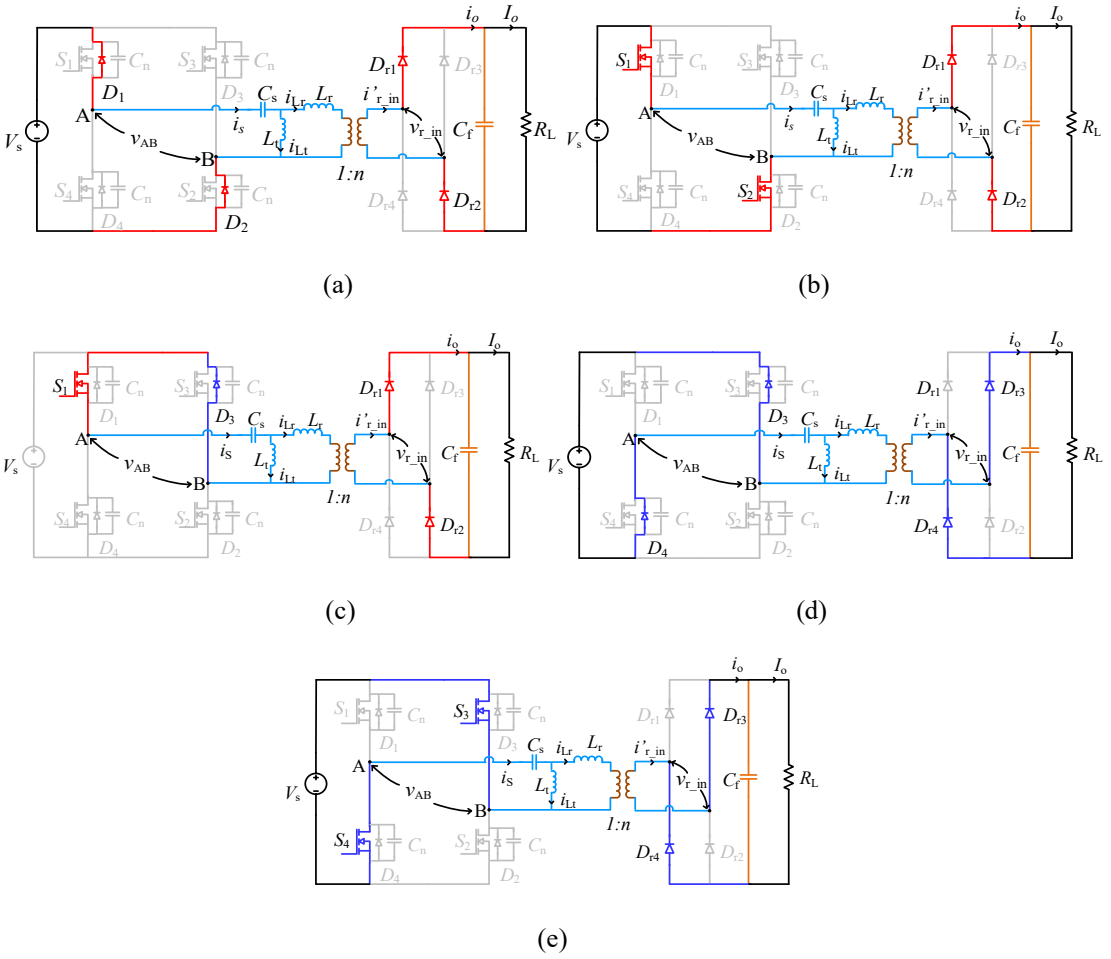


Fig. 3.7: Equivalent circuits for different operating states of Mode I when operated with MGS. (a) State I. (b) State II. (c) State III. (d) State IV. (e) State V.

State IV *($t_3 < t < t_4$) [Fig. 3.7(d)]:* Now the gating signal to S_1 is removed at instant t_3 making it to turn-off. The antiparallel diode D_4 begins to conduct with D_3 to continue the flow of current in a closed path. Voltage v_{AB} changes from zero to $-V_s$. Secondary rectifier diodes D_{r3} and D_{r4} start to conduct to supply power to the load.

State V *($t_4 < t < t_5$) [Fig. 3.7(e)]:* In this stage, the current i_s alters its direction making the switches S_3 and S_4 to turn-on. The antiparallel diodes D_3 and D_4 were conducting before the conduction of the switches S_3 and S_4, resulting in ZVS turn-on of the switches S_3 and S_4. The secondary rectifier diodes D_{r3} and D_{r4} continue to supply power to the load.

(ii) Mode-II (Operation with maximum input voltage):

The pulse-width 'δ' decreases with increases in the input voltage and/or reduced loading conditions. For maximum input voltage, the value of β increases (or δ reduces) which increases zero voltage duration of the inverter output square wave voltage v_{AB}. In this duration, the resonant current freewheels until the stored energy in the resonant circuit gets discharged completely. Further after a certain critical point, the i_{r_in} goes discontinuous and parallel inductor current i_{Lp} stays negative resulting in Mode II operation of the converter which causes switch S_4 to turn-on without ZVS as shown in Fig. 3.8. The operation of the converter in Mode II is same till State III of Mode I and the later stages are as follows:

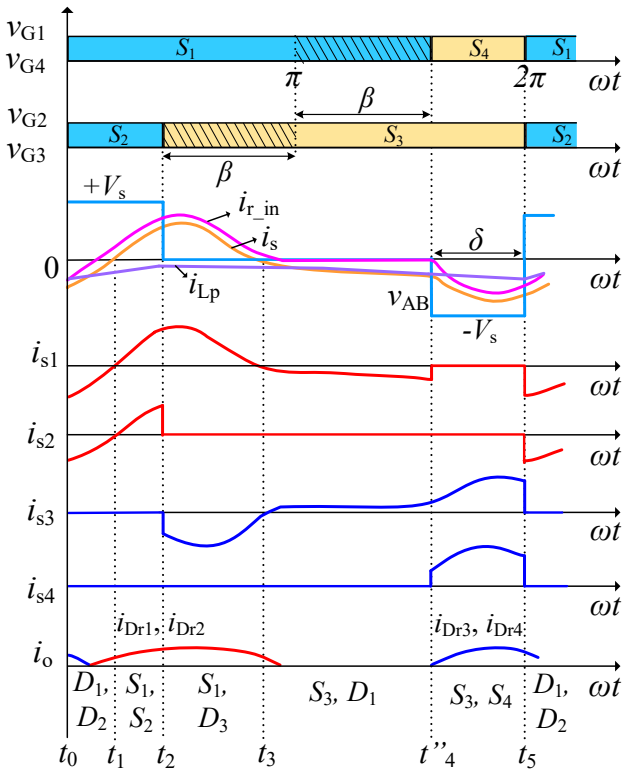


Fig. 3.8: Modified PWM gating scheme and operating waveforms of the converter when applied with maximum input voltage (Mode II).

State IV" *($t_3 < t < t_4$") [Fig. 3.9(a-b)]:* The direction of current i_s alters before the gating pulses are given to switch S_4 and the current freewheels through the path S_3 – resonant circuit – D_1. Secondary rectifier diodes D_{r1} and D_{r2} remain conducting as shown in Fig. 3.9(a). The freewheel of the current continues until the stored energy in the resonant circuit gets completely discharged and further results in a discontinuous current (i_{r_in} = 0). Hence the secondary rectifier diodes as depicted in Fig. 3.9(b) stop conducting. The capacitor filter C_f at the output solitary will be delivering power to the load.

State V" *($t"_4 < t < t_5$) [Fig. 3.7(e)]:* Now the gating pulses are applied to the switch S_4 which turns on conducting current i_s in the same direction as in the previous state *IV"* and v_{AB} goes to negative as '$-V_s$'. As the antiparallel diode D_4 does not conduct before the conduction of the switch S_4 [see Fig. 3.8], the turn-on operation of the switch S_4 is carried out without ZVS as shown in Fig. 3.7(e).

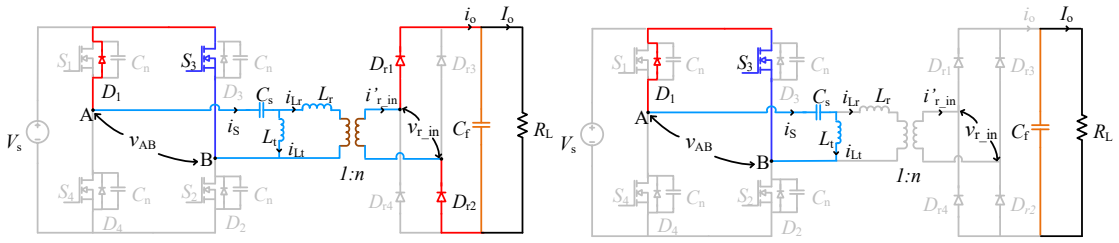


Fig. 3.9: Equivalent circuits for different operating states of Mode II when operated with MGS. (a-b) State IV".

3.3 Modeling and Steady State Analysis of the Converter

The detailed modeling and the steady state analysis of the converter shown in Fig 3.1 is carried out. The fundamental harmonic approximation approach (Bhat 1994) is used for the steady state analysis of the converter.

3.3.1 Assumptions

Some of the assumptions made in the steady-state analysis of the converter are:

i. All the semiconductor switches and diodes are ideal.
ii. The dead time between the gating signal of the two switches is neglected.
iii. The impact of snubbers is not considered.
iv. Only the fundamental components of current and voltage waveforms are considered.

3.3.2 Modeling of the Converter

The circuit diagram of CLL resonant converter with capacitive output filter is shown in Fig. 3.1. An equivalent circuit at the inverter output terminals AB of Fig. 3.1 referred to the primary side is obtained by following the network reduction techniques. As a first step, the HF transformer is represented by its T-equivalent and all the parameters on the secondary side are referred to primary side and the resultant circuit is shown in Fig. 3.10(a).

In Fig. 3.10(a), L_{lp} is the primary leakage inductance, L_{ls} is the secondary leakage inductance and L_m is the magnetizing inductance of the HF transformer. The series inductances L_r and L_{lp} are added to form L_{rlp} (i.e., $L_{rlp} = L_r + L_{lp}$). The circuit is further simplified by using delta to star transformation and the resultant elements are presented in Fig. 3.10(b). The simplified elements of Fig. 3.10(b) are given as:

$$L_a = \frac{L_{rlp} \cdot L_t}{L_t + L_{rlp} + L_m} \tag{3.1}$$

$$L_b = \frac{L_{rlp} \cdot L_m}{L_t + L_{rlp} + L_m} \tag{3.2}$$

$$L_p = \frac{L_m \cdot L_t}{L_t + L_{rlp} + L_m} \tag{3.3}$$

The magnetizing inductance of the transformer is very large compared to the leakage inductances. In equation (3.1), L_m appears only in the denominator which reduces L_a to a very small value. Hence it is neglected to simplify the circuit reduction.

The series connected inductances L_b and L'_{ls} in Fig. 3.10(b) are represented by L_s (i.e., $L_s=L_b+L'_{ls}$) and the simplified equivalent circuit is given in Fig. 3.10(c). An equivalent phasor circuit as shown in Fig. 3.10(d) is obtained by replacing the load, capacitive filter and rectifier block of Fig. 3.10(c) by an equivalent ac resistance R_{ac}. This ac resistance is derived by considering only the fundamental components of rectifier input current i_{r_in} and rectifier input voltage v_{r_in} waveforms shown in Fig. 3.11. The shapes of i_{r_in} and v_{r_in} depend on the type of output filter used.

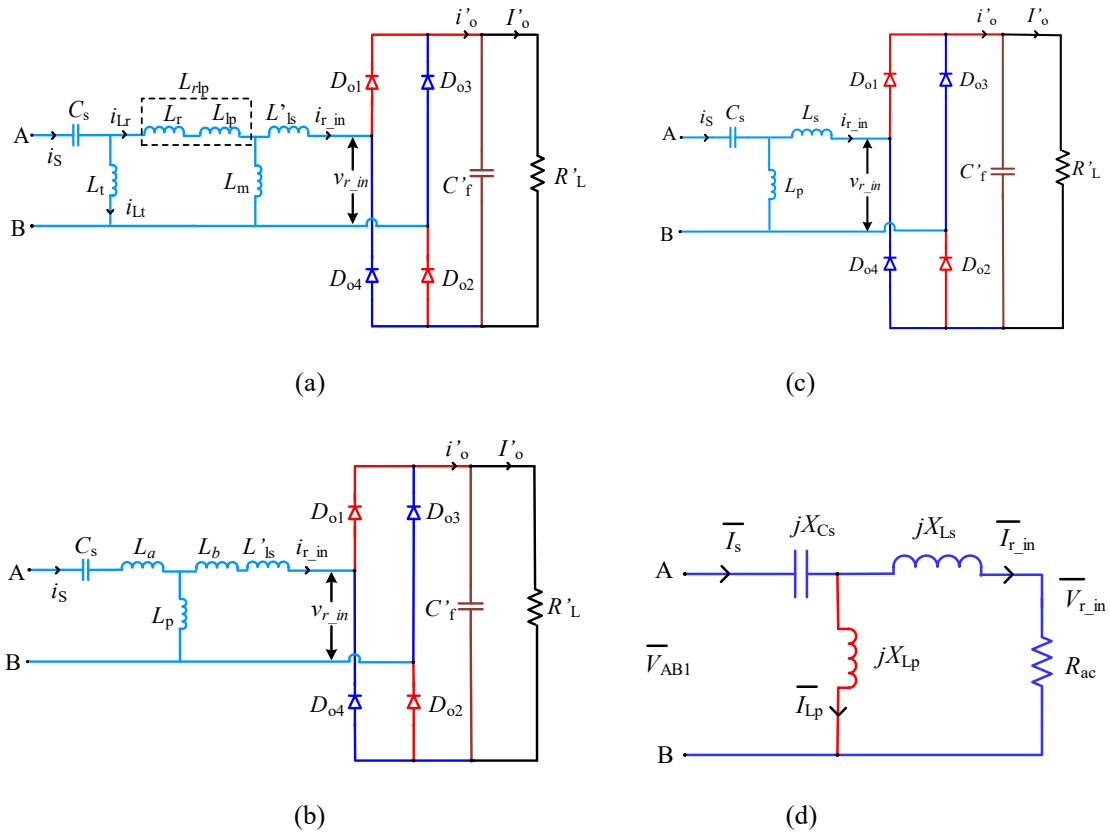


Fig. 3.10: (a) Transformer equivalent circuit of the converter. (b) Incorporating the Δ-Y transformed parameters in the circuit. (c) Simplified circuit of the converter. (d) Equivalent phasor circuit of the converter.

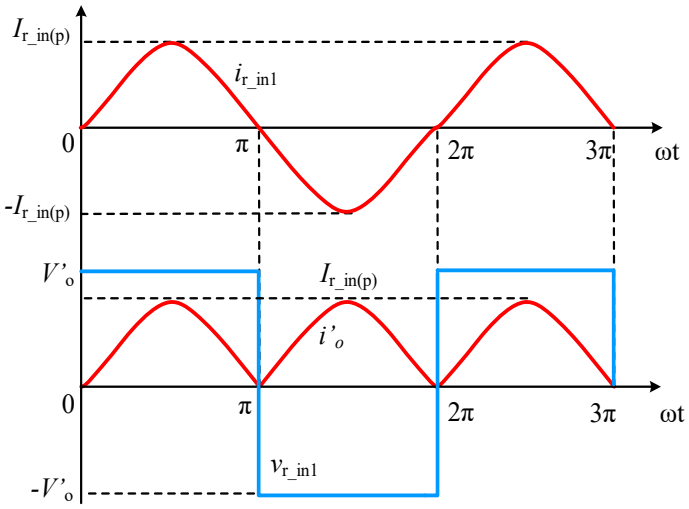


Fig. 3.11: Current and voltage waveforms at the input terminals of the rectifier and current waveform at the output terminal of the rectifier.

3.3.3 Steady State Analysis of the Converter

The root mean square of fundamental elements of the input current to the rectifier (I_{r_in1}) and voltage (approximate square-wave) across the input of the rectifier (V_{r_in1}) are obtained using Fig. 3.11 as,

$$I_{r\_in1} = \left(\frac{\pi}{2\sqrt{2}}\right) I'_o \tag{3.4}$$

$$V_{r\_in1} = \left(\frac{2\sqrt{2}}{\pi}\right) V'_o \tag{3.5}$$

The equivalent AC resistance is derived by (3.4) and (3.5) as,

$$R_{ac} = \frac{V_{r\_in1}}{I_{r\_in1}} = \left(\frac{8}{\pi^2}\right) R'_L \tag{3.6}$$

where, R'_L is the primary side referred load resistance (R_L) of the high-frequency transformer.

The approximate root mean square value of voltage across R_{ac} is,

$$\bar{V}_{r\_in} = \left[2\sqrt{2}/\pi\right]V_0' \tag{3.7}$$

where, V_0' is the primary side referred output voltage.

The RMS of a fundamental element of the inverter output voltage across AB with PGS is obtained as,

$$V_{\mathrm{AB1}} = \frac{2\sqrt{2}}{\pi} V_{\mathrm{s}} \left(sin\frac{\delta}{2}\right) \tag{3.8}$$

The RMS of a fundamental element of the inverter output voltage across AB with MGS is obtained as,

$$V_{\mathrm{AB1}} = \frac{\sqrt{2}}{\pi} V_{\mathrm{s}}(1 - \cos\delta) \tag{3.9}$$

The RMS of a fundamental element of the inverter output voltage across AB for full-load condition ($\delta = \pi$) is same for both the PGS and MGS as,

$$V_{\mathrm{AB1}} = \frac{2\sqrt{2}}{\pi} V_{\mathrm{s}} \tag{3.10}$$

From the equivalent phasor circuit shown in Fig. 3.10(d),

$$\frac{V_{\mathrm{r\_in}}}{V_{\mathrm{AB}}} = \frac{1}{\left(1-\frac{L}{F^2(L+1)}\right)+j\frac{\pi^2}{8}Q\left(F(L+1)-\frac{L}{F}-\frac{1}{F}\right)} \tag{3.11}$$

where,

Inductor ratio, K or $L = (\,L_{\mathrm{s}} \,/\, L_{\mathrm{p}})$,

Frequency ratio, $F = (\,\omega_{\mathrm{s}} \,/\, \omega_{\mathrm{r}})$,

Resonant frequency, $\omega_{\mathrm{r}} = \left(\frac{1}{\sqrt{L_{\mathrm{e}}C_{\mathrm{s}}}}\right)$,

Quality factor, $Q = (\,\omega_{\mathrm{r}}L_{\mathrm{e}}/R'_{\mathrm{L}})$ and

$L_e = (\,L_{\mathrm{s}}.L_{\mathrm{p}}/L_{\mathrm{s}} + L_{\mathrm{p}})$.

L_e is the approximated effective value at full-load condition of the parallel combination of L_s and L_p.

Using (3.6), (3.7), (3.8) and (3.11) the gain of the converter when applied with PGS is derived as,

$$M = \frac{V_0'}{V_s} = \frac{sin(\delta/2)}{\left(1-\frac{L}{F^2(L+1)}\right)+j\frac{\pi^2}{8}Q\left(F(L+1)-\frac{L}{F}-\frac{1}{F}\right)} \tag{3.12}$$

Using (3.6), (3.7), (3.9) and (3.11) the gain of the converter when applied with MGS is derived as,

$$M = \frac{V_0'}{V_s} = \frac{(1-cos\,\delta)/2}{\left(1-\frac{L}{F^2(L+1)}\right)+j\frac{\pi^2}{8}Q\left(F(L+1)-\frac{L}{F}-\frac{1}{F}\right)} \tag{3.13}$$

As the analysis is done considering full-load conditions ($\delta = \pi$) and the converter gain will be same for both PGS and MGS as,

$$M = \frac{1}{\left(1-\frac{L}{F^2(L+1)}\right)+j\frac{\pi^2}{8}Q\left(F(L+1)-\frac{L}{F}-\frac{1}{F}\right)} \tag{3.14}$$

The series resonant inductor,

$$L_s = L_e(L+1) \tag{3.15}$$

The parallel resonant inductor,

$$L_p = L_e(L+1)/L \tag{3.16}$$

Series resonant capacitor,

$$C_s = 1/(\omega^2{}_r.L_e) \tag{3.17}$$

Equivalent circuit impedance across AB of Fig. 3.10(d) is obtained as,

$$Z_{AB} = R_{AB} + jX_{AB} \tag{3.18}$$

The magnitude of the equivalent circuit impedance across AB of Fig. 3.10(d) is given as,

$$|Z_{\mathrm{AB}}| = [R_{\mathrm{AB}}^2 + X_{\mathrm{AB}}^2]^{\frac{1}{2}} \tag{3.19}$$

where,

$$R_{\mathrm{AB}} = \frac{R_{\mathrm{ac}}.\ (\omega_{\mathrm{s}} L_{\mathrm{p}})^2}{R_{\mathrm{ac}}^2 + \left(\omega_{\mathrm{s}} L_{\mathrm{s}} + \omega_{\mathrm{s}} L_{\mathrm{p}}\right)^2} \tag{3.20}$$

$$X_{\mathrm{AB}} = \frac{R_{\mathrm{ac}}^2\left(\omega_{\mathrm{s}} L_{\mathrm{p}} - (1/\omega_{\mathrm{s}} C_{\mathrm{s}})\right) + X_{\mathrm{LP}}^2(\omega_{\mathrm{s}} L_{\mathrm{s}} - (1/\omega_{\mathrm{s}} C_{\mathrm{s}})) + (\omega_{\mathrm{s}} L_{\mathrm{s}})^2\left(\omega_{\mathrm{s}} L_{\mathrm{p}} - (1/\omega_{\mathrm{s}} C_{\mathrm{s}})\right) - 2\omega_{\mathrm{s}} L_{\mathrm{s}}.\omega_{\mathrm{s}} L_{\mathrm{p}}.(1/\omega_{\mathrm{s}} C_{\mathrm{s}})}{R_{\mathrm{ac}}^2 + (\omega_{\mathrm{s}} L_{\mathrm{s}} + \omega_{\mathrm{s}} L_{\mathrm{p}})^2} \tag{3.21}$$

The peak switch current is,

$$I_{\mathrm{sp}} = \frac{V_S}{|Z_{AB}|} \tag{3.22}$$

The switch current is obtained as,

$$i_{\mathrm{S}} = I_{\mathrm{sp}}\,.\sin(\omega t - \phi) \tag{3.23}$$

The initial current through the switch is obtained by substituting $\omega t = (2\pi - \delta)$ in (3.23) as,

$$i_{\mathrm{s0}} = I_{\mathrm{sp}} \sin(2\pi - \delta - \phi) \tag{3.24}$$

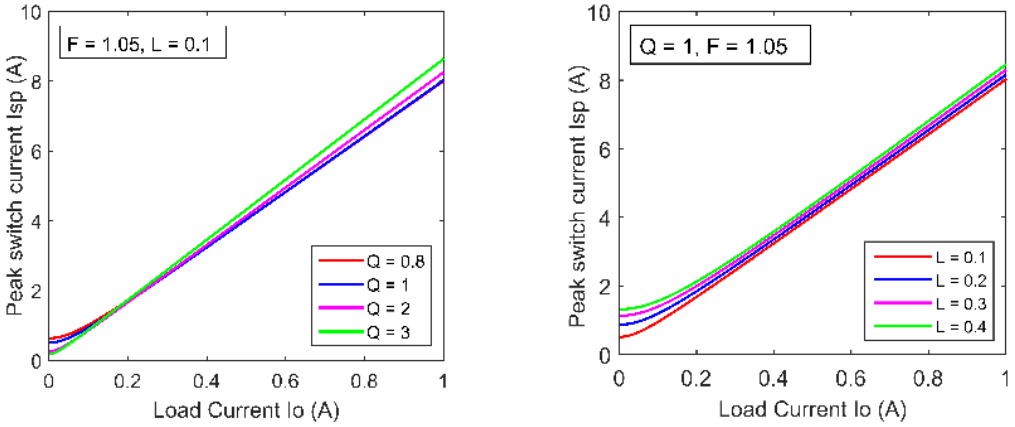
3.4 Design Considerations

The converter design parameters are chosen to their near optimum values by selecting them from the plotted design curves. The selected design parameters enable the converter to be reliable, compact and efficient. The extreme operating condition of full-load and minimum input voltage is considered for designing the converter. The sample design curves shown in Figs. 3.12-3.15 are plotted to choose the optimum

design parameters. The converter is designed to function in lagging power factor mode to attain ZVS for the inverter switches which minimize turn-on losses. This is done by selecting the frequency ratio F greater than 1. The converter is designed to decrease the peak current of the switch I_{sp} with a fall in the load current I_o to uphold good light-load efficiency. From the design curves shown in Fig. 3.12(a), it is observed that the peak switch current I_{sp} reduces with a decrease in Q. However, this reduction in I_{sp} is not very significant for $Q < 1$. Hence $Q = 1$ is favorable. For the same $F = 1.05$ and the selected $Q = 1$, variations of I_{sp} as a function of the inductor ratio L is shown in Fig. 3.12(b). It can be observed that as L increases, the peak current I_{sp} also increases. Also, it can be seen from Fig. 3.13 that for higher inductor ratio L, the kVA/kW rating will be high. Therefore, $L = 0.1$ that gives the lowest I_{sp} is chosen.

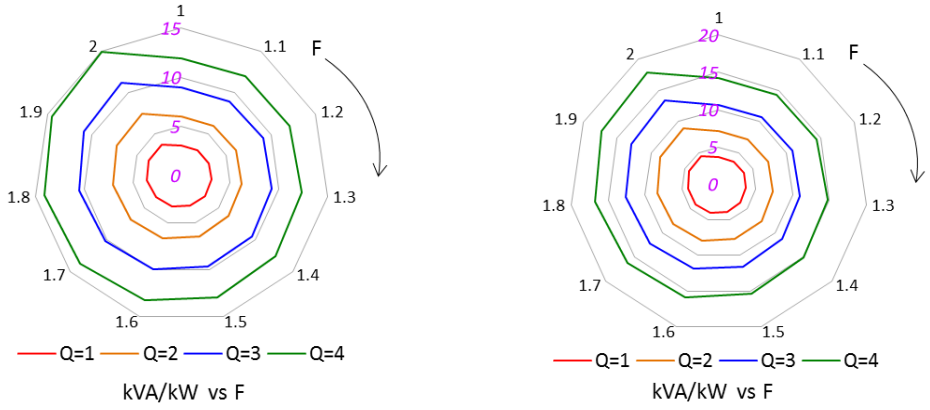
In Fig. 3.13, variations of kVA/kW of the tank circuit is plotted for different values F and Q for two inductor ratios i.e., $L = 0.1$ (see Fig. 3.13(a)) and $L = 0.2$ (see Fig. 3.13(b)). Here, the F varies from 1 to 2 along the circumference and grey color enclosed lines depict the scale for various kVA/kW rating (e.g., 0, 5, 10, 15, 20). The actual area of the colored curves gives the kVA/kW rating for different value of the parameters (i.e., F and Q). It can be observed from these Figs. that, the area (i.e., kVA/kW rating) is smallest for $Q = 1$ and $L = 0.1$. This also supports the justification given above in choosing Q and L. Also, in Fig. 3.13, as F increases from 1 to 2, the kVA/kW rating of the tank circuit increases. It can be inferred from Fig. 3.13(a) that for the chosen values of L and Q, and to operate the converter in above resonance mode, the lowest value of F which gives the lowest kVA/kW rating of the resonant circuit is preferred. Therefore, F is chosen as 1.05. The change in the gain of the converter with variations in F and Q is drawn in Fig. 3.14.

The Fig. 3.15 shows the variation of the initial switch current of all the four switches with the changes in load is obtained using (3.24) when the converter is applied with MGS. The negative sign of the switch current indicates the conduction of antiparallel diode, which results in ZVS of the respective switches. It is observed from Fig. 3.15(a) that, at minimum input voltage all the switches operate with ZVS whereas,



(a) (b)

Fig. 3.12: Variations of peak switch current I_{sp} with the output load current I_o. (a) For $F = 1.05$, $L = 0.1$ and for various values of Q. (b) For $Q = 1$, $F = 1.05$ and for various values of L.



(a) (b)

Fig. 3.13: kVA/kW rating of tank network for variations in F from 1 to 2 for different values of Q. (a) For $L = 0.1$. (b) For $L = 0.2$.

at maximum input voltage only switch S_4 loses ZVS turn-on feature as shown in Fig. 3.15(b). From the design curves presented in Figs. 3.12-3.15, the parameters chosen for the design of the converter are; $Q = 1$, $L = 0.1$ and $F = 1.05$. The procedure for the design of the resonant circuit elements and the high-frequency transformer turns ratio, is illustrated in the flowchart shown in Fig. 3.16. The technical specifications of the converter and the component values obtained are given in Table 3.1. The power loss at various parts of the converter is examined theoretically to know the efficiency of the proposed converter. The power loss distribution in the converter at full-load condition for minimum input voltage is shown in Fig. 3.17(a). It is to be noted that, this power loss remains the same for both PGS and MGS as the pulse-width angle '$\delta = \pi$' is chosen with minimum input voltage. The loss distribution of the converter at full-load condition, when operated with PGS and MGS at maximum input voltage is given in Fig. 3.17(b) and Fig. 3.17(c) respectively.

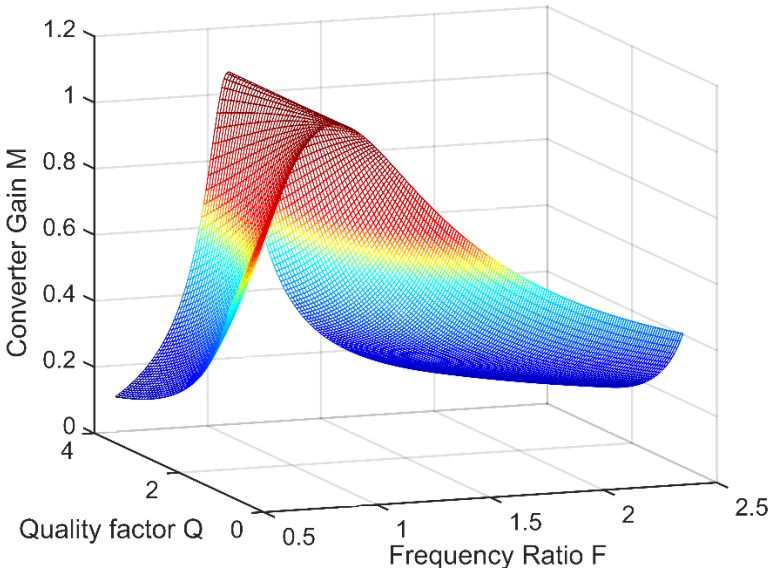
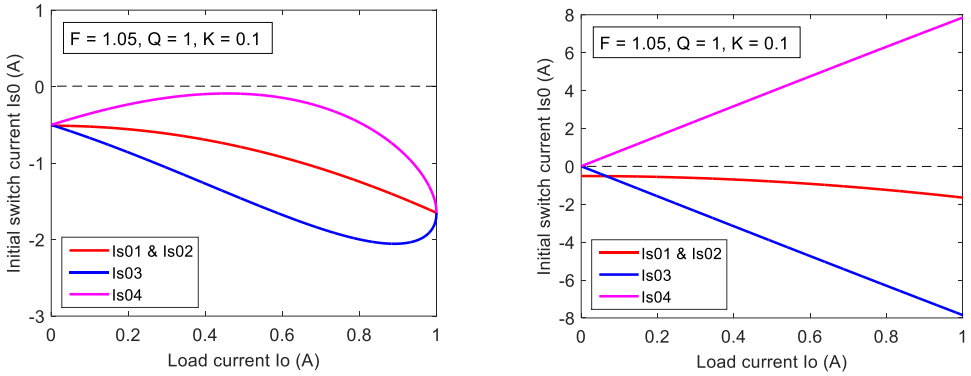


Fig. 3.14: Plot of converter gain (M) with variations in Q and F.



(a) (b)

Fig. 3.15: Variations in initial switch current of switches S_1, S_2, S_3 and S_4 for changes in load current I_o with MGS. (a) For $V_{s(min)}$ = 40 V. (b) For $V_{s(max)}$ = 80 V.

Table 3.1: Converter specifications and component values

Output Power (P_o)	200 W
Output voltage (V_o)	200 V
Input voltage (V_s)	40 – 80 V
Switching frequency (f_s)	100 kHz
Resonant series inductor (L_s)	171.11 µH
Resonant parallel inductor (L_p)	17.11 µH
Resonant capacitor (C_s)	0.1795 µF
Transformer turns ratio ($1:n$)	1 : 4.63
Snubber capacitor (C_n)	1 nF
Output capacitor (C_f)	470 µF

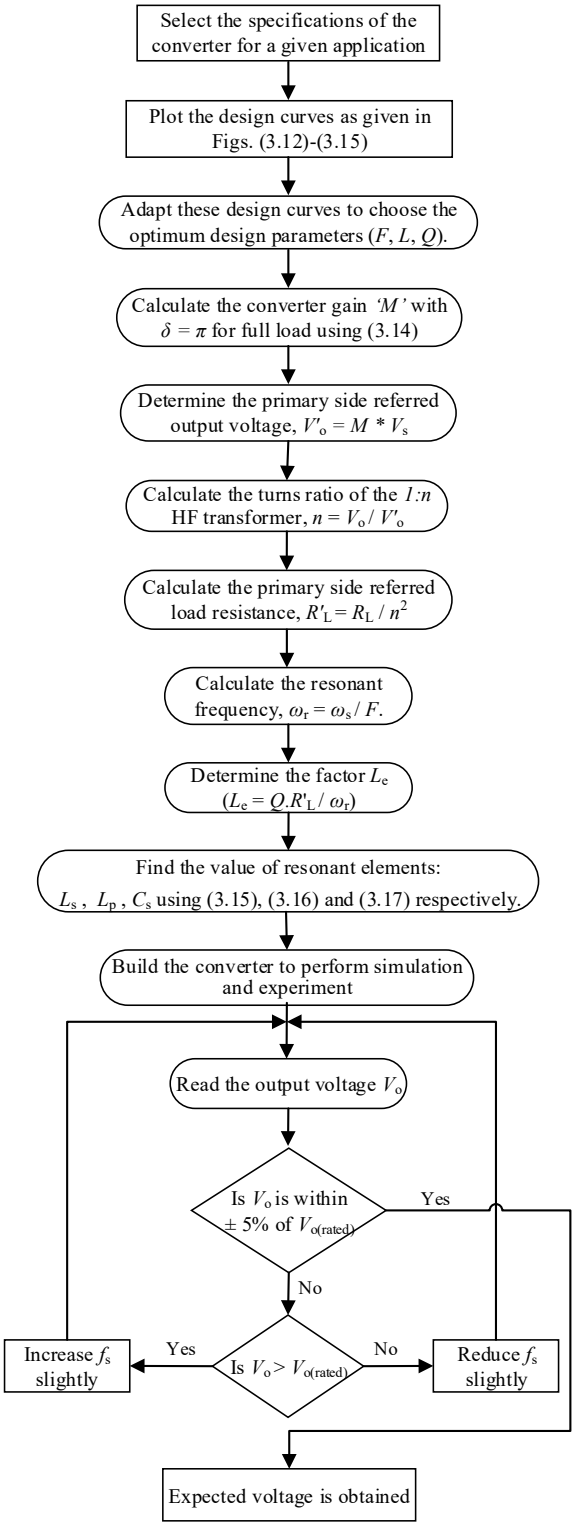
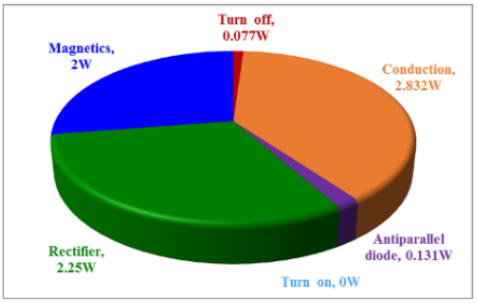
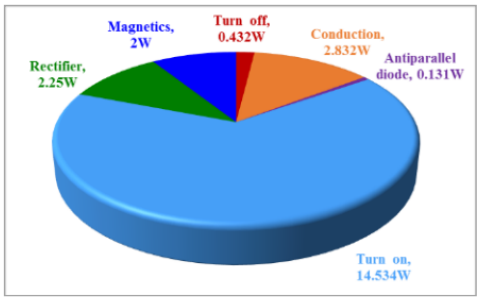


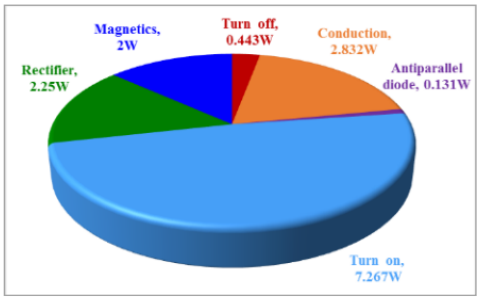
Fig. 3.16: Flowchart for the design procedure of the converter for full-load (δ = π) with minimum input voltage applied.



(a)



(b)



(c)

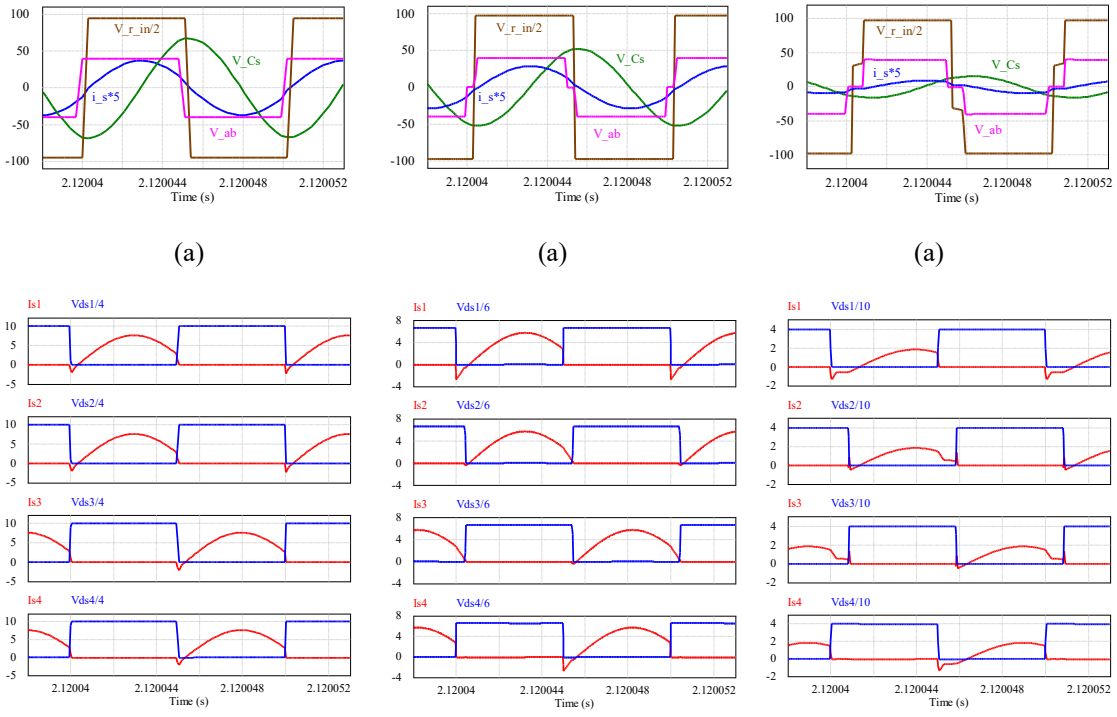
Fig. 3.17: Power loss distribution of the converter at full-load condition. (a) At minimum input voltage operated with PGS/MGS. (b) At maximum input voltage operated with PGS. (c) At maximum input voltage operated with MGS.

3.5 Simulation Results with PGS and MGS

3.5.1 Steady-State Conditions:

The high-frequency CLL resonant DC-DC converter circuit designed in Section 3.4 is simulated to realize its performance using PSIM software. The simulation is carried out with minimum and maximum input voltage for two loading conditions i.e., full-load (FL) and 20% of FL operated with phase-shift gating scheme (PGS) and modified PWM gating scheme (MGS). The results are shown in Figs. 3.18-3.21. The control of the output voltage is carried out by altering the value of pulse-width angle 'δ' for the variations in loading and input voltage conditions. Few iterations are

performed to determine the value of 'δ' required to have the output voltage constant at its full-load value. The ideal transformer and the MOSFETs with $R_{DS(on)}$ = 0.044 Ω are used in the simulation. For the minimum input voltage, the simulation results when operated with PGS and MGS are shown in Fig. 3.18(a) of (i-iii) and Fig. 3.19(a) of (i-iii) respectively. It is noticed from these simulation outcomes that the resonant current i_s lags voltage v_{AB} depicting lagging PF mode of operation and ensuring the ZVS turn-on of the switches. The voltage across and respective current through the switches when applied with PGS and MGS at minimum input voltage shown in Fig. 3.18(b) of (i-iii) and Fig. 3.19(b) of (i-iii) respectively indicates ZVS turn-on of all the switches.



(a) (a) (a)

(b) (b) (b)

(i) Full-Load (ii) 75% of Full-Load (iii) 20% of Full-Load

Fig. 3.18: PSIM simulation results for minimum input voltage $V_{s(min)}$ = 40 V when operated with phase-shift gating scheme for: (i) full-load (ii) 75% of full-load and (iii) 20% of full-load, where, (a) resonant current i_s, inverter output voltage v_{AB}, rectifier input voltage v_{r_in}, resonant capacitor voltage v_{Cs}. (b) voltage across (v_{ds}) and respective current through (i_s) switches $S_1 - S_4$.

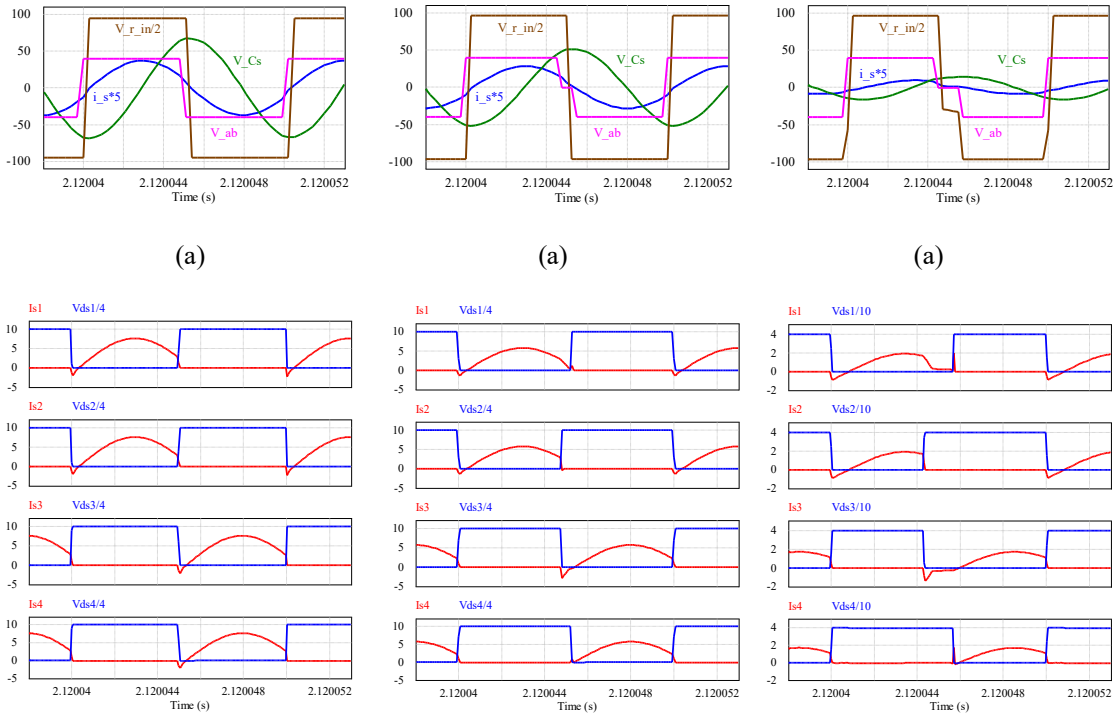


Fig. 3.19: PSIM simulation results for minimum input voltage $V_{s(min)} = 40$ V when operated with modified PWM gating scheme for: (i) full-load, (ii) 75% of full-load and (iii) 20% of full-load, where, (a) resonant current i_s, inverter output voltage v_{AB}, rectifier input voltage v_{r_in}, resonant capacitor voltage v_{Cs}. (b) voltage across (v_{ds}) and respective current through (i_s) switches $S_1 - S_4$.

When the converter is applied with maximum input voltage and operated using PGS, the converter does not function in lagging PF mode which consequences to turn-on of the two switches S_2 and S_3 without ZVS as shown in Fig. 3.20(a) of (i-iii). The voltage across and respective current through the switches indicating turn-on of switches the S_2 and S_3 without ZVS is shown in Fig. 3.20(b) of (i-iii). However, when the converter is applied with maximum input voltage and operated using MGS, only one switch S_4 turn-on without ZVS as shown in Fig. 3.21(a) of (i-iii). The voltage across and respective current through the switches indicating turn-on of only switch S_4 without ZVS is shown in Fig. 3.21(b) of (i-iii). As it is desirable, the peak resonant current

reduces with the load maintaining better light-load efficiency with both the gating schemes. The converter offers ZVS turn-on for all the switches with PGS and MGS for variation in loading conditions when applied with minimum input voltage. At maximum input voltage, PGS makes two switches i.e, S_2 and S_3 to turn-on without ZVS whereas, MGS makes only one switch S_4 to lose ZVS. This helps in minimizing the turn-on losses and hence the efficiency of the converter with MGS is better compared to that with PGS.

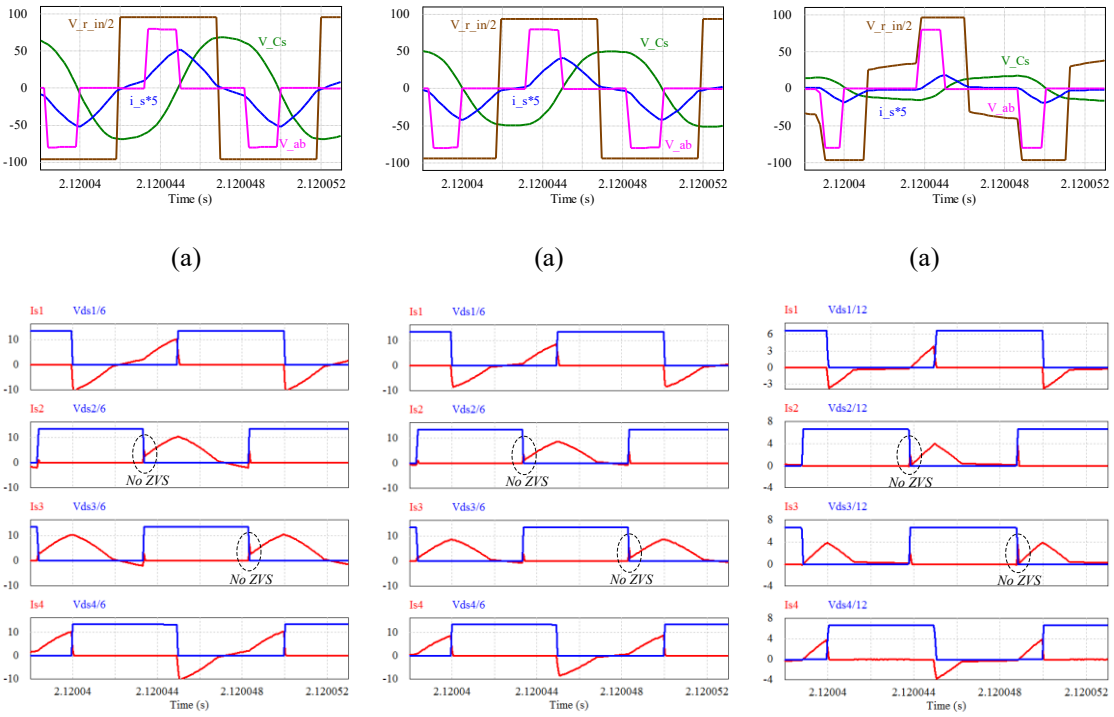


Fig. 3.20: PSIM simulation results for maximum input voltage $V_{s(max)}$ = 80 V when operated with phase-shift gating scheme for: (i) full-load, (ii) 75% of full-load and (iii) 20% of full-load, where, (a) resonant current i_s, inverter output voltage v_{AB}, rectifier input voltage v_{r_in}, resonant capacitor voltage v_{Cs}. (b) voltage across (v_{ds}) and respective current through (i_s) switches $S_1 - S_4$.

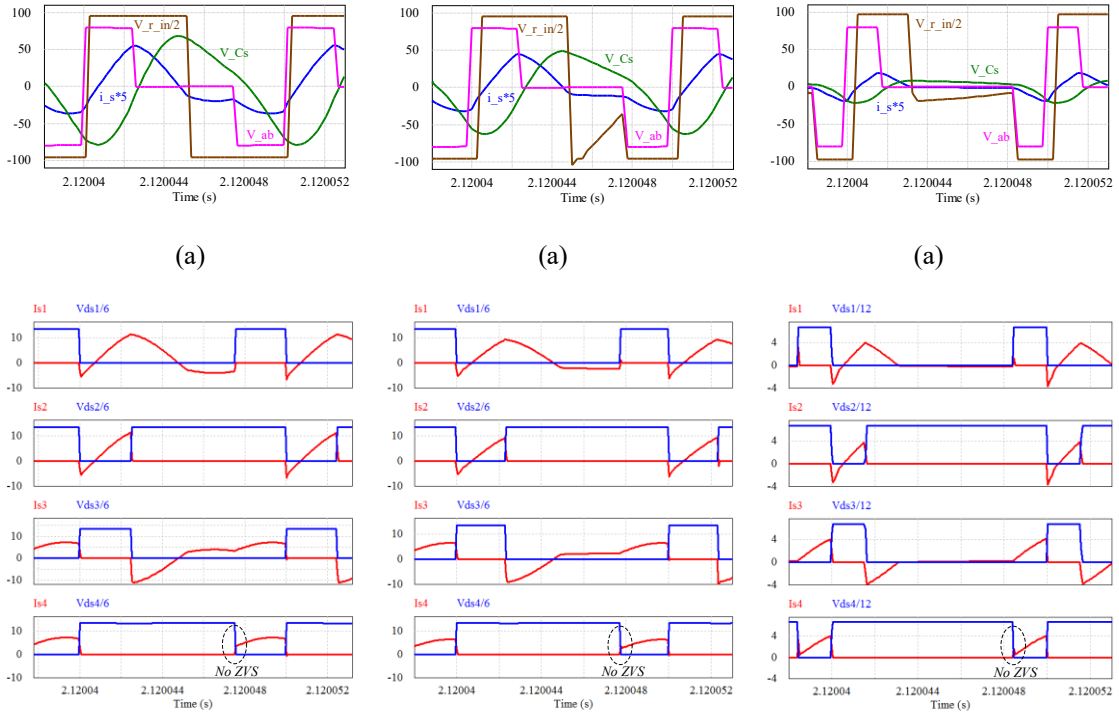


Fig. 3.21: PSIM simulation results maximum input voltage $V_{s(max)}$ = 80 V when operated with modified PWM gating scheme for: (i) full-load, (iii) 75% of full-load and (ii) 20% of full-load, where, (a) resonant current i_s, inverter output voltage v_{AB}, rectifier input voltage v_{r_in}, resonant capacitor voltage v_{Cs}. (b) voltage across (v_{ds}) and respective current through (i_s) switches $S_1 - S_4$.

3.5.2 Performance under Step Changes in Load:

The performance study of the converter under step changes in load is analysed in this part of the Section. One of the main objectives of the converter design is to maintain constant output voltage for variations in loading conditions. The ability of the converter to maintain constant output voltage when the load changes suddenly is tested by simulating its performance in PSIM. The phase-shift gating scheme with suitable pulse-width 'δ' mentioned in Table 3.2 for the corresponding step change in the load is applied and results are shown in Figs. 3.22-3.24. The PSIM simulation results for minimum input voltage $V_{s(min)}$ = 40 V when operated with PGS for step changes in load

current I_o from full-load to 75% load at t = 0.2 sec, and then to 20% load at t = 0.22 sec created by operating a load control switch is shown in Fig. 3.22. As the load is reduced from full-load to 75% load and then to 20% load, the output voltage V_o remains approximately constant at its full-load value as shown in Fig. 3.22(a). The expanded waveform of output voltage V_o is shown in Fig. 3.22(b). Here it is observed that, at the instant of sudden reduction in load, there is momentarily a rise in output voltage and the pulse-width angle 'δ' of the converter is however decreased to regulate the output voltage constant. The resonant current i_s for step decrease in the load and the expanded waveform of i_s are shown in Fig. 3.22(c) and Fig. 3.22(d) respectively. The smooth transition of the resonant current i_s as the step load changes can be observed in Fig. 3.22(d). The PSIM simulation results for minimum input voltage $V_{s(min)}$ = 40 V when operated with PGS for step changes in I_o from 20% of load to 75% load at t = 0.2 sec, and then to full-load at t = 0.22 sec is shown in Fig. 3.23(a). It is observed that, the output voltage has momentarily reduced at an instant of a step increase in the load and the pulse-width angle 'δ' of the converter is however increased to regulate the output voltage constant again as shown in Fig. 3.23(b). The resonant current i_s for step changes in the load and the expanded waveform of i_s are shown in Fig. 3.23(c) and Fig. 3.23(d) respectively. The smooth transition of the resonant current i_s as the step load changes can be observed in Fig. 3.23(d). The resonant capacitor voltage V_{Cs} for step changes in the load and the expanded waveform of V_{Cs} are shown in Fig. 3.24(a) and Fig. 3.24(b) respectively. The resonant capacitor voltage V_{Cs} remains sinusoidal and there is a smooth transition as the step load changes. The expanded waveforms of switch current i_{s1} and i_{s4} are shown in Fig. 3.24(c). The expanded waveforms of switch current i_{s2} and i_{s3} are shown in Fig. 3.24(d). The switch currents i_{s1}, i_{s2}, i_{s3} and i_{s4} have smooth transition without spikes during the step changes in load. The negative value of current in all the switches indicate ZVS turn-on of all the switches as antiparallel diodes conduct before the respective switches come into conduction.

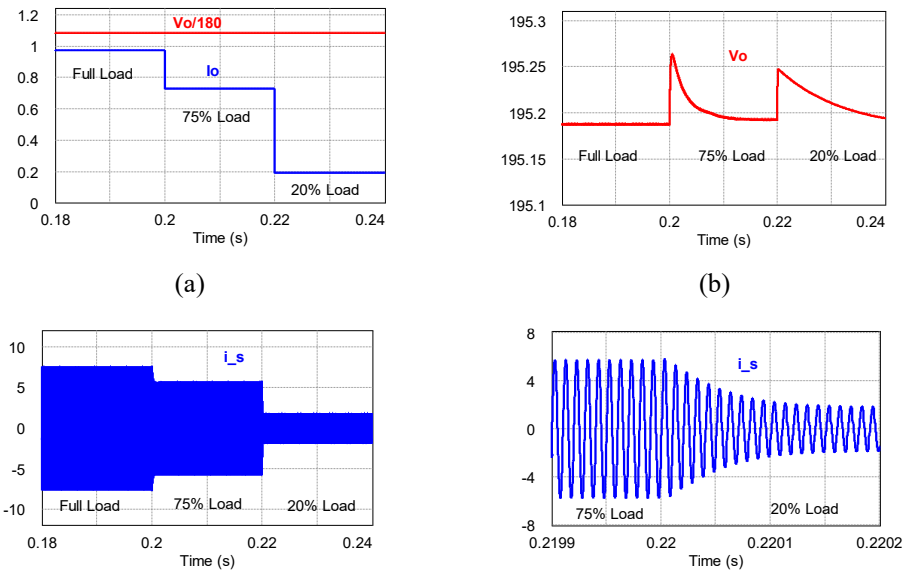


Fig. 3.22: PSIM simulation results for minimum input voltage $V_{s(min)}$ = 40 V when operated with phase-shift gating scheme for step changes in I_o from full-load to 75% load at t = 0.2 sec, and then to 20% load at t = 0.22 sec. (a) Waveforms of V_o and I_o (b) The expanded waveform of V_o. (c) Waveform of resonant current i_s. (d) The expanded waveform of i_s.

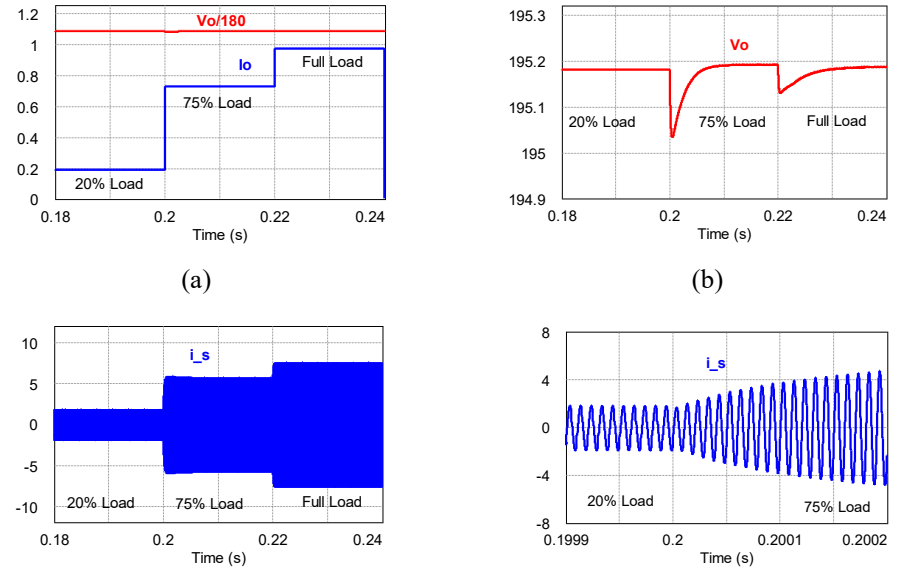


Fig. 3.23: PSIM simulation results for minimum input voltage $V_{s(min)}$ = 40 V when operated with phase-shift gating scheme for step changes in I_o from 20% of load to 75% load at t = 0.2 sec, and then to full-load at t = 0.22 sec. (a) Waveforms of V_o and I_o (b) The expanded waveform of V_o. (c) Waveform of resonant current i_s. (d) The expanded waveform of i_s.

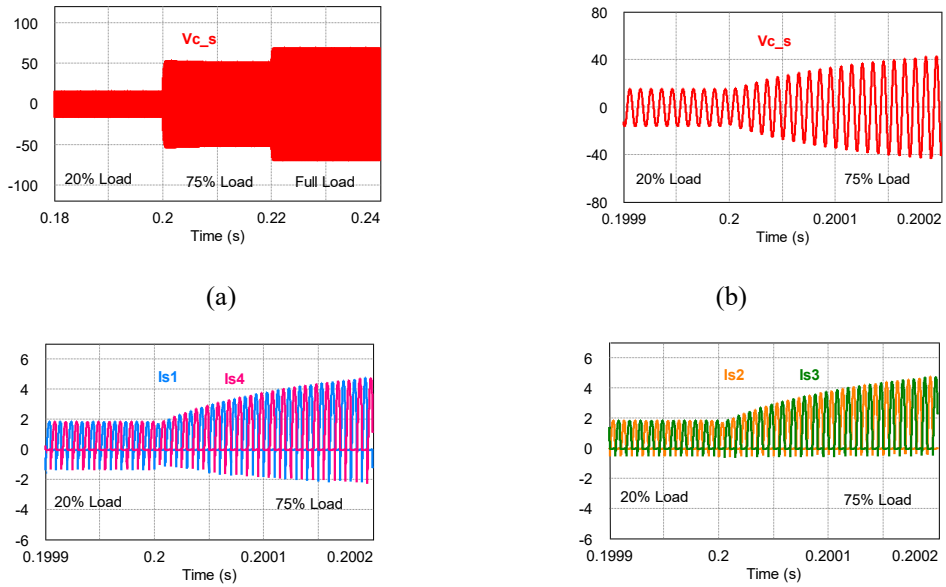


Fig. 3.24: PSIM simulation results for minimum input voltage $V_{s(min)}$ = 40 V when operated with phase-shift gating scheme for step changes in I_o from 20% of load to 75% load at t = 0.2 sec, and then to full-load at t = 0.22 sec. (a) Waveform of resonant capacitor voltage V_{Cs}. (b) The expanded waveform of V_{Cs}. (c) The expanded waveforms of switch current i_{s1} and i_{s4}. (d) The expanded waveforms of switch current i_{s2} and i_{s3}.

3.6 Experimental Results and Discussion

In order to verify the calculated and simulation results, a laboratory prototype is built and tested. The circuit parameters of the experimental prototype are given in Table 3.1. IRF540 MOSFET is used in making of the HF switched inverter. The WIMA polypropylene capacitor is used for making resonant capacitor and iron powdered toroidal cores are used in building the resonant inductors. The EE-type HF transformer of N87 material with 5:24 turns ratio is used. The DIGILENT NEXYS4 DDR Artix-7 FPGA board is used to generate gating pulses and is given to HCPL 2201 optocoupler and IR2110 driver circuit. The UF5404 diodes are used as secondary rectifier diodes. The experimental results shown in Fig. 3.25(a) of (i-iii) depict that the i_s lags v_{AB} when applied with PGS at minimum input voltage ($V_{s(min)}$ = 40 V) ensuring ZVS turn-on of all the main switches for changes in loading conditions. The Fig. 3.25(b) of (i-iii)

depicts the experimental waveforms when operated with PGS at maximum input voltage. Here, as the pulse-width of the inverter output voltage is reduced significantly to regulate V_o, the switches S_2 and S_3 lose ZVS during turn-on.

The experimental results shown in Fig. 3.26(a) of (i-iii) depict that the i_s lags v_{AB} when applied with MGS at minimum input voltage ($V_{s(min)}$ = 40 V) ensuring ZVS turn-on of all the main switches for variations in loading conditions. At maximum input voltage, only switch S_4 loses ZVS while turn-on as shown in Fig. 3.26(b) of (i-iii). This is an advantage as compared to two switches losing ZVS when the converter is operated with PGS. As expected theoretically with both the gating schemes, the peak resonant current reduces as the load is reduced from full-load to 20% of full-load maintaining

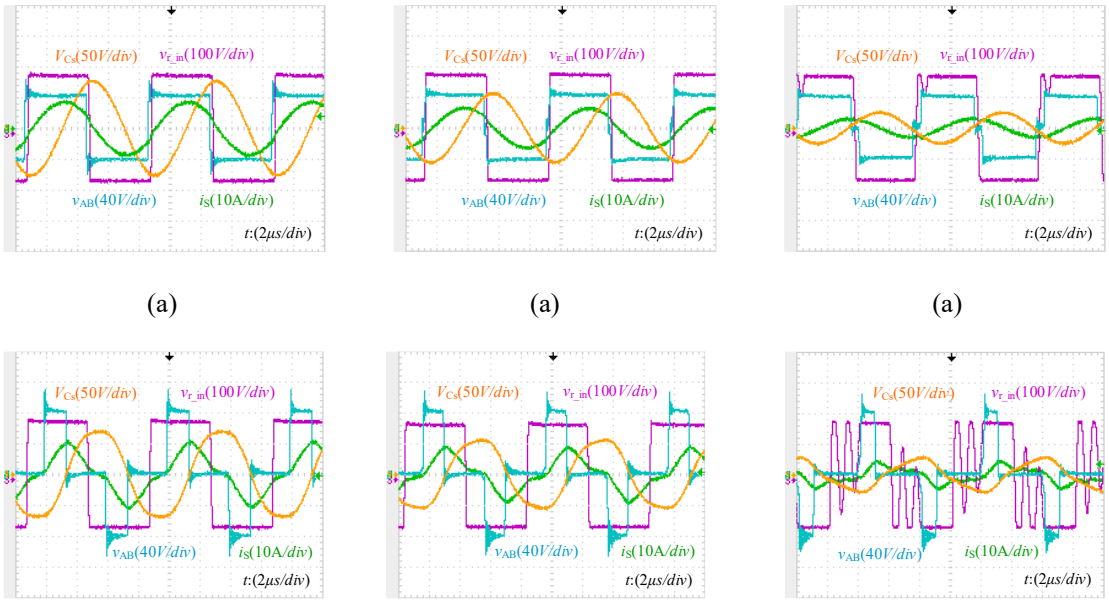


Fig. 3.25: Experimental results.(a) Minimum input voltage $V_{s(min)}$ = 40 V and (b) Maximum input voltage $V_{s(max)}$ = 80 V. For different loading conditions when applied with phase-shift gating scheme. where, resonant current i_s, inverter output voltage v_{AB}, rectifier input voltage v_{r_in}, resonant capacitor voltage v_{Cs}.

better light-load efficiency. Table 3.2 presents the comparison results of the converter when operated with PGS and MGS for various operating conditions. In general, the waveforms of V_{Cs} and i_s will be very close to the sinusoidal shape at full- load where, $\delta = \pi$. However, when the load is reduced, the pulse-width angle 'δ' is also decreased to regulate the output voltage constant, the sinusoidal waveforms get slightly distorted at light-load conditions. In simulations, the component values are used as obtained in the design calculations. However, the values of the components built in the laboratory had small variation from their design values which causes small variations in simulation and the experimental results. The outcome of the comparative study can be used to select a better control scheme for operating the CLL resonant converter under variable input voltage and loading conditions. The photograph of experimental setup of high-freqency transfomer isolated full bridge CLL resonant DC-DC converter with capacitive output filter is shown in Fig. 3.27.

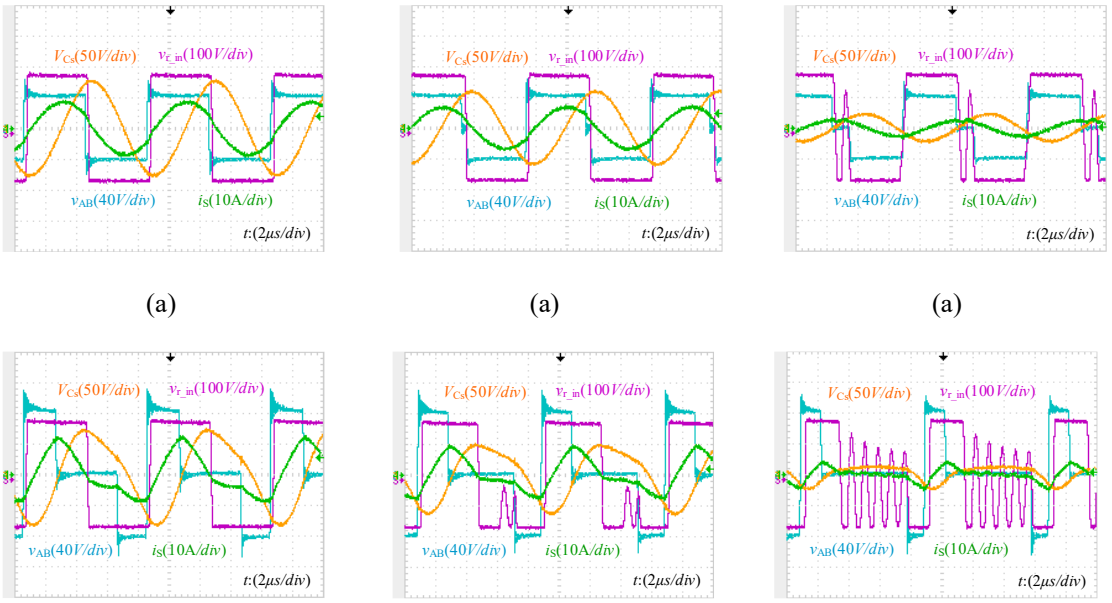


Fig. 3.26: Experimental results.(a) Minimum input voltage $V_{s(min)} = 40$ V and (b) Maximum input voltage $V_{s(max)} = 80$ V. For different loading conditions when applied with modified PWM gating scheme. where, resonant current i_s, inverter output voltage v_{AB}, rectifier input voltage v_{r_in}, resonant capacitor voltage v_{Cs}.

Table 3.2: Comparison of results when the converter is operated with phase-shift gating scheme and modified PWM gating scheme.

$V_{s(min)}$ = 40 V																			
Parameter	Full Load						75% of Full Load							20% of Full Load					
	Cal.		Sim.		Exp.		Cal.		Sim.		Exp.			Cal.		Sim.		Exp.	
	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	
V_o (V)	200	200	195.2	195.2	191.2	191.2	200	200	194.56	194.96	192	191.4	200	200	195.13	194.92	192.6	193.8	
I_o (A)	1	1	0.976	0.976	0.96	0.96	0.75	0.75	0.729	0.731	0.72	0.73	0.2	0.2	0.195	0.194	0.19	0.195	
$I_{s(f)}$ (A)	5.674	5.674	5.49	5.49	5.82	5.82	4.262	4.262	4.153	4.057	4.65	4.90	1.188	1.188	1.285	1.259	0.95	1.86	
$V_{Cs(f)}$ (V)	50.3	50.3	48.63	48.63	48.58	48.58	37.79	37.79	36.78	36.82	39.4	41.6	10.54	10.54	11.32	11.04	16.3	15.6	
δ (deg.)	179.9	179.9	178	178	174	174	169.17	172.33	166	169	166	166	163.91	168.61	150	153	149	148	
% η	96.34	96.34	97.8	97.8	91.18	91.18	96.73	96.72	98.24	98.07	92.4	92.9	97.34	97.31	98.07	97.6	91.48	92.62	

$V_{s(max)}$ = 80 V																			
Parameter	Full Load						75% of Full Load							20% of Full Load					
	Cal.		Sim.		Exp.		Cal.		Sim.		Exp.			Cal.		Sim.		Exp.	
	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	PGS	MGS	
V_o (V)	200	200	192.38	194.45	190.6	191.1	200	200	191.6	194.4	191.6	190.6	200	200	191.11	194.66	190.1	193.2	
I_o (A)	1	1	0.961	0.972	0.965	0.95	0.75	0.75	0.714	0.729	0.71	0.71	0.2	0.2	0.19	0.194	0.19	0.19	
$I_{s(f)}$ (A)	5.675	5.675	6.046	5.961	6.32	6.14	4.263	4.263	4.77	4.749	5.04	4.96	1.189	1.188	1.686	1.659	2.37	1.93	
$V_{Cs(f)}$ (V)	50.3	50.3	52.44	49.52	52.7	52.9	37.79	37.78	40.8	38.1	41.7	38.4	10.54	10.54	12.84	9.62	18.8	12.1	
δ (deg.)	60	89.99	63	89.5	67	88	59.7	89.74	61	82	65.5	81	59.35	89.43	43	55.5	45	53	
% η	88.9	92.55	95.65	96.9	86.75	87.23	87.24	91.88	95.71	96.81	85.02	88.56	65.70	81.31	93.97	94.59	82.08	84.97	

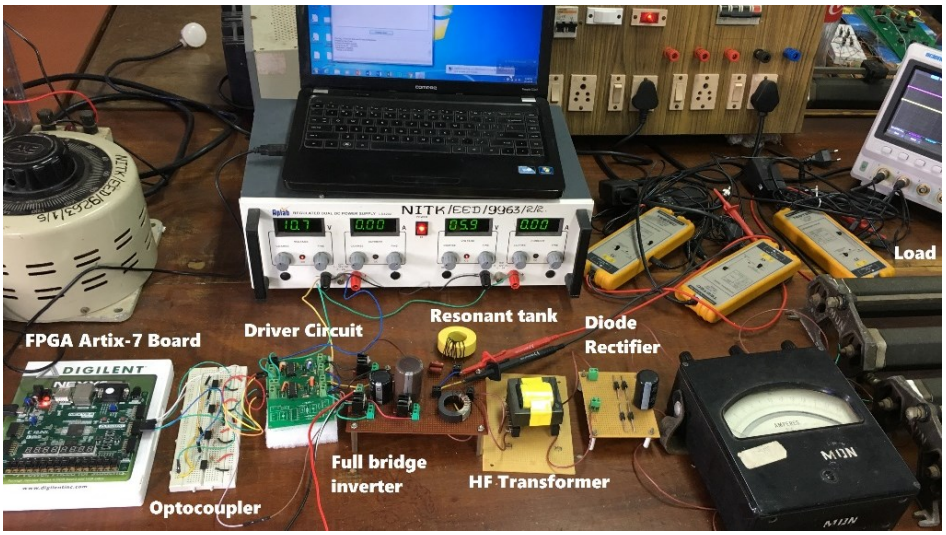


Fig. 3.27: Photograph of experimental setup of high-freqency transfomer isolated full bridge CLL resonant DC-DC converter with capacitive output filter.

3.7 Conclusion

The performance of high-frequency CLL resonant DC-DC converter operated with a phase-shift gating scheme (PGS) and modified PWM gating scheme (MGS) for wide variations in input voltage and loading conditions is studied. Fundamental harmonic approximation method is used for the steady-state analysis. The modeling and optimum design are carried out to have an efficient and compact converter. The proposed converter achieves ZVS turn-on of all the main switches for wide variations in loading when applied with minimum input voltage for both PGS and MGS. However, at maximum input voltage, it is shown that only one switch loses ZVS when operated with MGS as compared to two switches when operated with PGS. Hence, MGS is better in achieving higher efficiency of the converter. The theoretical and experimental results of the converter with both PGS and MGS are presented and compared to describe the performance features of the converter. It is seen that these results are in good agreement. Also, the performance of the designed converter under step changes in load is observed where, the converter is able to maintain constant output voltage. The resonant current

and the switch currents have smooth transitions when the step changes in load take place. Hence, the proposed resonant converter operated with MGS will be a good choice for the applications involving wide variations in input voltage and loading conditions.

Chapter 4

ANALYSIS AND DESIGN OF A HIGH-FREQUENCY TRANSFORMER ISOLATED FULL BRIDGE ZVT CLL RESONANT DC-DC CONVERTER

In this chapter, a zero-voltage transition (ZVT) auxiliary circuit along with a modified PWM gating scheme is proposed for a high-frequency full bridge CLL resonant DC-DC converter with a capacitive output filter. An approximate complex ac circuit approach is used for the steady state analysis of the converter. The optimum design of the converter is described with the help of design curves for a sample converter of 200 W rating operated with a switching frequency of 100 kHz. The converter with applied gating scheme and ZVT auxiliary circuit provides zero-voltage switching (ZVS) to all the switches for the entire variations in loading and input voltage conditions ensuring higher conversion efficiency. PSIM simulations are carried out to verify theoretical predictions about the performance of the converter for various operating conditions. Finally, experimental model of the converter is built in the laboratory and the experimental results are provided to verify the feasibility of the proposed converter. The theoretical, simulation and experimental results are given and discussed.

4.1 Introduction

The high-frequency CLL resonant converter topologies reported in (Asa et al. 2015b; a; Chakraborty et al. 1999; Chen et al. 2015; Huang et al. 2011; Tschirhart and Jain 2008) incorporates the advantageous features of both SRC, PRC and LCC resonant converter. Traditional resonant converters are regulated by varying switching frequency

(Bu et al. 1997; Kazimierczuk and Wang 1992; Steigerwald 1988). However, this variable frequency control produces electromagnetic interference (EMI) and problems associated with the design of filters and magnetics. Also, the effective use of parasitic components of transformers is difficult with variable frequency control (Chakraborty et al. 1999; Xie et al. 2005). Due to these problems, fixed-frequency control is chosen instead of the variable frequency control. In (Lin et al. 2017; Mangat et al. 2004; Tschirhart and Jain 2008), half-bridge resonant converters are given with fixed-frequency asymmetrical PWM gating signals for the output power control. However, this gating scheme develops excessive turn-off currents and rms currents which increase the conduction and switching losses. The full bride resonant converter described in (Bhat 1997a; Chakraborty et al. 1999; Koo et al. 2005; Lo et al. 2011) uses fixed-frequency phase-shifted 180^{o} wide gating signals which result in two switches losing ZVS with maximum input voltage and hence the efficiency is reduced. Also, the full-bridge CLL resonant converter in (Lo et al. 2011) has limited ZCS range and uses IGBT switches that lack high-frequency switching capabilities. The new/modified PWM gating scheme (Hamdad and Bhat 2001; Harischandrappa and Bhat 2014) applied to full bridge resonant converter provides ZVS to all the switches for variations in load with minimum input voltage and only one switch loses ZVS for maximum input voltage making it more advantageous than phase-shift gating scheme. The resonant converter fed with normal phase-shift gating scheme necessitates two ZVT auxiliary circuits to assist the switches to turn-on with ZVS thereby causing high conduction losses and increase in circuit complexity and cost (Cho et al. 1994; Lee et al. 2000; Wang 2006). Whereas, the CLL resonant converter proposed in this chapter, fed with modified PWM gating scheme requires only one ZVT auxiliary circuit to provide ZVS for all the main switches. The ZVT auxiliary circuit (Gautam and Bhat 2012; Khorasani et al. 2018; Ting et al. 2017; Wang 2006; Wu et al. 2008) helps the switch losing ZVS to turn-on with ZVS which reduces the switching losses and in-turn enhances the efficiency of the converter. This auxiliary circuit is operated for a small interval of time and consumes very less power which will not affect the overall operation of the converter. The

modified gating scheme applied to CLL topology provides ZCS feature for secondary side rectifier diodes. Hence, the switching losses in the rectifier diodes are minimized.

Analysis of a full bridge CLL resonant converter operating with the modified PWM gating scheme and application of the auxiliary circuit in a CLL resonant converter is not available in the literature. This chapter proposes the modified PWM gating scheme for a ZVT CLL resonant converter and its detailed analysis is carried out. The proposed converter provides ZVS for all the switches for entire variations in loading and input voltage conditions. The objectives of this chapter are, to: (i) propose a modified PWM gating scheme for the full-bridge ZVT CLL resonant DC-DC converter and to describe the circuit and its operation, (ii) carry out the modeling and analysis, (iii) illustrate the design procedure (iv) study the performance of the proposed converter with PSIM simulations and experimental prototype, and (v) compare the theoretical, simulation and experimental results. The layout of this chapter is as follows. Section 4.2 explains the principle of operation by giving the details of the proposed modified PWM gating scheme for CLL resonant converter and different operating modes of the converter. Steady-state analysis of the converter is given in Section 4.3 along with its modeling. The procedure for optimum design and typical design curves are depicted in Section 4.4. The PSIM simulation results of the CLL resonant converter are presented in Section 4.5. The theoretical and simulation results are validated with the help of an experiment and the results are presented in Section 4.6, finally the conclusions are drawn in Section 4.7.

4.2 Circuit Description and Operating Principle

4.2.1 Circuit Configuration

The circuit of a fixed frequency full-bridge ZVT CLL resonant DC-DC converter with capacitive output filter is shown in Fig. 4.1. It consists of a full bridge HF switched inverter along with the ZVT auxiliary circuit fed with a DC input V_s representing the power from a renewable energy source. A resonant tank circuit

consisting of capacitor C_s, inductors L_r and L_t is connected across output terminals (A, B) of the inverter bridge. A two winding HF transformer of turns ratio 1: n is connected between the tank circuit and the diode rectifier bridge. A filter capacitor (C_f) is connected at the output terminals of the diode rectifier that feeds the load resistance R_L. The series resonant capacitor C_s also helps in blocking the dc component so that the transformer core saturation can be avoided.

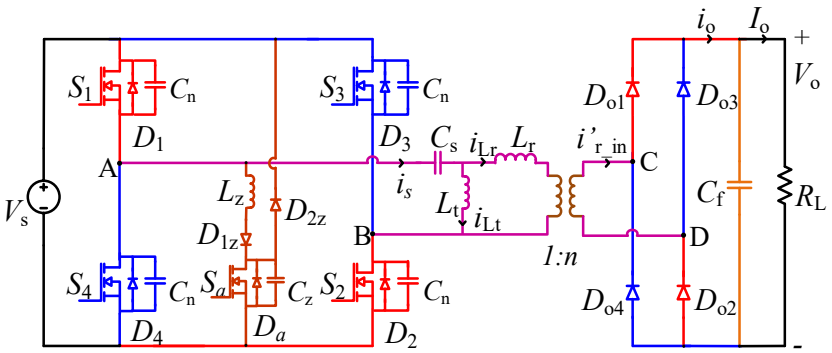


Fig. 4.1: Full bridge ZVT CLL resonant DC-DC converter with capacitive output filter.

The typical operating waveforms along with the modified PWM gating scheme of the proposed converter of Fig. 4.1 are shown in Fig. 4.2. Here, i_{Lp} is the current through the parallel inductor L_p shown in the converter equivalent circuit. The parallel inductor L_p is obtained by simplifying the converter circuit of Fig. 4.1 as explained later in Section 4.3.1**.** In the modified PWM gating scheme, the gating pulses of switches S_2 and S_4 are snipped by an angle 'α'and the widths of gating pulse of S_1 and S_3 are increased by the same angle 'α' as shown in Fig. 4.2. Application of these gating signals to the converter of Fig. 4.1 results in a square wave voltage v_{AB} of width 'δ' across the inverter output terminals AB. When the input voltage or load changes, to regulate the output voltage an angle 'α' is changed that in-turn changes the pulse-width of v_{AB} following the relation $\delta = \pi$-α. The converter is designed to operate with $\delta = 180^o$ (i.e., $\alpha = 0$) at full-load (FL) and with minimum input voltage. This angle 'δ' is reduced (or α is increased) to keep the output voltage constant whenever the load/input voltage is changed. For obtaining ZVS the converter is operated in the above resonance or lagging

power factor (PF) mode. From Fig. 4.2, it is seen that the resonant tank current i_s lags the inverter output voltage v_{AB} and the switch currents of all the switches (S_1-S_4) are negative before the current becomes positive in every cycle. This indicates that antiparallel diodes of the respective switches conduct before the switch conducts resulting in ZVS turn-on of the switches. For higher input voltage, the value of 'δ' decreases significantly and hence the switch S_4 loses ZVS as shown in Fig. 4.4(a). Therefore, the auxiliary circuit is made to activate by giving a short gating pulse to auxiliary switch S_a before applying gating signal to S_4 so that it turns on with ZVS as shown in Fig. 4.4(b). The power loss in the auxiliary switch is negligible as it carries a very small current for a short period.

4.2.2 Modes of Operation

Over a period of one cycle, the converter can work in either continuous current mode (CCM) or in discontinuous current mode (DCM). The CCM/DCM is identified by observing the rectifier input current i_{r_in} and parallel inductor current i_{Lp} waveform. If $i_{r\_in} = 0$ and i_{Lp} remains negative, then the operation is in DCM else CCM. The combination of devices conducting during different intervals in one cycle in CCM/DCM are discussed in the following subsection.

(i) Continuous Current Mode (CCM)

The stages of operation of CLL resonant converter working in CCM are identified in Fig. 4.2. Each stage is explained as following with the help of the equivalent circuit diagrams shown in Fig. 4.3(a)-(e). In CCM the converter operates with all the switches in ZVS when a minimum input voltage is applied.

Stage I *($t_0 < t < t_1$) [Fig. 4.3(a)]:* The gating pulses are applied to the switches S_1 and S_2. In the previous stage (i.e., ($t_4 < t < t_5$), the resonant/switch current 'i_s' is sinusoidal and the gating signals for the switches S_3 and S_4 are removed towards the end. However, since the resonant current i_s cannot change instantaneously, the antiparallel diodes D_1 and D_2 come into conduction to provide the same path for the smooth flow of i_s. The

inverter output voltage v_{AB} rises from 0 to '$+V_s$'. The output rectifier diodes D_{o1} and D_{o2} conduct to supply power to the load.

At the end of stage I (i.e., at t_1), the diodes D_1 and D_2 conduct in the reverse direction and takes some time (reverse recovery time) to recover to its reverse voltage blocking mode. This transient behavior of the semiconductor switch has not been depicted in Fig. 4.2 as only steady-state characteristics are considered.

Stage II *($t_1 < t < t_2$) [Fig. 4.3(b)]:* The negative resonant current starts to increase and becomes positive as the switches S_1 and S_2 turn-on and diodes D_1 and D_2 stop conducting. Since the antiparallel diodes of the switches S_1 and S_2 were conducting before the switches conduct, ZVS turn-on of the switches is achieved. The inverter output voltage v_{AB} remains at '$+V_s$' and the rectifier diodes D_{o1} and D_{o2} continue to conduct.

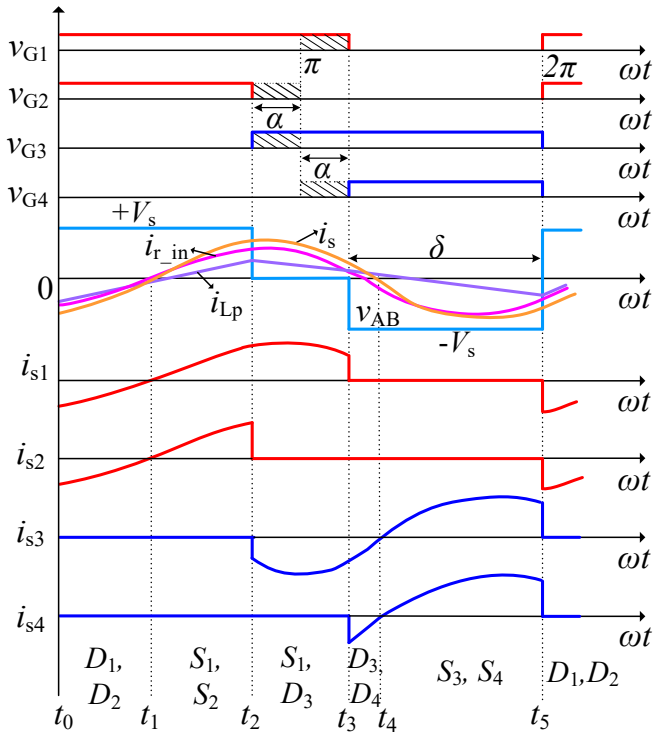


Fig. 4.2: Typical operating waveforms and gating scheme to describe the operation of the converter in CCM applied with minimum input voltage.

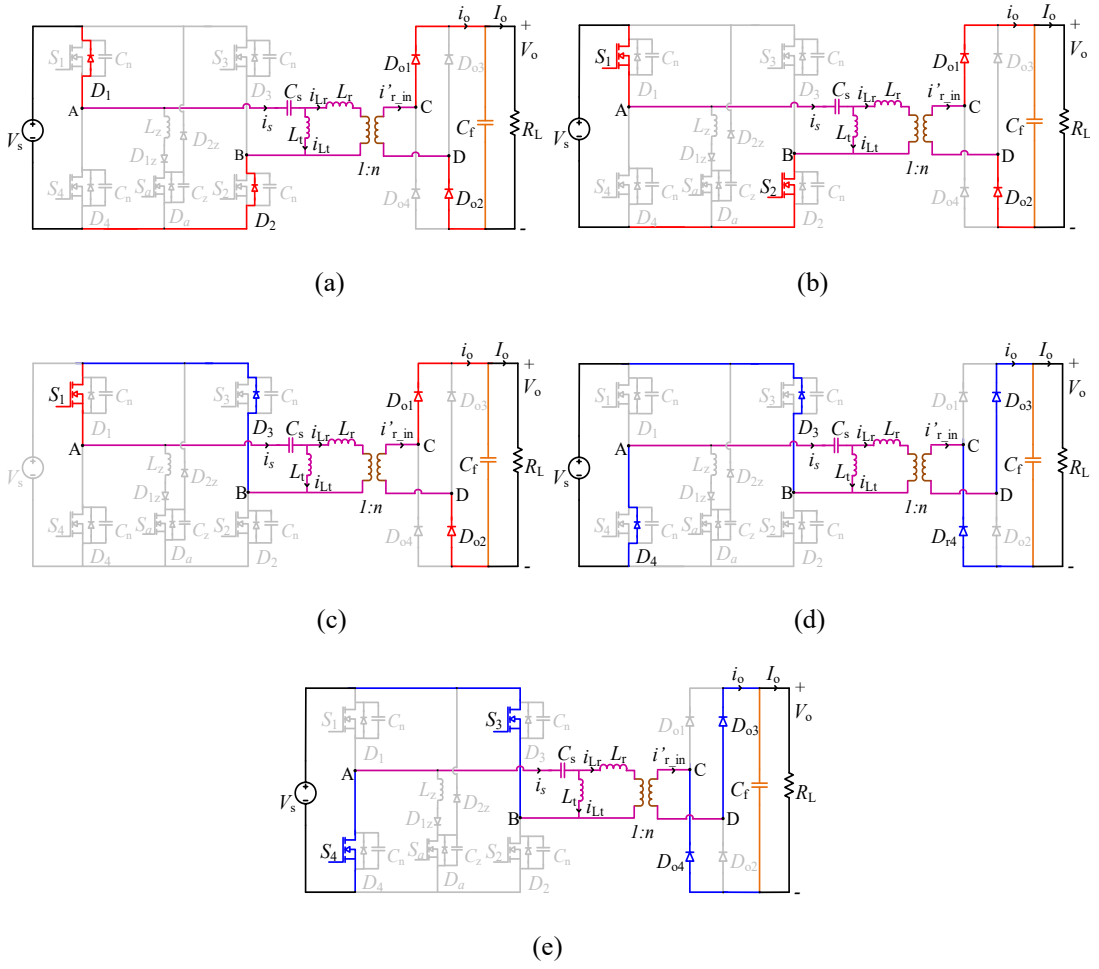


Fig. 4.3: Equivalent circuit diagrams of the converter for different stages in CCM. (a) Stage I, (b) Stage II, (c) Stage III, (d) Stage IV, (e) Stage V.

Stage III *($t_2 < t < t_3$) [Fig. 4.3(c)]:* In this stage, the gating pulse for switch S_2 is removed making it to turn-off. As the inductor current has to maintain the same direction, diode D_3 comes into conduction with S_1. Hence, the current freewheels in the path shown in Fig. 4.3(c) without flowing through the source, which brings the inverter output voltage v_{AB} to zero. The load is now supplied from the energy stored by the tank circuit components through the rectifier diodes D_{o1} and D_{o2}.

Stage IV *($t_3 < t < t_4$) [Fig. 4.3(d)]:* In this interval D_3 continues to conduct. Gating pulse for the switch S_1 is removed and it stops conducting. Hence the diode D_4 starts to

conduct providing a closed path of the current i_s to flow. Now the inverter output voltage v_{ab} changes from zero to '$-V_s$' and the rectifier diodes D_{o3} and D_{o4} start to conduct.

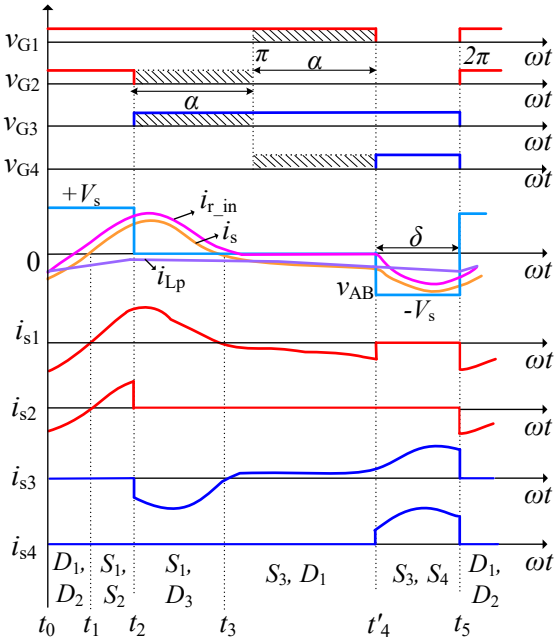
Stage V *($t_4 < t < t_5$) [Fig. 4.3(e)]:* The resonant current i_s changes its direction and switches S_3 and S_4 turn-on. Since the antiparallel diode D_3 and D_4 of these respective switches were conducting before this interval, the switches turn-on with ZVS. The rectifier diodes D_{o3} and D_{o4} continue to conduct, supplying power to the load.

(ii) Discontinuous Current Mode

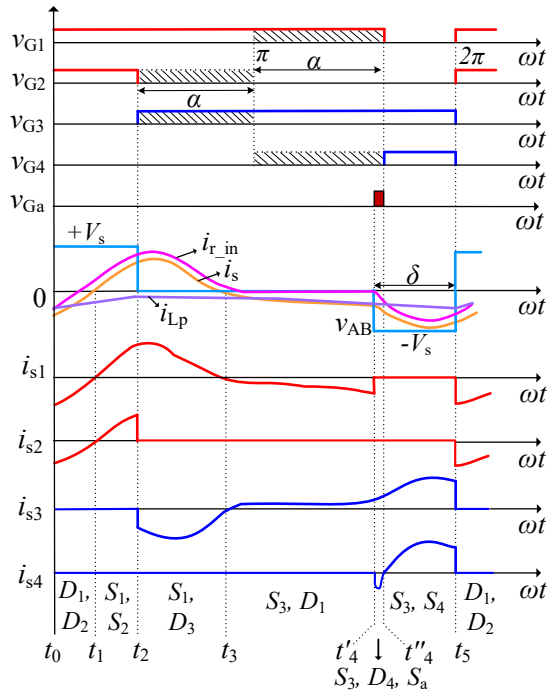
As the input voltage is increased to maximum, the output voltage can be regulated by decreasing the pulse-width which results in discontinuous current flowing through part of the tank circuit (i.e., $i_{r\_in} = 0$) and i_{Lp} remains always negative as shown in Fig. 4.4(a-b). The converter operation in DCM is same as that described in CCM till stage III. After stage III, the current i_{r_in} becomes zero and current i_s becomes negative to equal i_{Lp} which is explained in the following stages:

Stage IV' *($t_3 < t < t'_4$) [Fig. 4.5(a-b)]:* As the pulse-width 'δ' is reduced significantly, direction of i_s changes before the gating signals are applied to the switch S_4. This change in direction of i_s makes switch S_3 and diode D_1 to conduct which keeps the current i_{Lp} negative as shown in Fig. 4.4. During this interval, i_s freewheels using the stored energy in the tank circuit elements as shown in Fig. 4.5(a). This freewheeling of i_s continues till the energy in resonant components gets fully discharged further resulting in DCM. The rectifier input current i_{r_in} becomes zero and D_{o3} and D_{o4} stops conducting as shown in Fig. 4.5(b). The filter capacitor C_f solely will be supplying the load.

The gating pulse is applied to switch S_4 to turn-on with conducting i_s in the same direction and v_{AB} goes to negative as shown in Fig. 4.4(a). Since there is no antiparallel diode D_4 conducting before the turn-on of S_4, the switch turns on without ZVS as shown in Fig 4.4(a). To assist this switch to turn-on with ZVS, a ZVT auxiliary circuit is activated by giving a gating pulse of short width to switch S_a. Here, before the conduction of switch S_4, the auxiliary switch S_a is made to turn-on which is depicted in Fig. 4.4(b).



(a)



(b)

Fig. 4.4: Typical operating waveform and gating scheme to describe the operation of the converter in DCM applied with a maximum input voltage. (a) without activation of ZVT (b) with activation of ZVT.

Stage IV'' *($t'_4 < t < t''_4$) [Fig. 4.5(c-d)]:* The gating pulse v_{Ga} shown in Fig. 4.4(b) is applied to turn-on the auxiliary switch S_a and the antiparallel diode D_4 of switch S_4 also starts to conduct as shown in Fig. 4.5(c). The v_{ab} changes from zero to '$-V_S$' and the rectifier diodes D_{o3} and D_{o4} transfers power to the load. At the end of this interval, the S_4 is applied with gating signal to turn-on. As the antiparallel diode D_4 is in conduction before the S_4 turns on, ZVS turn-on of the switch S_4 is achieved which minimizes its turn-on switching losses. The small amount of energy stored in the auxiliary inductor L_Z is discharged as soon as the start of next stage (*Stage V*) as shown in Fig. 4.5(d) and the cycle repeats.

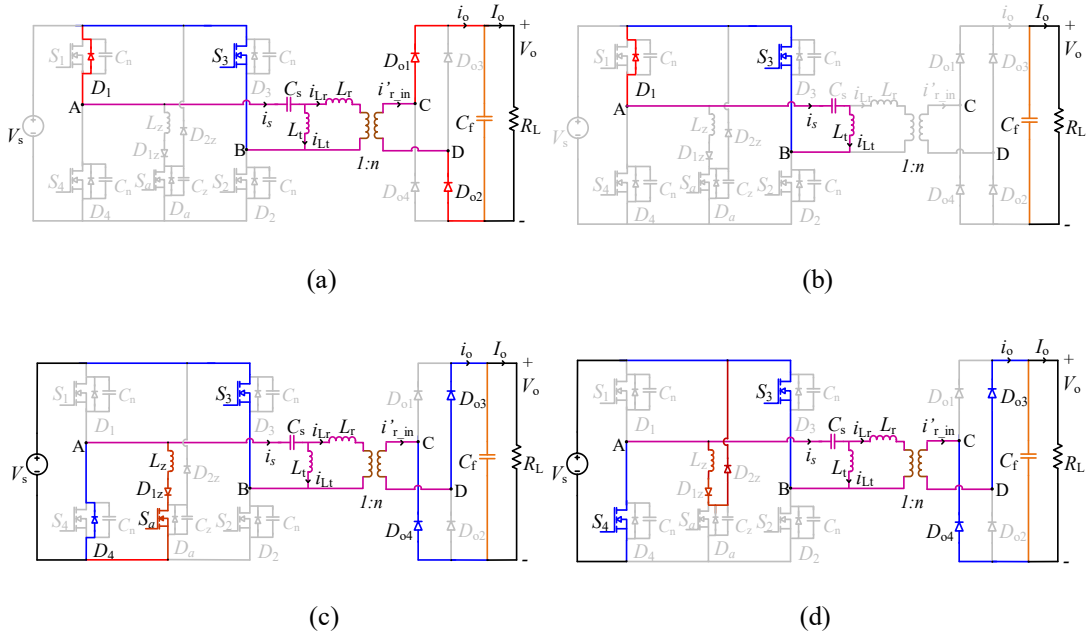


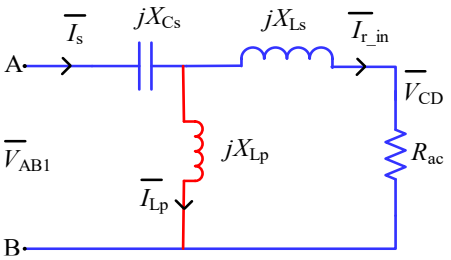
Fig. 4.5: Equivalent circuit diagrams of the converter for different stages in DCM. (a-b) Stage IV', (c-d) Stage IV''.

4.3 Modeling and Analysis of the Converter

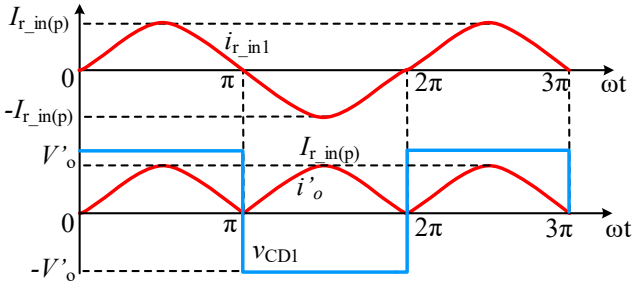
4.3.1 Converter Modeling

The converter is modeled by referring all the elements from the secondary side of the HF transformer to the primary. The transformer considered in modeling is

represented by its T-equivalent circuit. Further, the circuit is simplified to derive a phasor equivalent circuit (PEC) as depicted in Fig. 4.6(a). An equivalent ac resistance R_{ac} is used to replace the rectifier block, capacitive filter and load resistance of the converter. The R_{ac} is derived by accounting only the fundamental components of input current to the rectifier i_{r_in} and input voltage to the rectifier v_{CD} waveforms depicted in Fig. 4.6(b). The nature of waveform of i_{r_in} and v_{CD} relies on the type of output filter used.



(a)



(b)

Fig. 4.6: (a) Simplified circuit of the converter. (b) Waveforms of input current (i_{r_in}) and voltage (v_{CD}) to the rectifier of the converter.

The RMS values of the fundamental components of the rectifier input voltage (V_{CD1}) and current (I_{r_in1}) are derived by using Fig. 4.6(b) as,

$$I_{r\_in1} = \left(\frac{\pi}{2\sqrt{2}}\right) I'_o \tag{4.1}$$

$$V_{CD1} = \left(\frac{2\sqrt{2}}{\pi}\right) V'_o \tag{4.2}$$

The equivalent ac resistance R_{ac} is obtained by (4.1) and (4.2) as,

$$R_{ac} = \frac{V_{CD1}}{I_{r\_in1}} = \left(\frac{8}{\pi^2}\right) R'_L \tag{4.3}$$

where, $R'_{\mathrm{L}}(= V'_0/I'_0)$ is the load resistance referred to a primary side of the HF transformer of 1:n turns ratio.

4.3.2 Steady State Analysis of the Converter

With the help of phasor equivalent circuit shown in Fig. 4.6(a), the steady-state analysis of the full bridge CLL resonant converter of Fig. 4.1 operated with modified PWM gating scheme is carried out in detail using approximate complex ac circuit analysis method.

The RMS value of a fundamental component of inverter output voltage shown in Fig. 4.2 is derived as,

$$V_{\mathrm{AB1}} = \frac{\sqrt{2}}{\pi} V_{\mathrm{s}}(1 - \cos\delta) \tag{4.4}$$

where, δ is the pulse-width of the inverter output voltage used to regulate the output voltage V'_{o}.

From the phasor equivalent circuit shown in Fig. 4.6(a) and using (4.4), the converter gain is formulated as,

$$M = \frac{V'_0}{V_{\mathrm{s}}} = \frac{(1-cos\,\delta)/2}{\left(1-\frac{K}{F^2(K+1)}\right)+j\frac{\pi^2}{8}Q\left(F(K+1)-\frac{K}{F}-\frac{1}{F}\right)} \tag{4.5}$$

where, Inductance ratio, $K = L_{\mathrm{s}}/L_{\mathrm{p}}$ (4.6)

Frequency ratio, $F = \omega_{\mathrm{s}}/\omega_{\mathrm{r}}$ (4.7)

Resonant frequency, $\omega_{\mathrm{r}} = \frac{1}{\sqrt{L_{\mathrm{e}}C_{\mathrm{s}}}}$ (4.8)

Quality factor, $Q = (\omega_{\mathrm{r}}L_{\mathrm{e}}/R'_{\mathrm{L}})$ (4.9)

Effective inductance, $L_e = \frac{L_p \, . \, L_s}{L_p + L_s}$ (4.10)

L_e is the full-load approximated effective value of the parallel combination of L_s and L_p in Fig. 4.6(a). This approximation holds true at full-load as R_{ac} is at its lowest value when the load is increased from no-load to full-load.

From the Fig. 4.6(a), the equivalent impedance across terminals AB is obtained as,

$$Z_{AB} = R_{AB} + jX_{AB} \tag{14.11}$$

The magnitude and phase of the impedance are given as,

$$|Z_{AB}| = [R_{AB}^2 + X_{AB}^2]^{\frac{1}{2}} \tag{4.12}$$

$$\phi = arctan\left(\frac{X_{AB}}{R_{AB}}\right) \tag{4.13}$$

The R_{AB} and X_{AB} are given by,

$$R_{AB} = \frac{R_{ac} \, . \, X_{LP}^2}{R_{ac}^2 + (X_{LS} + X_{LP})^2} \tag{4.14}$$

$$X_{AB} = \frac{R_{ac}^2 (X_{LP} + X_{CS}) + X_{LP}^2 (X_{LS} + X_{CS}) + X_{LS}^2 (X_{LP} + X_{CS}) + 2 \, X_{LS} \, X_{LP} X_{CS}}{R_{ac}^2 + (X_{LS} + X_{LP})^2} \tag{4.15}$$

where, $X_{LS} = \omega_s L_s$, $X_{LP} = \omega_s L_p$, $X_{CS} = -\frac{1}{\omega_s C_s}$

The peak current through the switch is obtained as,

$$I_{sp} = \frac{V_{AB1(max)}}{|Z_{AB}|} \tag{4.16}$$

The peak voltage across the resonant capacitor C_s is given as,

$$V_{Csp} = I_{sp} \, X_{Cs} \tag{4.17}$$

The peak current through inductor L_s is given as,

$$I_{r\_in(p)} = \frac{V_{CD(p)}}{R_{ac}} \tag{4.18}$$

The peak current through inductor L_p is given by,

$$I_{\mathrm{Lp(p)}} = I_{\mathrm{sp}} - I_{\mathrm{r\_in(p)}} \tag{4.19}$$

The current through the switch is,

$$i_{\mathrm{s}} = I_{\mathrm{sp}} \sin(\omega t - \phi) \tag{4.20}$$

The kVA/kW rating of resonant tank circuit can be obtained by using,

$$\frac{kVA}{kW} = \frac{I^2_{\mathrm{r\_in(r)}} \cdot X_{\mathrm{Ls}} + I^2_{\mathrm{Lp(r)}} \cdot X_{Lp} - I^2_{\mathrm{s(r)}} \cdot X_{\mathrm{Cs}}}{P_o} \tag{4.21}$$

where, P_o is the rated output power of the converter.

4.4 Design of the Converter

The design of proposed CLL resonant converter shown in Fig. 4.1 is explained with the help of a design example as given in Table 4.1. Design curves are drawn and are used in selecting different design parameters to make converter design optimum. Selection of the optimum design parameters is a prime factor in making a reliable, compact and efficient converter. The converter is designed by considering the toughest operating condition of full-load current and minimum input voltage.

4.4.1 Design Trade-off

The selection of optimum design parameters is made with the help of design curves shown in Figs. 4.7-4.8. Main objective of the design is to regulate the output voltage for variations in load and input voltage by controlling the pulse-width 'δ' as per the modified PWM gating scheme described in Fig. 4.2. The intent of the converter design is to obtain ZVS by making the converter to operate with lagging PF which minimizes the turn-on losses. This is achieved by choosing the value of F greater than one in (4.7). Also, the converter is designed to reduce peak switch current as load current is reduced so that good light-load efficiency is maintained which is taken care by choosing a proper value of full-load quality factor Q_F. The change in peak switch

current I_{sp} as a function of load current I_o using (4.16) for various values of Q_F is plotted in Fig. 4.7(i)(a-b) for $K = 0.1$ and $K = 0.2$ at $F = 1.05$. From these design curves, it is observed that higher values of Q_F will increase I_{sp} with increase in the load current I_o. Under light-load conditions, I_{sp} reduces with an increase in the value of Q_F. This reduction in current is not so noticeable for $Q_F > 2$. From (4.9) it is seen that the value of inductance L_e is directly proportional to Q_F. Hence, $Q_F = 1$ is favorable.

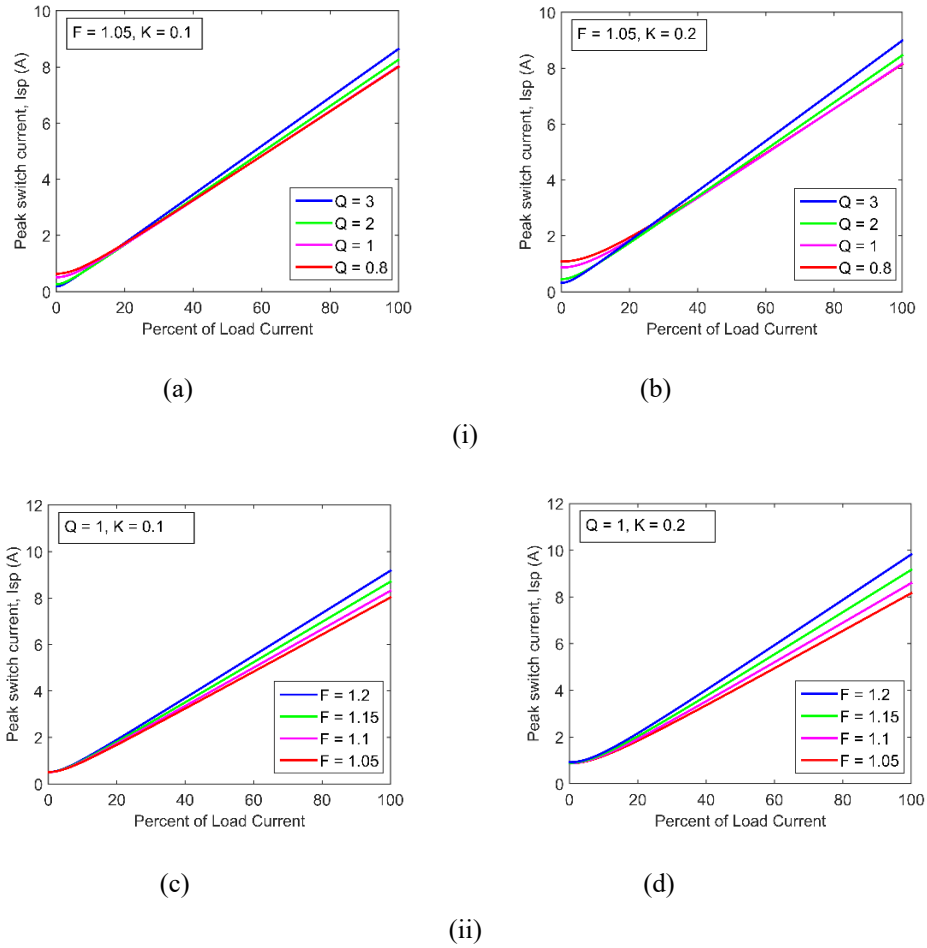
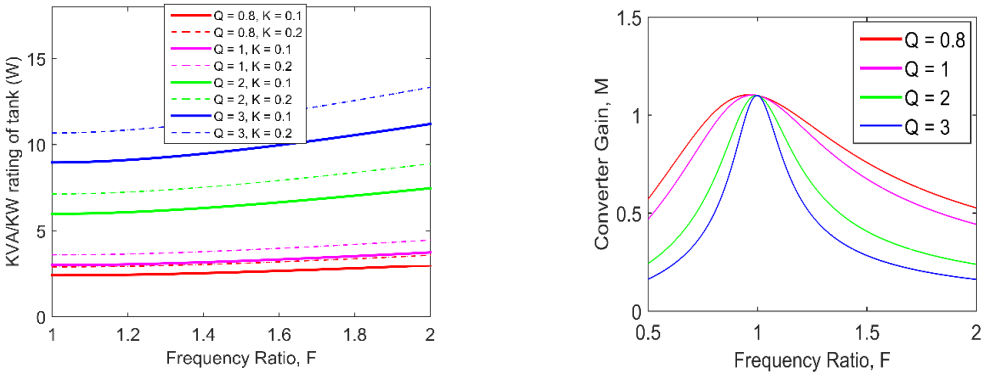


Fig. 4.7: Peak switch current variation with percentage of full-load current at constant output voltage for full-load value. (i) For $F = 1.05$ and for different values of Q_F. (a) $K = 0.1$ (b) $K = 0.2$. (ii) For $Q_F = 1$ and different values of F. (c) $K = 0.1$ (d) $K = 0.2$.



(a) (b)

Fig. 4.8: (a) kVA/kW rating variation of tank circuit versus F for various values of Q and for $K = 0.1$ and $K = 0.2$. (b) Converter gain versus F with variation in Q.

The change in I_{sp} as a function of I_o for various values of F is plotted in Fig. 4.7(ii)(c-d) for $K = 0.1$ and $K = 0.2$ at $Q_F = 1$. It is observed that for $K = 0.1$, the peak switch current I_{sp} reduces as compared to that with $K = 0.2$. The kVA/kW rating of the tank circuit given in (4.21) is plotted for various values of F and Q_F at $K = 0.1$ and $K = 0.2$ and is shown in Fig. 4.8(a). The decrease in Q_F will decrease kVA/kW rating of a tank circuit which results in low losses in the converter. From Fig. 4.8(a) it is also observed that the kVA/kW rating is low for a lower value of K. Hence, from Figs. 4.7-4.8, $Q_F = 1$ and $K = 0.1$ are chosen. Fig. 4.8(b) presents the change in converter gain M for the changes F and Q. To operate the converter in lagging PF mode for having the advantage of ZVS of the switches, $F = 1.05$ is selected.

The output voltage as referred to primary, $V_o' = 43.14$ V. The selected parameters i.e., $Q_F = 1$, $K = 0.1$ and $F = 1.05$ are used in the calculation of converter gain from (4.5), i.e., $M = 1.078$.

The turns ratio of the high-frequency transformer is calculated using,

$$n = \frac{V_o}{V_o'} \tag{4.22}$$

The load resistance R_L referred to the primary is,

$$R_L' = \frac{R_L}{n^2} \tag{4.23}$$

The turns ratio obtained using (4.22) is, n = 4.635 and the value of R'_L using (4.23) is R'_L = 9.308 Ω. From equations (4.3) and (4.6)-(4.10) the values of the tank circuit elements are obtained as L_s = 17.11 μH, C_s = 0.1795 μF. L_p = 171.1 μH.

4.4.2 Design of ZVT Auxiliary Circuit

The ZVT auxiliary circuit is designed and used to assist switch S_4 to turn-on with ZVS when the converter operates with the maximum input voltage. Now with this ZVT auxiliary circuit, the converter is able to provide ZVS to all the MOSFET switches for the entire variations in loading and input voltage conditions. The design procedure for the ZVT auxiliary circuit given in (Gautam and Bhat 2012) is followed for determining the ZVT auxiliary circuit elements. The resonant frequency of ZVT auxiliary circuit f_z is assumed to be about 30 times of the switching frequency f_s for a short transition time.

$$L_z = \frac{1}{(60\pi.f_s)^2.C_z} \tag{4.24}$$

The peak resonant current in the auxiliary circuit is,

$$I_{\mathrm{ZVT(p)}} = \frac{V_{\mathrm{s(max)}}}{\sqrt{L_z/C_z}} \tag{4.25}$$

The gating pulse-width of the ZVT auxiliary switch S_a is,

$$t_{\mathrm{ZVT}} = \frac{L_z \cdot I_{\mathrm{in(avg)}}}{V_{s(max)}} + \frac{\pi}{4} \cdot \sqrt{L_z \cdot C_z} + t_d \tag{4.26}$$

where t_d is the conduction time of the antiparallel diode of switch S_4.

The L_z and C_z are respectively the inductor and capacitor used in the ZVT auxiliary circuit of the converter shown in Fig 4.1. The value of ZVT auxiliary

components obtained using (4.24) and (4.25) are L_z = 0.8488 μH, C_z = 3.315 nF. The t_{ZVT} obtained using (4.26) is 214.71 ns (by assuming t_d = 120 ns). The auxiliary switch is activated for a very short interval of time which carries only a small initial current of the converter. The peak current in the auxiliary circuit $I_{ZVT(p)}$ is less than the peak resonant current i_{sp} of 8 A. Hence, the peak auxiliary switch current $I_{ZVT(p)}$ is chosen as 8 A for the worst conditions in the design of auxiliary circuit. The ZVT auxiliary switch carries very small current and hence losses in the auxiliary switch are negligible. The switching transition of ZVT auxiliary circuit is of very short interval and hence is not included in the theoretical analysis.

4.5 Simulation Results

The ZVT CLL resonant converter circuit of Fig. 4.1 designed in Section 4.4 is simulated using PSIM software to study its performance. The simulation is carried out with the minimum and maximum input voltages for three different loading conditions i.e., full-load, half-load and 10% of full-load as given in the following cases: Case I: $V_{s(min)}$ = 40 V and full-load; Case II: $V_{s(min)}$ = 40 V and half-load; Case III: $V_{s(min)}$ = 40 V and 10% of full-load; Case IV: $V_{s(max)}$ = 80 V and full-load; Case V: $V_{s(max)}$ = 80 V and half-load; Case VI: $V_{s(max)}$ = 80 V and 10% of full-load. In the simulations, the pulse-width angle 'δ' is changed to keep the output voltage constant at its full-load value when the load current or input voltage is changed. Since open-loop control is used, a number of iterations were carried to determine the required value of *'δ'* that keeps the output voltage constant at its full-load value. The simulation results for all the aforementioned cases are shown in Figs. 4.9-4.11.

It is observed from Figs. 4.9(a) of (i-ii) and 4.10(a) of (i) that, the converter operates in lagging PF mode providing ZVS for all the switches for wide variations in load from full-load to 10% of full-load when minimum input voltage is applied. From Figs. 4.9(b) of (i-ii) and 4.10(b) of (i), we notice that all the switches are turned-on during the conduction of its respective antiparallel diode which results in ZVS turn-on of the switches at different loading conditions. The voltage across the switch when it is

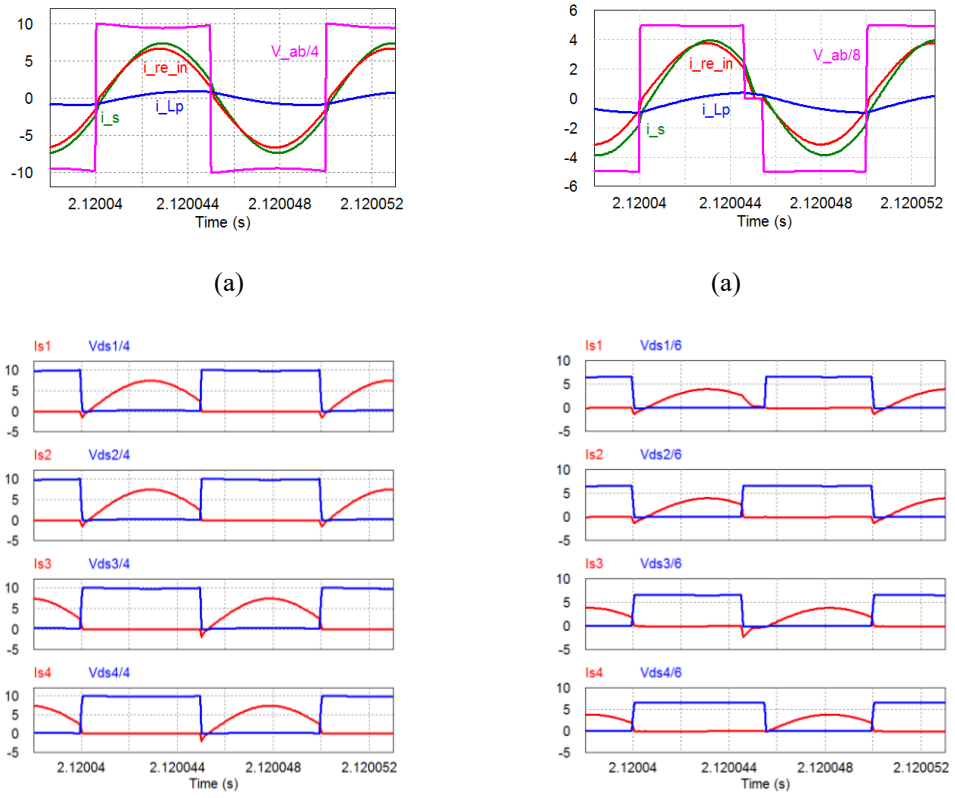
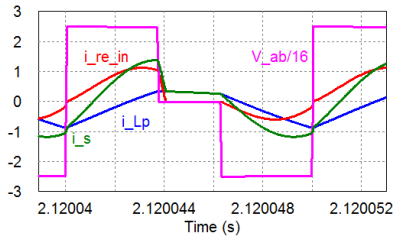


Fig. 4.9: Simulation waveforms. (a) inverter output voltage v_{AB}, resonant current i_s, current through parallel inductor i_{Lp}, current at the input terminals of rectifier i_{re_in}. (b) voltage across switches (v_{ds}) and respective current through the switches (i_s).

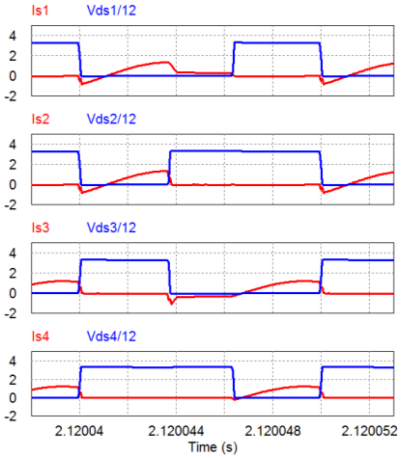
in off condition is same as the input voltage which decides the device rating. The peak inverter output current decreases approximately from 7.76 A at full-load [see Fig. 4.9(a) of (i)] to 1.05 A at 10% of full-load [see Fig. 4.10(a) of (i)] with minimum input voltage ($V_{s(min)}$ = 40 V) applied. The simulation waveforms in Figs. 4.10(a) of (ii) and 4.11(a) of (i-ii) are obtained when the converter is applied with maximum input voltage with activation of ZVT auxiliary circuit. From Figs. 4.10(b) of (ii) and 4.11(b) of (i-ii), we observe that when maximum input voltage is applied, the ZVT auxiliary switch provides ZVS for the switch S_4 for varying loading conditions. Hence, all the switches turn-on with ZVS resulting in higher efficiency. The peak inverter output current

decreases approximately from 8.42 A at full-load [see Fig. 4.10(a) of (ii)] to 1.39 A at 10% of full-load [see Fig. 4.11(a) of (ii)] with maximum input voltage ($V_{s(max)}$ = 80 V) applied.

The simulation results can be summarized as: the peak resonant current reduces as the load is decreased in all the six cases as presented in Figs. 4.9-4.11. Hence, light-load efficiency of the converter is high. The proposed converter operates with ZVS turn-on of all the switches for wide variations in loading and input voltage conditions.

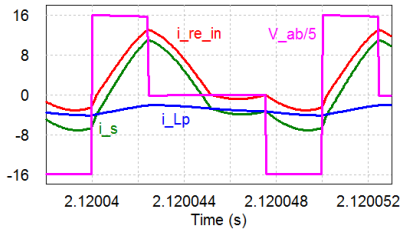


(a)

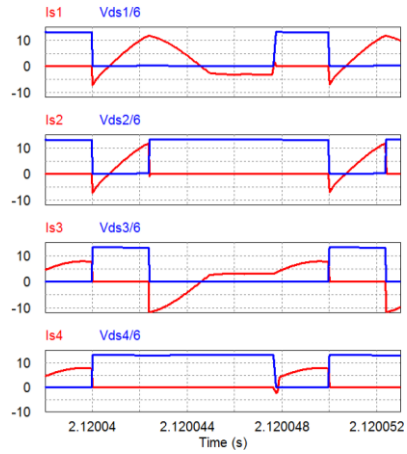


(b)

(i) Case: III



(a)



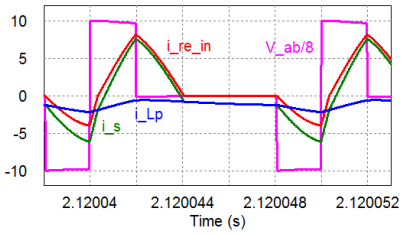
(b)

(ii) Case: IV

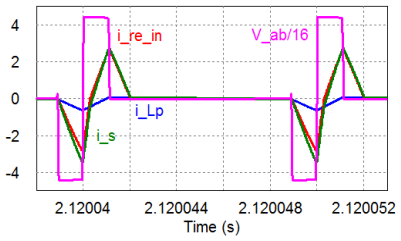
Fig. 4.10: Simulation waveforms. (a) inverter output voltage v_{AB}, resonant current i_s, current through parallel inductor i_{Lp}, current at the input terminals of rectifier i_{re_in}. (b) voltage across switches (v_{ds}) and respective current through the switches (i_s).

Table 4.1: Specifications of the converter

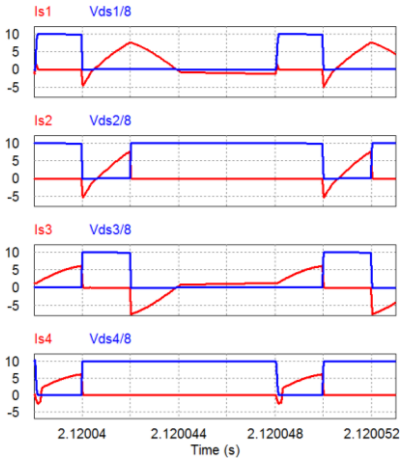
Minimum input DC voltage	40 V
Maximum input DC voltage	80 V
Rated output DC voltage	200 V
Rated Output power	200 W
Switching frequency	100 kHz



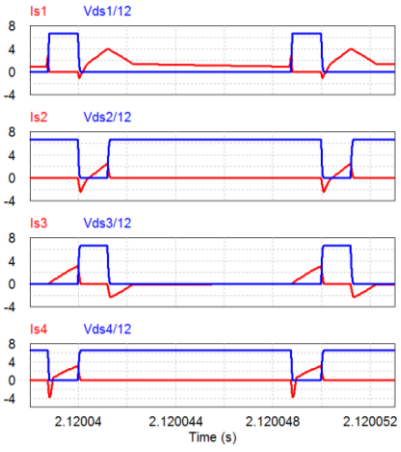
(a)



(a)



(b)



(b)

(i) Case: V

(ii) Case: VI

Fig. 4.11: Simulation waveforms. (a) inverter output voltage v_{AB}, resonant current i_s, current through parallel inductor i_{Lp}, current at the input terminals of rectifier i_{re_in}. (b) voltage across switches (v_{ds}) and respective current through the switches (i_s).

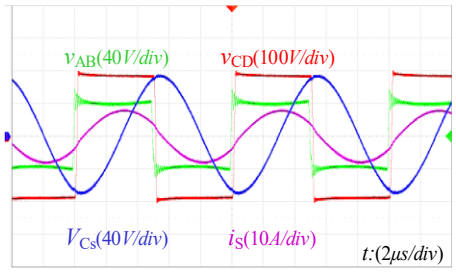
4.6 Experimental Results

To validate the proposed topology designed in Section 4.4, an experimental prototype was built in the laboratory. The converter's ability to keep the output voltage constant while maintaining ZVS is tested by applying wide range of input voltage and load. An HF transformer of 5:24 turns ratio was built using TDK-N87 EE-type core. The tank circuit is built with inductor of iron powdered toroidal cores and the series capacitor (WIMA polypropylene film) were used in building the converter. The gating pulses were generated by Xilinx Artix-7 FPGA board programmed using Verilog code and interfaced with the IR2110 driver circuit through the optocoupler HCPL 2201. The switching devices used were MOSFET (IRF540) for the full bridge inverter and diodes (UF5404) for the secondary output rectifier. A toroidal ferrite inductor core, an auxiliary switch MOSFET (IRF540) and MBR20100CT schottky diodes are used in the ZVT auxiliary circuit. The sinusoidal current through the rectifier diodes and the use of ultra-fast diodes (UF5404) as output rectifier diodes result in switching the diodes smoothly without suffering from di/dt and reverse recovery problems. The rectifier diode voltages are also clamped to the output voltage through the output capacitor filter C_L. Hence, the impact of reverse recovery of secondary rectifier diodes is negligible. The leakage inductance of transformer results in voltage drop due to commutation overlap of the secondary side rectifier diodes. This reduces the average (DC) output voltage applied to the load terminals.

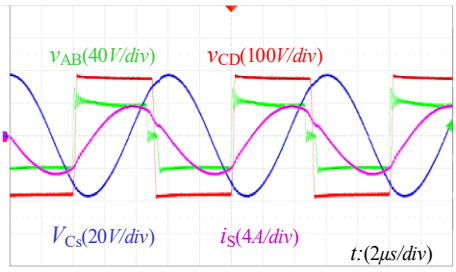
It can be observed from the experimental results shown in Fig. 4.12(i-iii) that the resonant current lags the inverter output voltage ensuring lagging PF operation which confirms ZVS operation of the switches. When the maximum input voltage is applied (Fig. 4.12(iv-vi)), the auxiliary circuit provides ZVS to the switch S_4. The peak resonant current reduces as the load is decreased keeping good efficiency at light-load. The waveforms of the voltage across the switches and their respective gating signals for all switches are shown to assure ZVS turn-on of the switches in Figs. 4.13(i-iii) and 4.14(i-iii). All the switches turn-on with ZVS for variations in load from full-load to 10% of full-load [see Fig. 4.13(i-iii)] when minimum input voltage is applied. However, when

the maximum input voltage is applied, with the assistance of the ZVT auxiliary circuit to one switch (S_4), the converter is able to provide ZVS to all the switches for variations in load from full-load to 10% of full-load [see Fig. 4.14(i-iii)]. The proposed converter provides ZVS for all the switches for the entire variations in loading and input voltage conditions. The comparison of converter efficiency with and without ZVT auxiliary circuit during the operation with maximum input voltage is given in Table 4.2 along with other theoretical, simulation and experimental results.

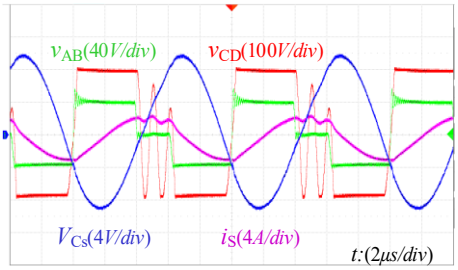
The power loss analysis shown in Table 4.3 is performed in order to estimate the losses in various parts of the converter and determine the overall efficiency for different operating cases. The possible reasons for the difference between these results are:
(i) since the converter analysis is done by using approximate complex AC circuit method, in theoretical calculations only fundamental component of voltage and current is considered while in simulation and experiments effects of all the harmonics is included; (ii) in theoretical calculations, the voltage drop across all the elements is neglected. In simulations, only the drain-to source resistance of $R_{DS}(on) = 0.044\ \Omega$ is set for MOSFET and all other elements are treated as ideal. However, in the experiment all the elements would have voltage drop and some power loss in them. Hence, the experimental efficiency is generally less compared to the calculated and simulation efficiency; (iii) in theoretical calculations, the transformer loss is assumed as 1% of the output power at different loading conditions. In simulations, all the parameters are referred to primary of the transformer and the circuit is developed. But in experiment, for transformer only the copper loss changes as the load is reduced while iron losses remain the same; (iv) in calculations and simulations, the component values are chosen as obtained in the design. However, the values of components built in the laboratory had small variations from their designed values.



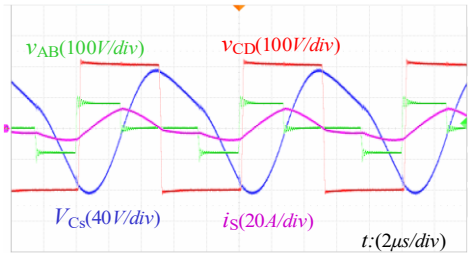
(i) Case: I



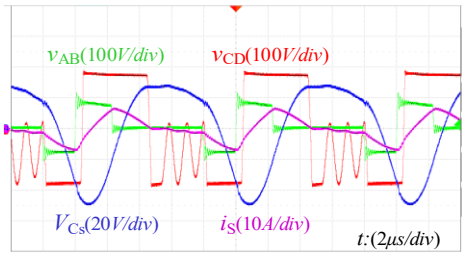
(ii) Case: II



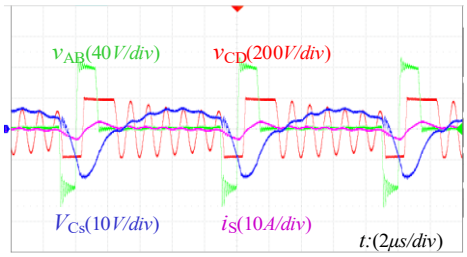
(iii) Case: III



(iv) Case: IV

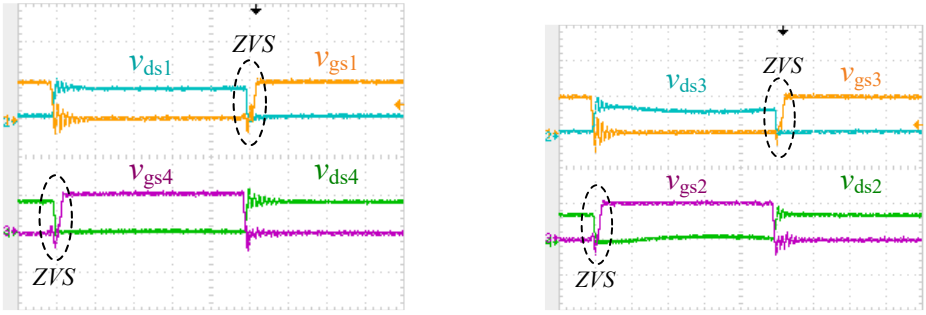


(v) Case: V

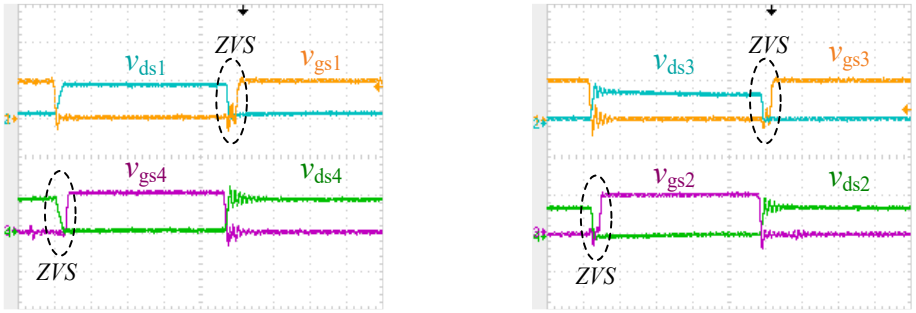


(vi) Case: VI

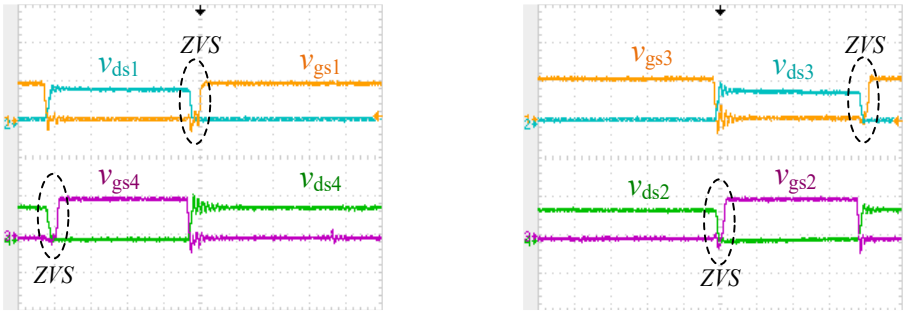
Fig. 4.12: Experimental results (Cases (I-VI)). Inverter output voltage (v_{AB}), resonant current (i_s), voltage across series capacitor (v_{Cs}), voltage across input terminals of rectifier (v_{CD}).



(i) Case: I

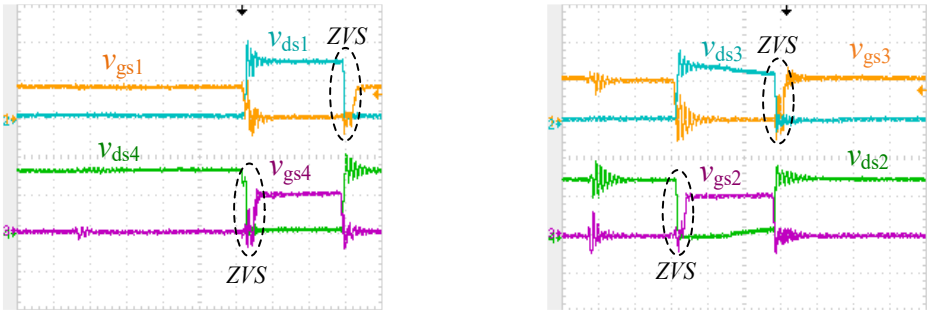


(ii) Case: II

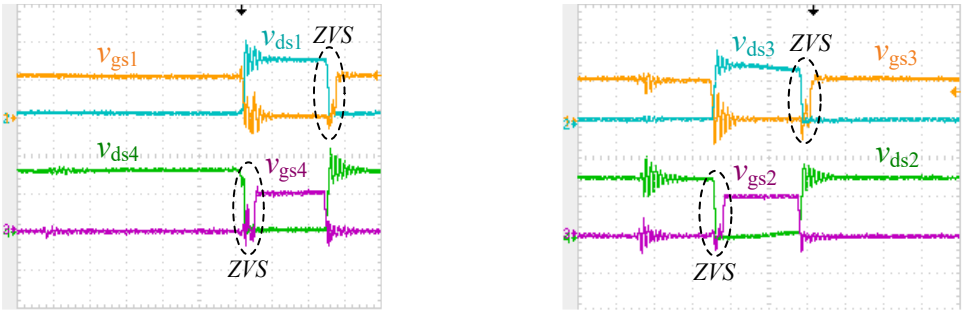


(iii) Case: III

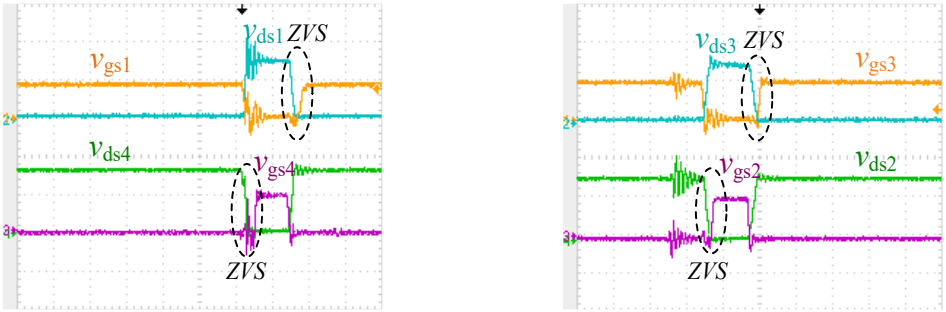
Fig. 4.13: Experimental results (Cases (I-III)). Voltage across switches (v_{ds}, 50 V/div) and respective gating signal to the switches (v_{gs}, 10 V/div).



(i) Case: IV



(ii) Case: V



(iii) Case: VI

Fig. 4.14: Experimental results (Cases (IV-VI)). Voltage across switches (v_{ds}, 50 V/div) and respective gating signal to the switches (v_{gs}, 10 V/div).

Table 4.2: Comparison of results.

Parameter	$V_{s(min)}$ = 40 V								
	Full-Load			Half-Load			10% of Full-Load		
	Cal.	Sim.	Exp.	Cal.	Sim.	Exp.	Cal.	Sim.	Exp.
V_o (V)	200	195.2	191.2	200	194.5	193.2	200	194.5	192.4
I_o (A)	1	0.976	0.96	0.5	0.486	0.48	0.1	0.097	0.096
$I_{s(r)}$ (A)	5.674	5.49	5.82	2.854	2.835	2.97	0.671	0.745	0.91
$V_{Cs(r)}$ (V)	50.3	48.63	48.58	25.3	25.07	25.97	5.955	6.428	6.54
δ (deg.)	179.9	178	174	169.9	164	161	168.4	144	137
% η	96.34	97.8	91.18	97.05	98.51	93.1	96.96	96.61	92.42
% η with ZVT	ZVT circuit is not activated as all the switches turn-on with ZVS with minimum input voltage								
Parameter	$V_{s(max)}$ = 80 V								
	Full-Load			Half-Load			10% of Full-Load		
	Cal.	Sim.	Exp.	Cal.	Sim.	Exp.	Cal.	Sim.	Exp.
V_o (V)	200	194.3	190.4	200	193.5	191.8	200	194.5	193
I_o (A)	1	0.971	0.97	0.5	0.483	0.48	0.1	0.097	0.098
$I_{s(r)}$ (A)	5.675	5.961	6.14	2.86	3.40	3.68	0.671	0.987	1.02
$V_{Cs(r)}$ (V)	50.3	49.51	52.6	25.3	25.48	27.46	5.95	4.39	6.63
δ (deg.)	89.99	89	88	89.55	75	74	89.41	43	39
% η (without ZVT)	92.5	96.73	87.11	90.19	95.94	88.52	67.1	90.42	74.62
% η (with ZVT)	96.19	97.42	90.04	96.87	97.24	91.2	96.77	91.6	88.89

Table 4.3: Power loss breakdown of the converter

Case	Turn-off (W)	Turn-on (W)	MOSFET Antiparallel diode (W)	MOSFET Conduction (W)	Output rectifier (W)	Transformer + Q loss (W) (assumed 1%)	Total Loss (W)
I	0.077	0	0.131	2.832	2.25	2	7.302
II	0.037	0	0.061	0.718	1.125	1	2.941
III	0.024	0	0.119	0.039	0.225	0.2	0.608
IV	0.405	7.267	0.131	2.832	2.25	2	14.887
V	0.221	6.67	0.061	0.718	1.125	1	9.803
VI	0.061	6.21	0.119	0.039	0.225	0.2	6.80

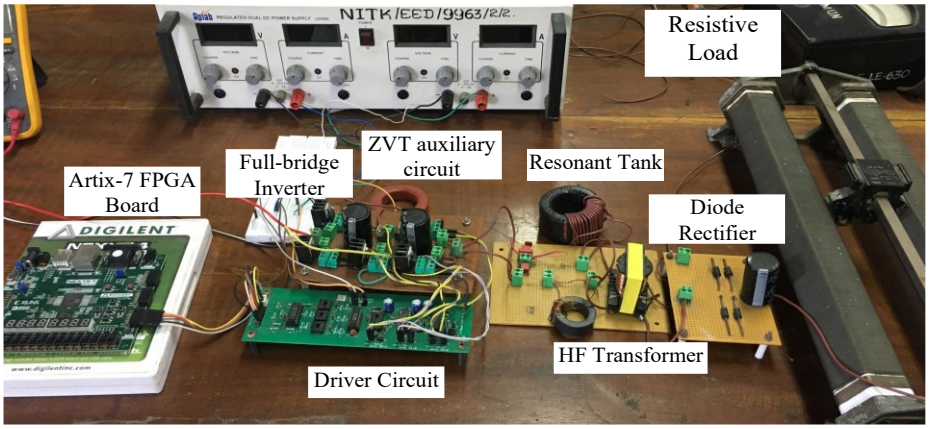


Fig. 4.15: Photograph of experimental setup of full bridge ZVT CLL resonant DC-DC converter.

4.7 Conclusion

The analysis and design of the full bridge ZVT CLL resonant DC-DC converter operating with the modified PWM gating scheme is presented. Approximate ac circuit analysis method is used in the steady-state analysis of the proposed converter. The optimum design of the converter is described with the help of design curves. The performance of the proposed converter with modified PWM gating scheme control is studied with PSIM simulations and by building a 200W converter in the laboratory. It is shown that the converter operates with ZVS for all the switches for the entire variations in loading and input voltage conditions. The secondary side rectifier diodes operate with ZCS. Hence, this converter is a good choice for applications involving fluctuating power which is typical of a renewable energy source. The theoretical, simulation and experimental results are presented and discussed.

Chapter 5

ANALYSIS AND DESIGN OF THREE PHASE INTERLEAVED FULL BRIDGE CLL RESONANT CONVERTER OPERATED WITH FIXED FREQUENCY MODIFIED PWM GATING CONTROL

A three-phase interleaved CLL resonant DC-DC converter operated with fixed frequency modified PWM gating scheme is presented in this chapter. The interleaving operation of the resonant converter achieves higher power level, low output ripple current, high conversion efficiency and the operation of the converter at high-frequency achieves high power density. The three identical full bridges with CLL resonant tank on the primary side of high-frequency (HF) transformer are connected in parallel. The operating modes of the converter for different intervals are described with the help of key operating waveforms. The steady state analysis of the converter is carried out by using fundamental harmonic approximation approach and the design procedure is explained. The PSIM simulations are carried out to substantiate calculated predictions of the converter for various operating conditions.

5.1 Introduction

The recent developments in renewable energy technology is leading to large power generation by way of establishing renewable energy plants. Hence, there is need for finding a DC-DC power converter that is capable of handling medium to high level power with higher efficiency and good reliability. In conventional single-phase DC-DC converters, the current rating will be limited due to component and device stress, and

large or parallel output capacitors are needed in high power applications**.** And also, the failure of any component or device in the converter will stop the power being transfer to the load leading to interruption of power supply. Therefore, interleaved connection of 1-phase converters is introduced (Chien et al. 2012; Hu et al. 2014b; Lin and Cheng 2013; Moon et al. 2015; Murata and Kurokawa 2016; Sun et al. 2015; Wu et al. 2017b; Zhang et al. 1998). In the interleaved configuration, the current can be divided and shared among the different modules/phases reducing the current stress, thermal stress and conduction losses. The problem of large size or paralleling of output capacitor filter in the conventional single-phase structure to satisfy output voltage and current ripple can be overcome by interleaving or multi-phasing. Due to ripple cancellation effect in interleaved or multiphase converters, the output ripple current is lowered resulting in reduced size of output capacitor (Hu et al. 2014b; Lin and Chiang 2007; Sato et al. 2016; Zhang et al. 1998). Hence, interleaved or multi-phase resonant DC-DC converters are employed for medium to high power applications (Chien et al. 2012; Huang et al. 2019; Lin and Cheng 2013; Moon et al. 2015; Sun et al. 2015). The additional advantage of the three-phase interleaved converter is that, the converter is able to supply the part-load in the case of failure of component or device of any of the modules, which ensures continuity of the power supply.

In 3- phase interleaved converters, the gating signals between the paralleled module structures are given with 120° phase-shift from each other respectively. This scheme can be expanded to interconnect 'n' number of such 1-phase converter modules in parallel configuration applied with gating signals to the inverter bridges of each module phase-shifted by $(360/n)°$ respectively to realize multi-phase converter operation for medium to high power ratings.

The variable frequency control of interleaved resonant converter requires all the parallel structures of the converter to be operated at the synchronized frequency (Murata and Kurokawa 2016; Wu et al. 2017b). However, this frequency control of the interleaved converter leads to complexity in designing the filters and magnetics of the converter and the effective use of the parasitic components becomes difficult. Additionally, frequency control over wide range increases EMI in the converter. Thus,

interleaved converter with fixed frequency gating scheme is favored to overcome these difficulties. In order to have higher efficiency, reliability and robust operation of the interleaved converter, the MOSFET switches of the full-bridge should be operated with ZVS. It is difficult to have ZVS for all the switches at light-load or maximum input voltage conditions, as the energy stored in leakage inductor is insufficient. This limits the ZVS range (Jang and Jovanović 2004; Shi et al. 2018; Yoon et al. 2006) of the converter. The 1-phase resonant converter applied with fixed frequency phase-shift gating scheme offers ZVS to all the switches for wide variations in load at minimum input voltage but loses ZVS for two switches of the full-bridge converter at maximum input voltage conditions (Gautam et al. 2013; Kong and Khambadkone 2007; Shi et al. 2018; Wu et al. 2015). The 3-phase interleaved resonant converter with three module structure of full-bridge applied with phase-shift gating scheme (Almardy and Bhat 2019; Kim et al. 2014), loses ZVS of six switches (two switches in each module) of the converter when applied with maximum input voltage. The modified PWM gating scheme (Harischandrappa and Bhat 2014) provides ZVS to all the switches of 1-phase full-bridge resonant converter when applied with minimum input voltage and only one switch in a full bridge loses ZVS when applied with maximum input voltage for variations in loading conditions.

The 3-phase interleaved full bridge CLL resonant DC-DC converter applied with fixed frequency modified PWM gating scheme is proposed. The proposed converter provides ZVS to all the switches of the converter for wide variations in loading conditions. While only one switch loses ZVS in each module/bridge of the interleaved converter at maximum input voltage conditions which is advantageous as compared to the normal phase-shift gating scheme applied to the converter where, two switches in each module of interleaved structure loses ZVS. Also, the rectifier diodes at the secondary side operate with ZCS reducing reverse recovery losses.

In this chapter, a modified gating signal controlled 3-phase interleaved full bridge CLL resonant DC-DC converter with capacitive output filter is presented and the performance of the converter is analysed. The organization of the chapter is as following. The interleaved operation of the proposed converter is explained with the

key waveforms and equivalent circuit diagrams in Section 5.2. The detailed steady state analysis and the design procedure are given in Section 5.3. Section 5.4 describes the performance of the converter with theoretical and simulation results. Section 5.5 draws the conclusion.

5.2 Circuit Configuration and Operation Principle

The schematic of the proposed 3-phase interleaved full bridge CLL resonant DC-DC converter is shown in Fig. 5.1. The structure of the proposed converter consists of three identical full bridge HF switched inverter, followed by CLL resonant network on the Y-connected primary side, and 3-phase rectifier on the Δ-connected secondary side of the HF transformer. A capacitive filter C_f is used before connecting the load to the output terminals of the 3-phase rectifier. The resonant network of each module of the converter comprises series resonant capacitor C_s, resonant inductors L_t and L_r connected across the inverter output terminals of all the three-phases. The series resonant capacitor avoids the saturation of the transformer core by blocking DC component.

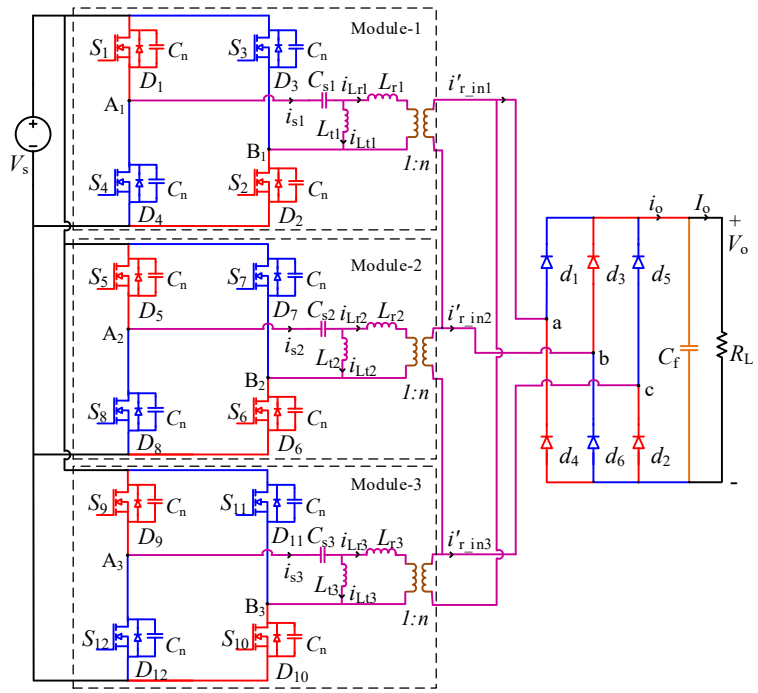


Fig. 5.1: Three-phase interleaved full bridge CLL resonant DC-DC converter.

The key operating waveforms along with the fixed frequency modified PWM gating scheme of the proposed converter is shown in Fig. 5.2. The width of gating signal of the switches S_1 and S_3 is increased by an angle 'α' and for the switches S_2 and S_4 the width of gating pulse is reduced by the same angle 'α' as shown in Fig. 5.2. By varying the angle 'α', the pulse-width of the inverter output voltage is varied to regulate the output voltage V_o for the variations in input voltage and loading conditions. The gating signals applied to the full bridge inverter of each module are respectively phase shifted by 120° from one another. The converter is made to work in above resonance mode or lagging power factor mode to achieve ZVS turn-on of the inverter switches. It can be seen in Fig. 5.2 that, the resonant current i_{s1} is lagging the inverter output voltage v_{A1B1} depicting the lagging power factor mode. The rectifier input current i_{r_in1} describes the diode conducting in the 3-phase rectifier. In the same manner, notations i_{s2}, v_{A2B2}, i_{r_in2} of the second bridge and i_{s3}, v_{A3B3}, i_{r_in3} of the third bridge are denoted.

All the main switches of the three full-bridge inverters turn-on with ZVS when applied with minimum input voltage for entire variations in load. But when maximum input voltage is applied, the pulse-width 'δ' decreases significantly resulting in only one switch losing ZVS in each full-bridge as against two switches with normal 180^o wide gating signals. The diodes in 3-phase rectifier are operated with ZCS resulting in minimized turn-off losses.

The operation of the converter is described in two major modes:

(i) Mode I (Operation with minimum input voltage):

(ii) Mode II (Operation with maximum input voltage):

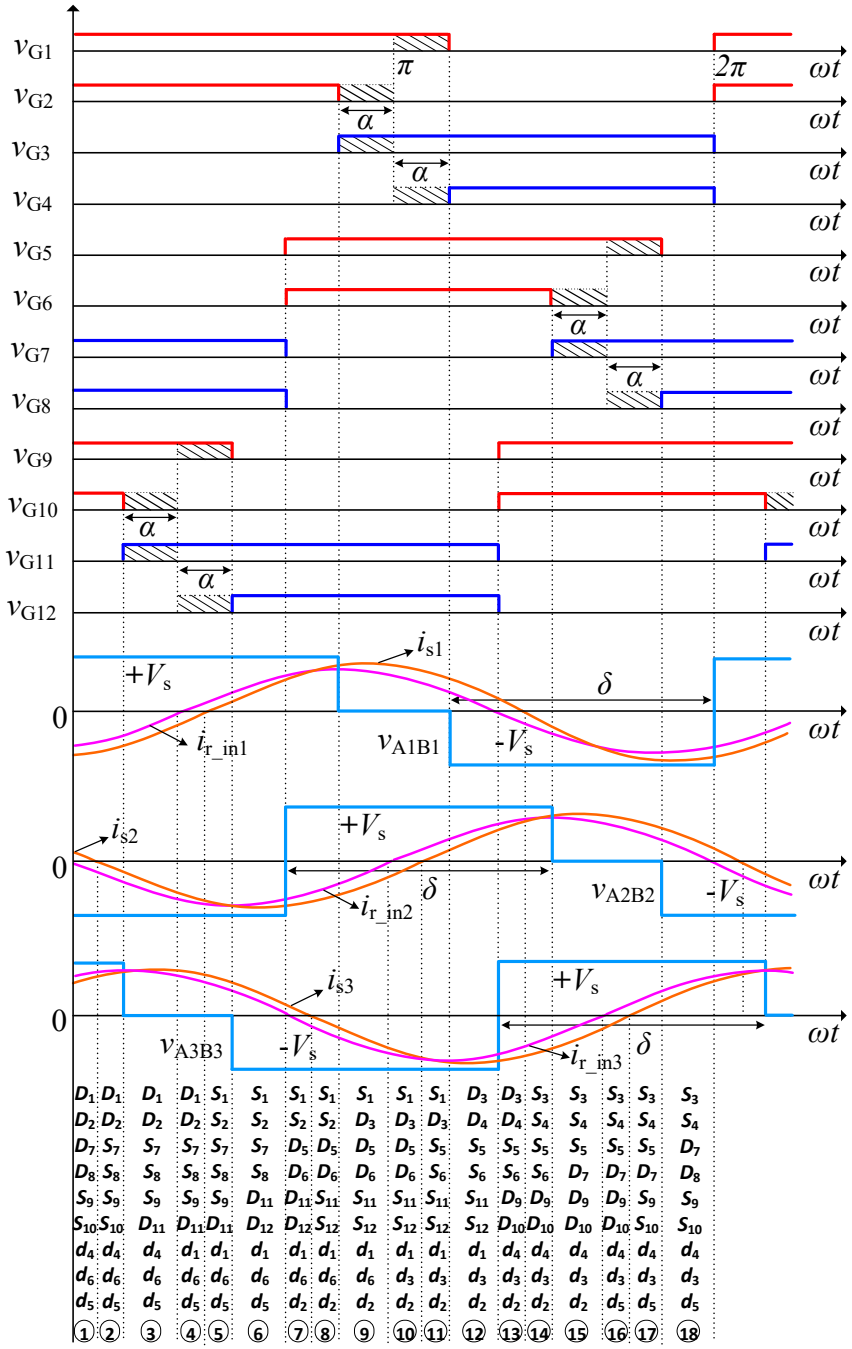


Fig. 5.2: The key operating waveforms along with the modified PWM gating scheme of Mode-I operation.

(i) ***Mode I (Operation with minimum input voltage):***

The devices of the converter conducting during different states of operation in Mode I is depicted in Fig 5.2. The converter is operated in lagging power factor mode as the resonant current i_s lags the inverter output voltage in each bridge of the three-phase structure of the converter. Hence, all the switches of the converter are turned-on with ZVS. In one cycle of switching period, the operation of the converter is included with 18 different states/intervals. The conduction of devices in first half cycle and second half cycle of the switching period are symmetrical. The operation of the converter for the first half cycle of the switching period is explained with equivalent circuit diagrams as shown in Fig. 5.3.

State 1 *[Fig. 5.3(a)]*: During this state 1, antiparallel diodes D_1, D_2, D_7 and D_8 of the respective switches S_1, S_2, S_7 and S_8 of bridge/module I and II are conducting carrying negative current i_{s1} and positive current i_{s2} respectively. Switches S_9 and S_{10} of bridge III are conducting carrying positive current i_{s3}. The secondary rectifier diodes d_4, d_5, d_6 are conducting supplying the load. This state ends when the current i_{s2} reaches zero.

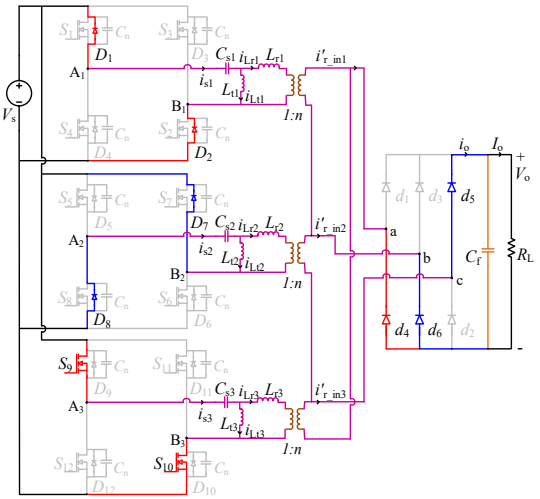
State 2 *[Fig. 5.3(b)]*: In this state, the current i_{s2} goes negative making switches S_7 and S_8 to turn-on and antiparallel diodes D_7 and D_8 to turn-off. Here, switches S_7 and S_8 turn-on with ZVS as the respective antiparallel diodes D_7 and D_8 were in conduction before the switches conduct. All other devices remain conducting same as in state 1.

State 3 *[Fig. 5.3(c)]*: The gating pulse to switch S_{10} is removed and it stops conducting, antiparallel diode D_{11} with S_9 conducts carrying positive current i_{s3} in freewheeling mode.

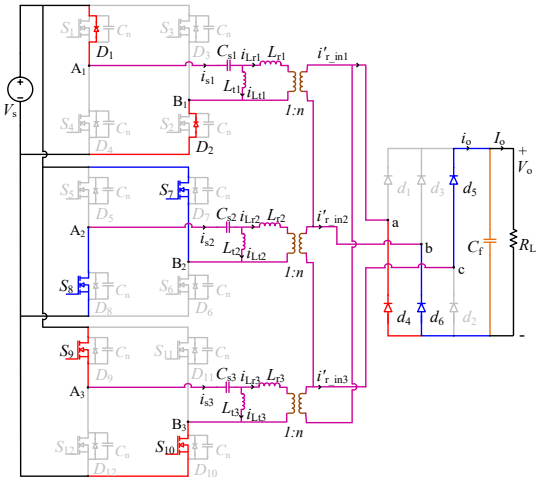
State 4 *[Fig. 5.3(d)]*: At the start of this state, the current i_{r_in1} goes positive making secondary output rectifier diode d_4 off and d_1 start conducting. Other rectifier diodes and switches remain the same conducting as in the previous state.

State 5 *[Fig. 5.3(e)]*: In this state, the current i_{s1} goes positive making switches S_1 and S_2 to turn-on and antiparallel diodes D_1 and D_2 to turn-off. Here, switches S_1 and S_2

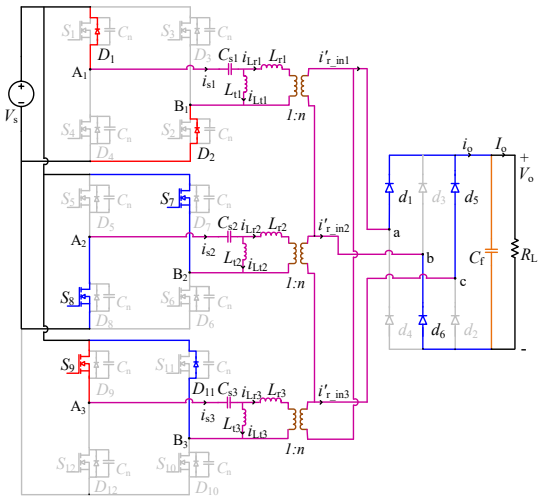
turn-on with ZVS as the respective antiparallel diodes D_1 and D_2 were in conduction before the switches conduct.



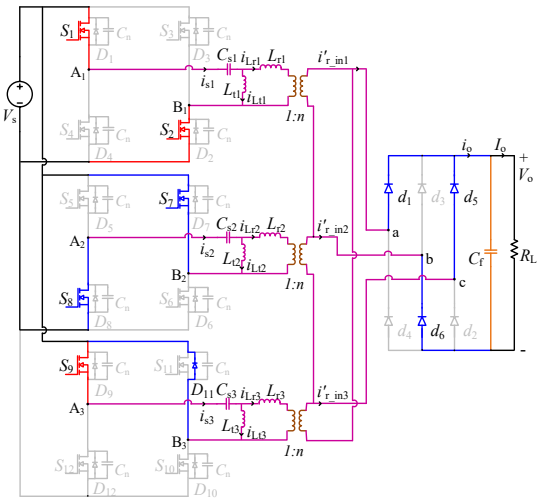
(a) State 1



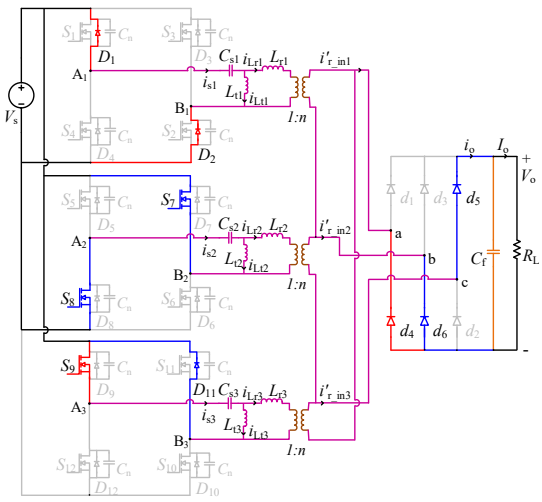
(b) State 2



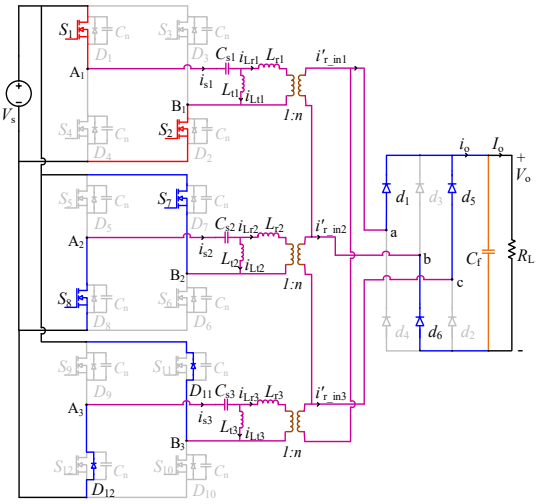
(c) State 3



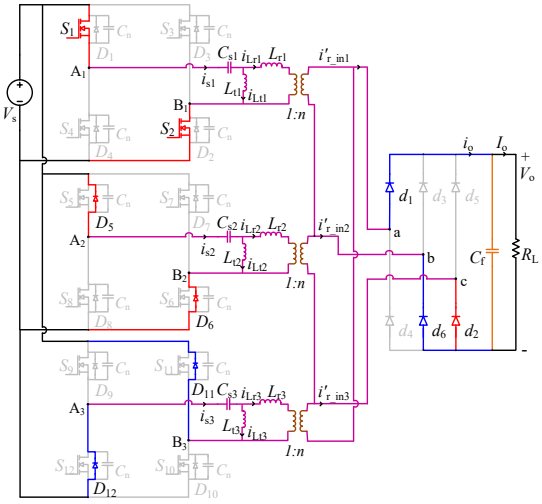
(d) State 4



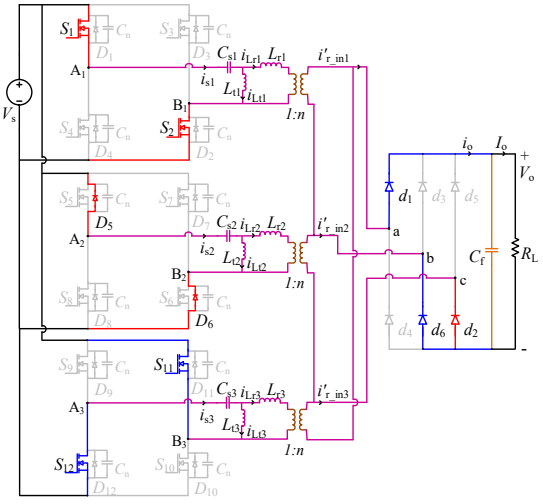
(e) State 5



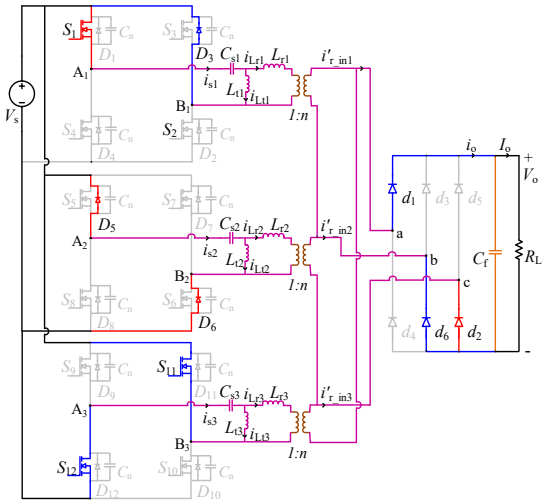
(f) State 6



(g) State 7



(h) State 8



(i) State 9

Fig. 5.3: Equivalent circuit for different operating states of Mode I operation.

State 6 *[Fig. 5.3(f)]*: Now the gating signal to switch S_9 is removed and it is turned-off. Antiparallel diodes D_{11} and D_{12} conduct maintaining the same direction of current i_{s3}. All other devices conduct same as in the previous state.

State 7 *[Fig. 5.3(g)]*: In this state, the gating signal to switches S_7 and S_8 is removed and the switches are turned-off. As the direction of current i_{s2} remains same, antiparallel diodes D_5 and D_6 start to conduct connecting with the input power supply. The current i_{r_in3} goes negatives making secondary output rectifier diode d_5 off and d_1 start conducting. The current i_{s3} becomes zero at the end instant of this state.

State 8 *[Fig. 5.3(h)]*: As the current i_{s3} goes negative making switches S_{11} and S_{12} to turn-on and antiparallel diodes D_{11} and D_{12} to turn-off. Here, switches S_{11} and S_{12} turn-on with ZVS as the respective antiparallel diodes D_{11} and D_{12} were in conduction before the switches conduct.

State 9 *[Fig. 5.3(i)]*: The gating signal to the switch S_2 is removed at the instant of start of this state and the switch is turned-off. The diode D_3 comes into conduction maintaining the same direction of current i_{r1}. The current i_{r_in2} goes zero at the end of this state.

(ii) ***Mode II*** (Operation with maximum input voltage):

The devices of the converter conducting during different states/intervals of operation in Mode II is depicted in Fig. 5.4. When the maximum input voltage is applied, there is a significant reduction in pulse-width 'δ' to regulate the output voltage and the converter is not operated in lagging power factor mode in each bridge/module of the three-phase structure of the converter. Hence, one switch in each bridge of the converter is turned-on without ZVS. In one cycle of the switching period, the operation of the converter is included with 21 different states. The conduction of devices in the first 11 states has been explained with the equivalent circuit diagrams as shown in Fig. 5.5 and other states of switching period are symmetrical.

State 1 *[Fig. 5.5(a)]*: During this state, D_1, D_2 of module I and S_7, D_5 of module II are conducting with negative current i_{s1} and i_{s2} respectively. Switch S_9 and diode D_{11} conducts carrying current i_{s3} in positive direction. The secondary rectifier diodes d_4, d_5 and d_6 are conducting supplying the load.

State 2 *[Fig. 5.5(b)]*: The gating signal is given to the switch S_8 at the start of this state. The switch S_8 turn-on without ZVS as there is no respective antiparallel diode conducting before switch S_8 conducts. The switches S_8 and S_9 are conducting keeping the same direction of current i_{s2} as in the previous state.

State 3 *[Fig. 5.5(c)]*: The current i_{r_in1} goes positive making secondary output rectifier diode d_4 off and d_1 start conducting. Other rectifier diodes and switches remain the same conducting as in the previous state.

State 4 *[Fig. 5.5(d)]*: In this state, the current i_{s1} goes positive making switches S_1 and S_2 to turn-on and antiparallel diodes D_1 and D_2 to turn-off. Here, switches S_1 and S_2 turn-on with ZVS as the respective antiparallel diodes D_1 and D_2 were in conduction before the switches conduct. And all other devices conduct same as in the previous state.

State 5 *[Fig. 5.5(e)]*: At the start of this state, the current i_{r_in3} goes negative making secondary output rectifier diode d_5 off and d_2 starts conducting. Other rectifier diodes and switches remain the same conducting as in the previous state.

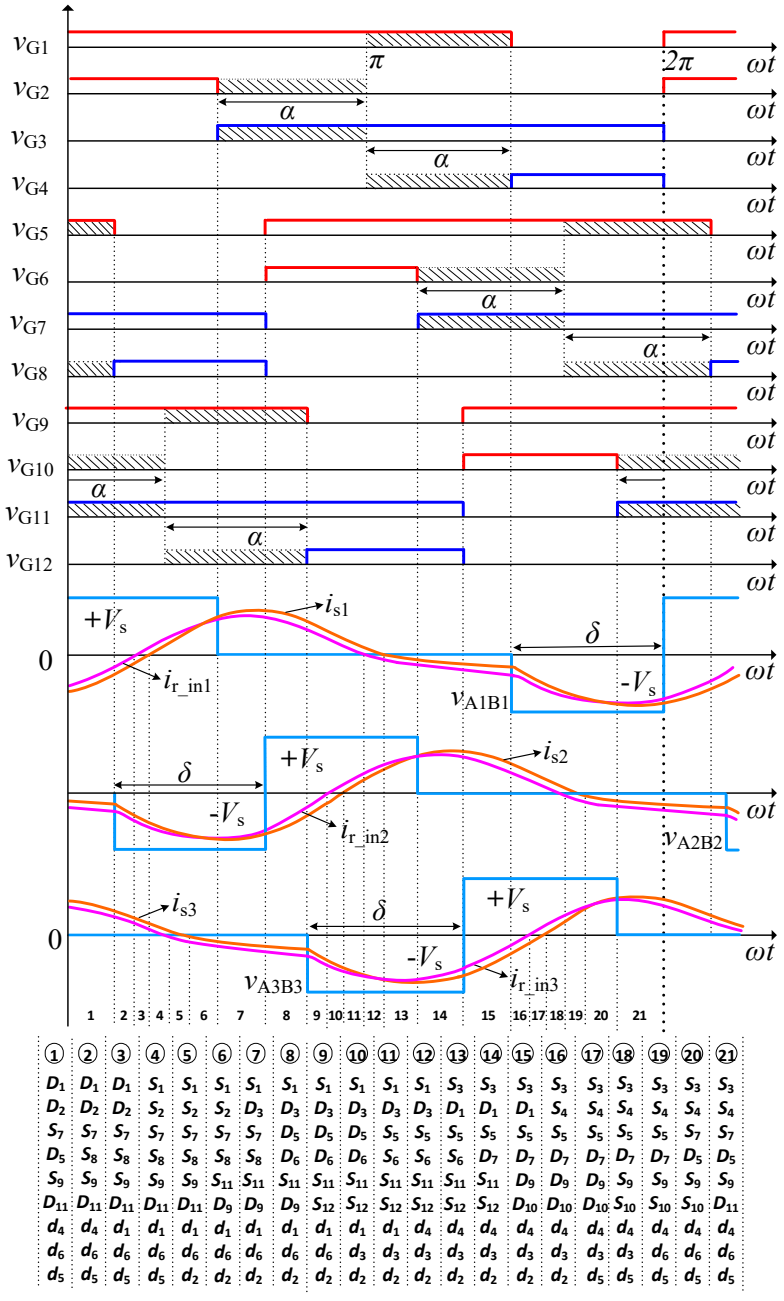
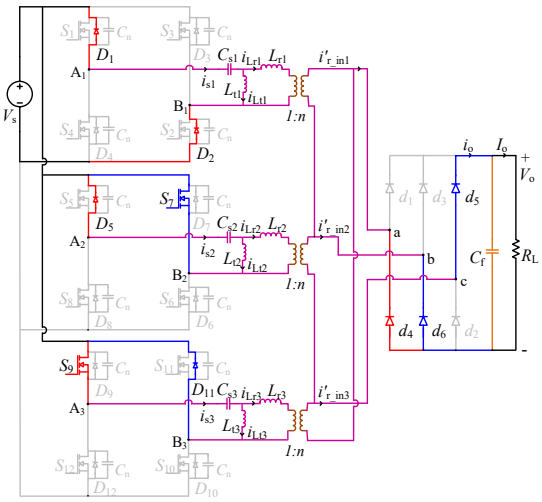
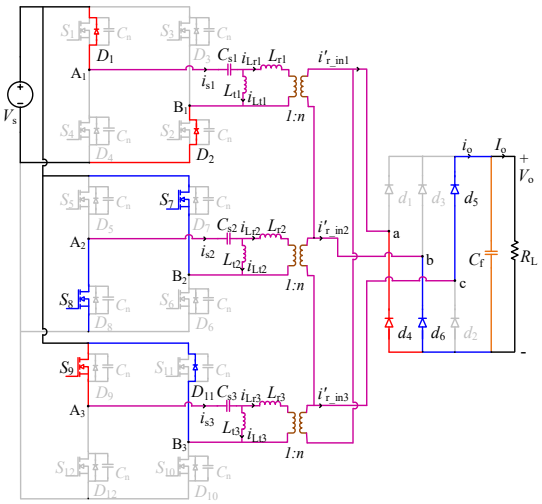


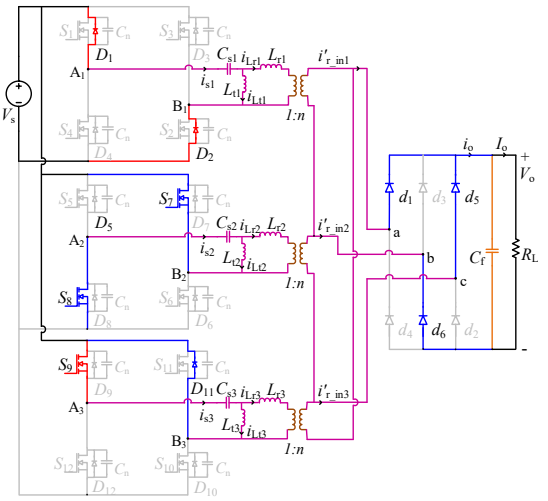
Fig. 5.4: The key operating waveforms along with the modified PWM gating scheme of Mode-II operation.



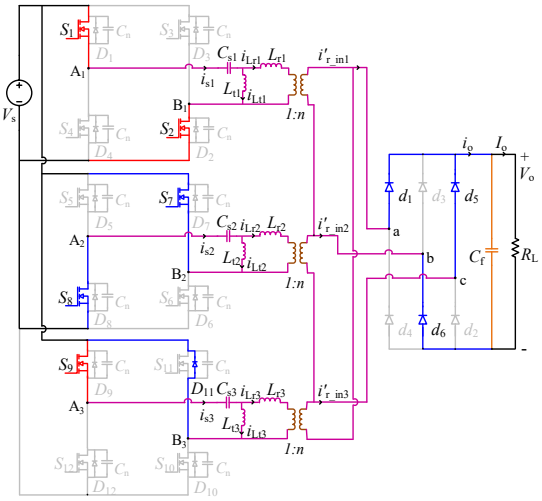
(a) State 1



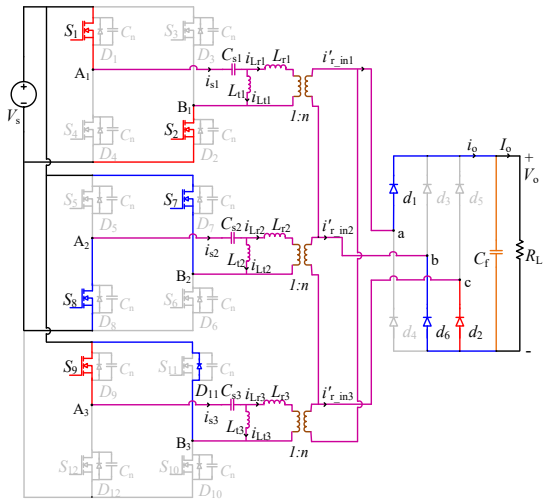
(b) State 2



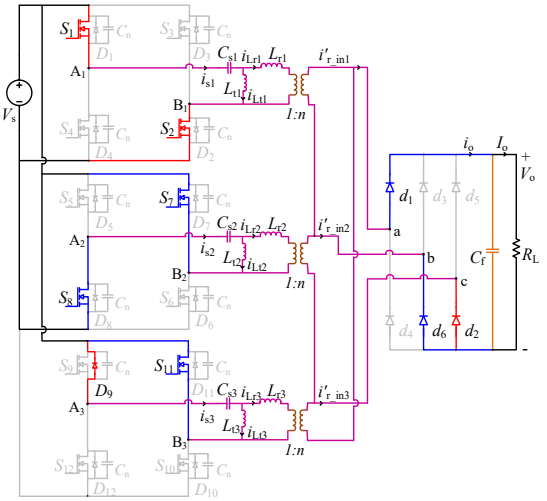
(c) State 3



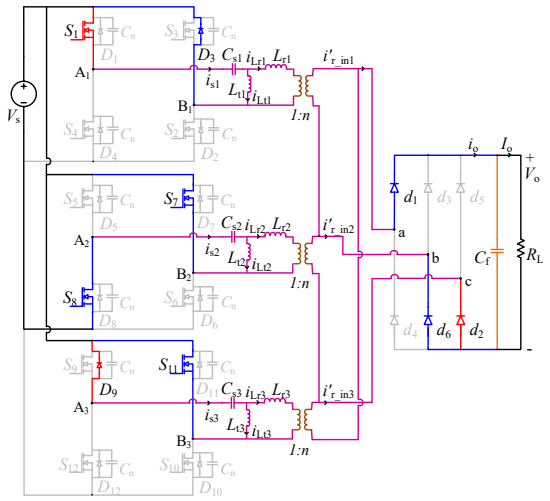
(d) State 4



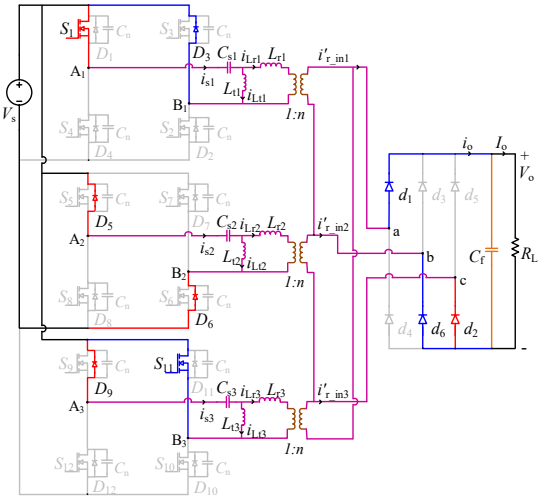
(e) State 5



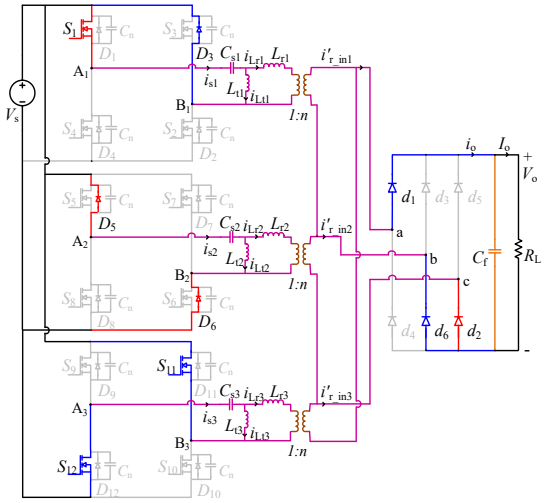
(f) State 6



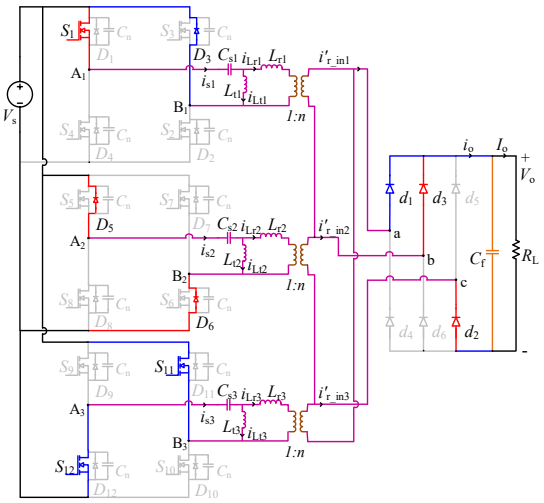
(g) State 7



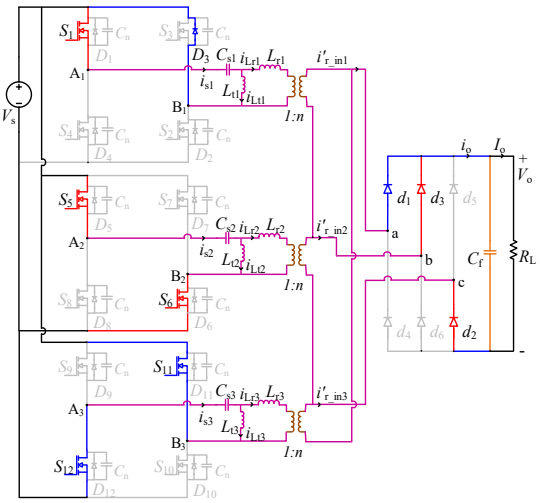
(h) State 8



(i) State 9



(j) State 10



(k) State 11

Fig. 5.5: Equivalent circuit for different operating states of Mode II operation.

State 6 *[Fig. 5.5(f)]*: The current i_{s3} goes negative in freewheeling mode making switch S_{11} and D_9 to conduct. As there is no respective antiparallel diode conducting before the switch S_{11} conducts, only switch S_{11} of the bridge III turn-on without ZVS.

State 7 *[Fig. 5.5(g)]*: The gating signal to switch S_2 is removed and made to turn-off.

Antiparallel diode D_3 comes into conduction keeping the same direction of current i_{s1}. All other devices remain to conduct same as in the previous state.

State 8 *[Fig. 5.5(h)]*: At the start of this state, gating signals to switches S_7 and S_8 are removed and the switches are turned-off. As the direction of current i_{s2} remains same, antiparallel diodes D_5 and D_6 start to conduct connecting with the input power supply.

State 9 *[Fig. 5.5(i)]*: The gating signal to switch S_{12} is given and made to turn-on. As the antiparallel diode D_{12} is not conducting before S_{12} conducts, switch S_{12} turn-on without ZVS. All other devices conduct same as in the previous state.

State 10 *[Fig. 5.5(j)]*: The current i_{r_in3} goes positive making secondary output rectifier diode d_6 off and d_3 start conducting. The current i_{s2} becomes zero at the end instant of this state.

State 11 *[Fig. 5.5(k)]*: In this state, the current i_{s2} goes positive making switches S_5 and S_6 to turn-on and antiparallel diodes D_5 and D_6 to turn-off. Here, switches S_5 and S_6 turn-on with ZVS as the respective antiparallel diodes D_5 and D_6 were in conduction before the switches conduct.

5.3 Analysis and Design Procedure

The following assumptions are made in the modeling and analysis of the proposed converter:

(i) The diodes, switches, capacitors and inductors used are ideal.

(ii) The output and input voltages are assumed to be constant without any ripple.

(iii) The three-phases/modules are identical and the three-phase interleaved circuit is balanced.

(iv) The following relations are considered: $L_{r1} = L_{r2} = L_{r3} = L_r$, $L_{t1} = L_{t2} = L_{t3} = L_t$, $C_{s1} = C_{s2} = C_{s3} = C_s$.

(v) The snubber capacitors effect is neglected.

5.3.1 Modeling of the Converter

The 3-phase interleaved CLL resonant converter with capacitive output filter shown in Fig. 5.1 is modeled to analyse for only one module/phase as all the three-phases are identical. The inverter output voltage of full bridges v_{A1B1}, v_{A2B2} and v_{A3B3} are square waveform for full-load and quasi square wave for reduced loading conditions. The rectifier input voltages v_{ab}, v_{ba}, v_{ca} are also considered as a quasi square wave with pulse-width angle 'δ'. Since all the three-phases are similar, it is sufficient to analyse per phase equivalent circuit at the inverter output terminals A_1B_1. The per-phase equivalent circuit described in Chapter-3 is extended for modeling the proposed 3-phase interleaved CLL resonant converter as shown in Fig. 5.6(a). To simplify the analysis, only, the fundamental component of voltages and currents is considered. All the parameters on secondary side of HF transformer are referred on primary side. The rectifier, output capacitive filter and load are transferred to primary side as an equivalent ac resistance R_{ac}. Equivalent circuit of the converter for one of the three-phases of the converter is shown in Fig. 5.6(b).

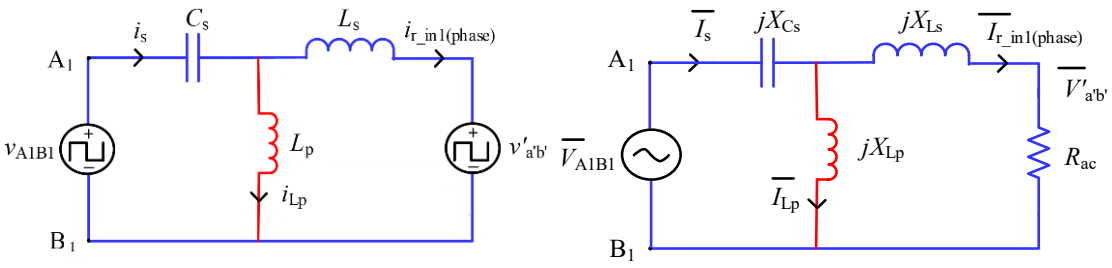


Fig. 5.6: Equivalent circuit (a) Per phase equivalent circuit referring all the parameters to primary side of HF transformer. (b) Phasor equivalent circuit of the converter for one of the three-phases of the converter. Where, $X_{LS} = \omega_s L_s$, $X_{LP} = \omega_s L_p$, $X_{CS} = -\frac{1}{\omega_s C_s}$.

5.3.2 Converter Analysis

The fundamental harmonic approximation approach is used for the steady state analysis of the converter. The rectifier input voltage $v_{a'b'}$ is considered as quasi square wave with an amplitude of $\pm V'_o = \pm nV_o$ and the pulse-width angle equal to $2\pi/3$. The root mean square value of fundamental component of $v_{a'b'}$ is obtained as,

$$v_{a'b'(\mathrm{rms})} = \frac{\sqrt{6}\, V'_o}{\pi} \tag{5.1}$$

The rectifier input current referred to primary side as i_{r_in1}, i_{r_in2}, i_{r_in3} are assumed approximately as sinusoidal. The root mean square value of fundamental component of rectifier input current i_{r_in1} is obtained as,

$$I_{r\_in1} = \left(\frac{\pi}{3\sqrt{2}}\right) I'_o \tag{5.2}$$

The root mean square value of fundamental component of rectifier input current per phase $i_{r\_in1(phase)}$ is obtained as,

$$I_{r\_in1(phase)} = \left(\frac{\pi}{\sqrt{6}}\right) I'_o \tag{5.3}$$

The equivalent ac resistance R_{ac} shown in Fig. 5.6(b) is obtained from (5.1) and (5.3) as,

$$R_{ac} = \frac{V_{a'b'}}{I_{r\_in1(phase)}} = \left(\frac{18}{\pi^2}\right) R'_L \tag{5.4}$$

The resonant frequency is defined as,

$$\omega_r = \frac{1}{\sqrt{L_e C_s}} \tag{5.5}$$

where, $L_e = \frac{L_p \,.\, L_s}{L_p + L_s}$

L_e is the approximated effective value at full-load condition of the parallel combination of L_s and L_p.

The RMS value of the fundamental component of inverter output voltage is,

$$V_{\mathrm{A1B1}} = \frac{\sqrt{2}}{\pi} V_{\mathrm{s}} (1 - \cos\delta) \tag{5.6}$$

Using the phasor equivalent circuit shown in Fig. 5.6(a) and (5.6), the converter gain is obtained as,

$$M = \frac{V_0'}{V_{\mathrm{s}}} = \frac{(1-cos\,\delta)/\sqrt{3}}{\left(1-\frac{K}{F^2(K+1)}\right)+j\frac{\pi^2}{18}Q\left(F(K+1)-\frac{K}{F}-\frac{1}{F}\right)} \tag{5.7}$$

Where, K is the inductance ratio ($K = L_{\mathrm{s}}/L_{\mathrm{p}}$), Q is the Quality factor,($Q = \omega_{\mathrm{r}} L_{\mathrm{e}}/R'_{\mathrm{L}}$) and F is the frequency ratio ($F = \omega_{\mathrm{s}}/\omega_{\mathrm{r}}$).

Equivalent circuit impedance across A_1B_1 of the Fig. 5.6(b) is obtained as,

$$Z_{\mathrm{A1B1}} = R_{\mathrm{A1B1}} + jX_{\mathrm{A1B1}} \tag{5.8}$$

The magnitude and phase of the equivalent circuit impedance across terminals A_1B_1 of Fig. 5.6(b) are given as,

$$|Z_{\mathrm{A1B1}}| = [R_{\mathrm{A1B1}}^2 + X_{\mathrm{A1B1}}^2]^{\frac{1}{2}} \tag{5.9}$$

where,

$$R_{\mathrm{A1B1}} = \frac{R_{\mathrm{ac}} \cdot (\omega_{\mathrm{s}} L_{\mathrm{p}})^2}{R_{\mathrm{ac}}^2 + (\omega_{\mathrm{s}} L_{\mathrm{s}} + \omega_{\mathrm{s}} L_{\mathrm{p}})^2} \tag{5.10}$$

$$X_{\mathrm{A1B1}} = \frac{R_{\mathrm{ac}}^2(\omega_{\mathrm{s}} L_{\mathrm{p}} - (1/\omega_{\mathrm{s}} C_{\mathrm{s}})) + X_{\mathrm{LP}}^2(\omega_{\mathrm{s}} L_{\mathrm{s}} - (1/\omega_{\mathrm{s}} C_{\mathrm{s}})) + (\omega_{\mathrm{s}} L_{\mathrm{s}})^2(\omega_{\mathrm{s}} L_{\mathrm{p}} - (1/\omega_{\mathrm{s}} C_{\mathrm{s}})) - 2\omega_{\mathrm{s}} L_{\mathrm{s}} . \omega_{\mathrm{s}} L_{\mathrm{p}} . (1/\omega_{\mathrm{s}} C_{\mathrm{s}})}{R_{\mathrm{ac}}^2 + (\omega_{\mathrm{s}} L_{\mathrm{s}} + \omega_{\mathrm{s}} L_{\mathrm{p}})^2} \tag{5.11}$$

The peak current through the switch is obtained as,

$$I_{\mathrm{sp}} = \frac{V_{\mathrm{A1B1(max)}}}{|Z_{\mathrm{A1B1}}|} \tag{5.12}$$

Then, the expression for current through the switch is,

$$i_s = I_{sp} \sin(\omega t - \phi) \tag{5.13}$$

where, $\phi = arctan\left(\frac{X_{A1B1}}{R_{A1B1}}\right)$

The peak voltage across the resonant capacitor C_s is given by,

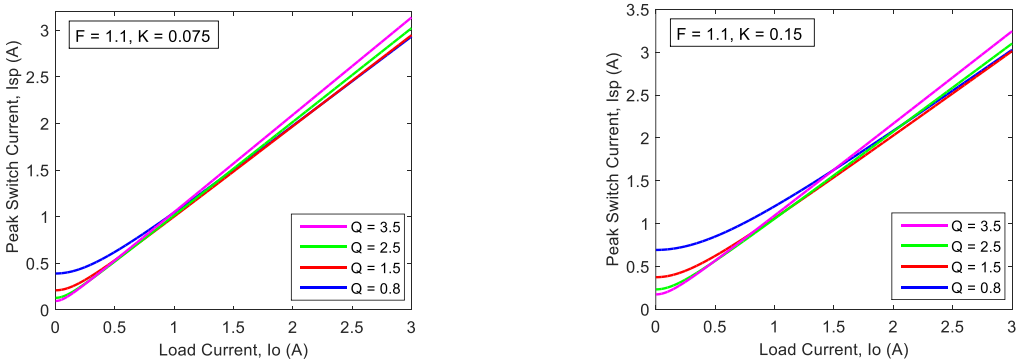
$$V_{Csp} = I_{sp} . X_{Cs} \tag{5.14}$$

5.3.3 Converter Design

The converter is designed for maximum duty cycle ($\delta = \pi$) with full-load and minimum input voltage operating conditions. By selecting from the graphical design curves, the converter design parameters are made optimized. The chosen parameters ensure a compact, reliable and good conversion efficiency of the converter. For the design of the converter, the severe operating condition of full-load and the minimum input voltage is considered. The necessary parameters that include frequency ratio *F*, inductor ratio *K* and full-load *Q* are chosen using the design curves shown in Figs. 5.7-5.9. The converter is made to operate in lagging PF mode by choosing *F* larger than 1 to achieve ZVS turn-on of the switches. The specifications of the converter are mentioned in Table 5.1.

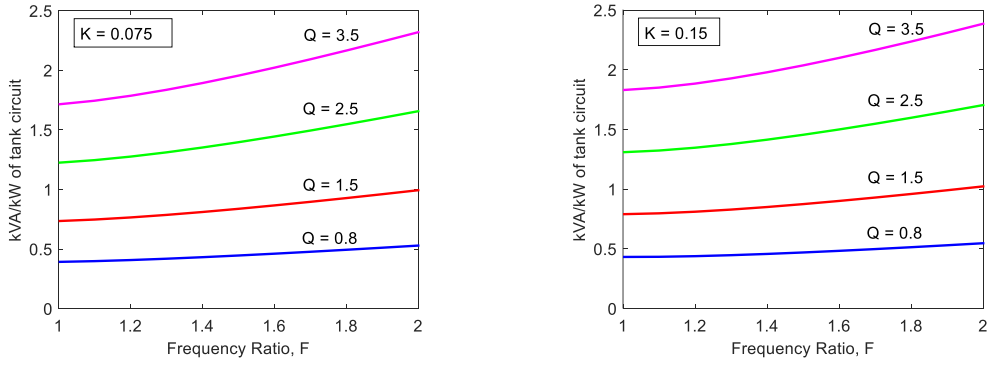
The variation of peak switch current I_{sp} with the load current is shown in Fig. 5.7. The I_{sp} reduces as the load current decreases and I_{sp} is also low for $K = 0.075$ [see Fig. 5.7(a)] as compared to $K = 0.15$ [see Fig. 5.7(b)]. Considering the low I_{sp} at full-load and light-load conditions $Q = 1.5$ is chosen. The kVA/kW of tank circuit versus frequency ratio *F* is shown in Fig. 5.8. The kVA/kW of the tank circuit reduces as the load current decreases and I_{sp} is also low for $K = 0.075$ [see Fig. 5.8(a)] as compared to $K = 0.15$ [see Fig. 5.8(b)]. Also, we can notice that as the value of kVA/kW of the tank circuit reduces with *Q* and *F*. Hence, $K = 0.075$ and $Q = 1.5$ is favorable and chosen as near optimum values. Fig 5.9(a) shows the variation in converter gain with the frequency ratio. The *F* is chosen as 1.1 to operate the converter in lagging PF mode. The plot of duty ratio versus load current is shown in Fig. 5.9(b). It is observed that the

output voltage is regulated from full-load to no-load for small variation in duty ratio. The selected parameters from the design i.e., K = 0.075, Q = 1.5, F = 1.1 are used in the calculation of converter gain from (5.7), i.e., M = 1.206. The output voltage referred to primary is, Vo' = 132.67 V. The turns ratio of the high-frequency transformer is calculated as, $n = Vo/Vo' = 1.507$. The load resistance R_L referred to the primary is, $R_L' = R_L/n^2 = 29.33\ \Omega$. From equations (5.4), (5.5) and (5.7), the values of the resonant tank elements are obtained as Cs = 0.03978 µF, Lp = 1.1 mH, Ls = 82.82 µH. The current and voltage stresses on the resonant tank elements are calculated by using (5.12)-(5.14).



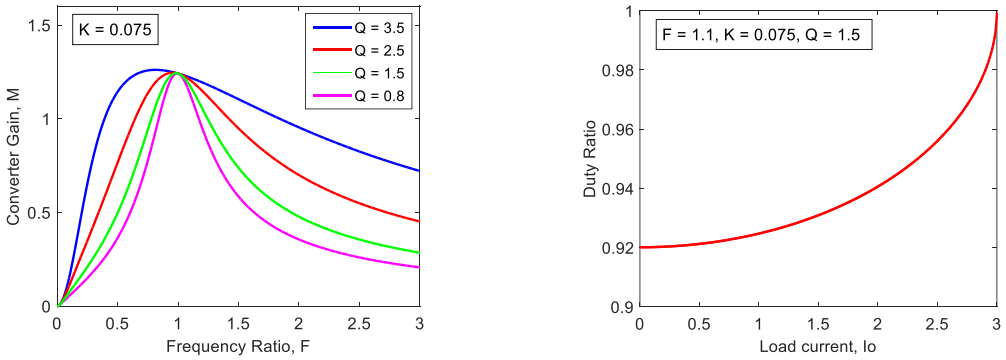
(a) (b)

Fig. 5.7: Peak switch current versus load current at constant output voltage for F = 1.1. (a) K = 0.075 for different values of Q. (b) K = 0.15 for different values of Q.



(a) (b)

Fig. 5.8: kVA/kW rating of tank circuit versus frequency ratio. For F = 1.1 and for different values of Q. (a) K = 0.075 (b) K = 0.15.



(a) (b)

Fig. 5.9: (a) Converter gain versus frequency ratio. (b) Duty ratio versus load current.

Table 5.1: Specifications of the converter

Power rating	600 W
Input DC voltage	110 -130 V
Output DC voltage	200 V
Switching frequency	100 kHz

5.4 Simulation Results

The high-frequency interleaved CLL resonant DC-DC converter analysed and designed in Section 5.3 is simulated by using the calculated values of components. The performance evaluation is done for the proposed converter with the PSIM simulation for various operating conditions when operated with modified PWM gating scheme.

The simulation results of the converter are obtained with minimum input voltage ($V_{s(min)}$ = 110 V) and maximum input voltage ($V_{s(max)}$ = 130 V) for two loading conditions i.e., full-load (FL) and 20% of FL when operated by modified PWM gating scheme shown in Figs. 5.10-5.14. The regulation of the output voltage is done by changing the pulse-width angle 'δ' for variations in input voltage and loading conditions. Some iterations are conducted to evaluate the value of 'δ' needed to keep the steady output voltage at its rated value. The ideal transformers and the MOSFETs

with $R_{DS(on)}$ = 0.15 Ω are considered in the simulation. The phase difference between the waveforms of the three modules of the converter in each operating condition is 120°.

The simulation results of the converter when applied with minimum input voltage ($V_{s(min)}$ = 110 V) at full-load condition is shown in Fig. 5.10. It is observed in Fig. 5.10(a) of (i)-(iii), the resonant current (i_{r1}, i_{r2}, i_{r3}) lags the inverter output voltage (v_{A1B1}, v_{A2B2}, v_{A3B3}) in all the three-phase modules illustrating lagging power factor mode and ensuring ZVS turn-on of the all the MOSFET switches. The current through and the respective voltage across the switches is shown in Fig. 5.10(b) of (i)-(iii), all the switches operate with ZVS turn-on as the antiparallel diode conducts before the respective switch start to conduct. The Fig. 5.11 shows the simulation waveforms at minimum input voltage ($V_{s(min)}$ = 110 V) at 20% of full-load. It is observed here also that the converter operates in lagging power factor mode as seen in Fig. 5.11(a) of (i)-(iii) and Fig. 5.11(b) of (i)-(iii) respectively indicates the ZVS turn-on of the switches. The converter is able to provide ZVS turn-on to all the switches when applied with minimum input voltage for variations in loading conditions.

The simulation results of the converter when applied with maximum input voltage ($V_{s(max)}$ = 130 V) at full-load condition operated is shown in Fig. 5.12. It is observed in Fig. 5.12(a) of (i)-(iii), the resonant current (i_{r1}, i_{r2}, i_{r3}) is not lagging the inverter output voltage (v_{A1B1}, v_{A2B2}, v_{A3B3}) i.e., the converter does not function in lagging power factor mode and hence one switch in each module of the proposed three-phase interleaved converter does not turn-on with ZVS. The current through and the respective voltage across the switches is shown in Fig. 5.12(b) of (i)-(iii), it is seen that only one switch in each module loses ZVS turn-on and all other switches of the converter turn-on with ZVS. The Fig. 5.13 shows the simulation waveforms at maximum input voltage ($V_{s(max)}$ = 130 V) at 20% of full-load. It is also observed in Fig. 5.13(a) of (i)-(iii) that the converter does not function in lagging power factor mode. Fig. 5.13(b) of (i)-(ii) indicates that only one switch in each module of the converter loses ZVS.

The power loss breakdown of the converter is given in Table 5.2 for the following cases: Case (I): $V_{s(min)}$ = 110 V and full-load; Case (II): $V_{s(min)}$ = 110 V and

20% of full-load; Case (III): $V_{s(max)}$ = 130 V and full-load; Case (IV): $V_{s(max)}$ = 130 V and 20% of full-load. The comparison of calculated and simulated results for different operating conditions is given in Table 5.3. It can be noticed that the resonant current decreases as the load is reduced which ensures good light-load efficiency. The converter operated with modified PWM gating scheme offers ZVS turn-on to all the switches when applied with minimum input voltage and however when applied with maximum input voltage, only one switch in each module of three-phase structure loses ZVS for wide variations in loading condition. This is advantageous as compared to the three-phase interleaved converter when operated with phase-shift gating scheme where two switches in each module of three-phase structure loses ZVS when applied with maximum input voltage. Hence, the proposed three-phase interleaved resonant converter operated with modified PWM gating scheme reduces switching losses which in-turn increases the efficiency of the converter.

Table 5.2: Power loss breakdown of the converter

Case	Turn-off (W)	Turn-on (W)	MOSFET Antiparallel diode (W)	Conduction (W)	Output rectifier (W)	Tfr. + Q loss (W) (assumed 1%)	Total Loss (W)
I	0.0439	0	0.2246	3.9044	7.5	18	29.6729
II	0.0138	0	0.1107	0.1749	1.5	3.6	5.3995
III	0.0996	36.9346	0.2246	3.9044	7.5	18	66.6633
IV	0.0237	36.3799	0.1107	0.1749	1.5	3.6	41.7893

i) Case I: $V_{s(min)}$ = 110 V, Full-Load

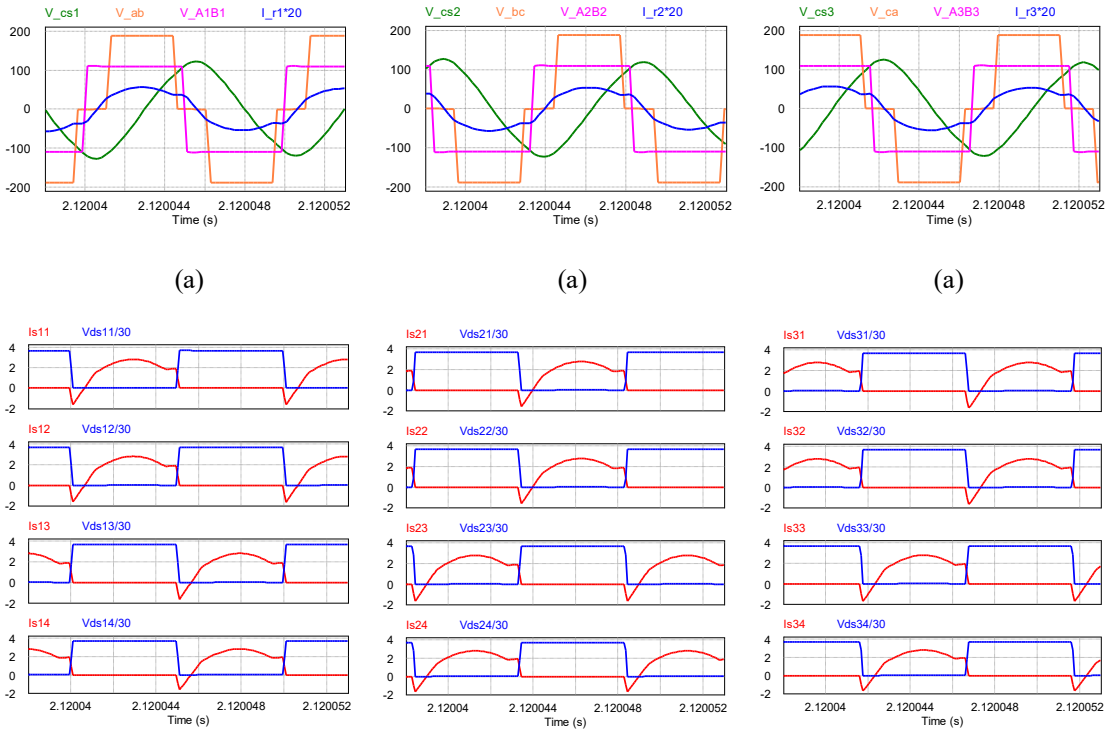


Fig. 5.10: PSIM simulation results for minimum input voltage $V_{s(min)}$ = 110 V for full-load condition, where, (a) resonant inductor currents i_{r1}, i_{r2}, i_{r3}; inverter output voltages v_{A1B1}, v_{A2B2}, v_{A3B3}; rectifier input voltages v_{ab}, v_{bc}, v_{ca}; resonant capacitor voltage v_{Cs1}, v_{Cs2}, v_{Cs3}. (b) voltage across the switches (v_{ds11}, v_{ds12}, v_{ds13}, v_{ds14}, v_{ds21}, v_{ds22}, v_{ds23}, v_{ds24}, v_{ds31}, v_{ds32}, v_{ds33}, v_{ds34}) and respective current through (i_{s11}, i_{s12}, i_{s13}, i_{s14}, i_{s21}, i_{s22}, i_{s23}, i_{s24}, i_{s31}, i_{s32}, i_{s33}, i_{s34}) switches $S_1 - S_{12}$.

ii) Case II: $V_{s(min)}$ = 110 V, 20% of Full-Load

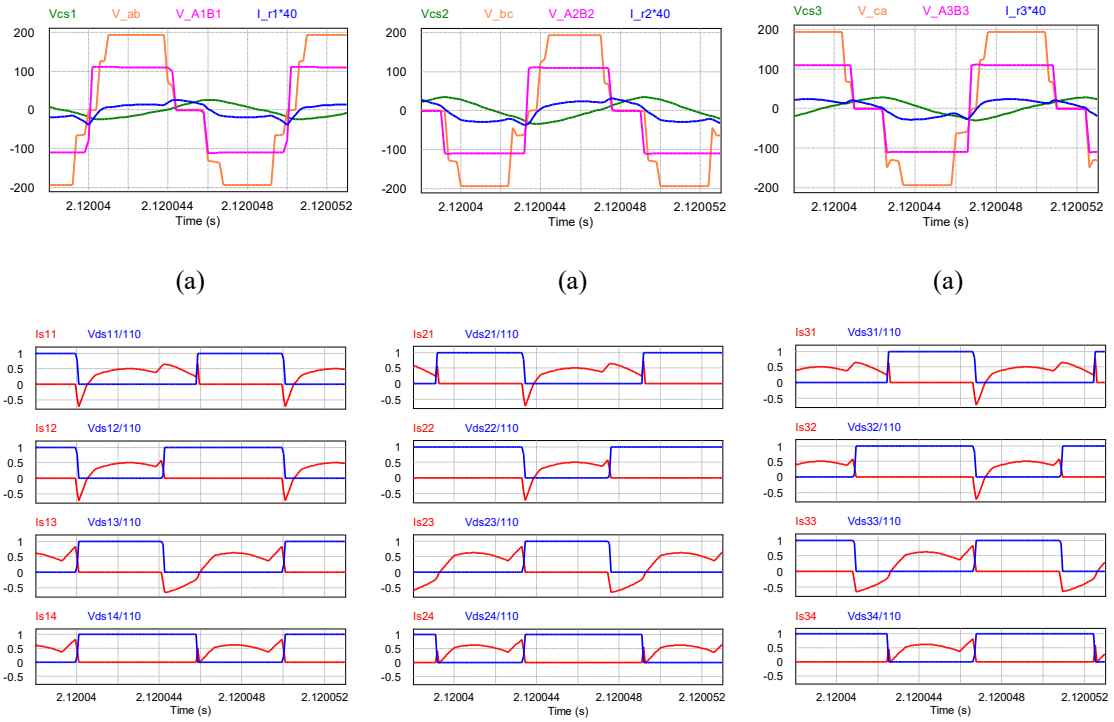


Fig. 5.11: PSIM simulation results for minimum input voltage $V_{s(min)}$ = 110 V for 20% of full-load condition, where, (a) resonant inductor currents i_{r1}, i_{r2}, i_{r3}; inverter output voltages v_{A1B1}, v_{A2B2}, v_{A3B3}; rectifier input voltages v_{ab}, v_{bc}, v_{ca}; resonant capacitor voltage v_{Cs1}, v_{Cs2}, v_{Cs3}. (b) voltage across the switches (v_{ds11}, v_{ds12}, v_{ds13}, v_{ds14}, v_{ds21}, v_{ds22}, v_{ds23}, v_{ds24}, v_{ds31}, v_{ds32}, v_{ds33}, v_{ds34}) and respective current through (i_{s11}, i_{s12}, i_{s13}, i_{s14}, i_{s21}, i_{s22}, i_{s23}, i_{s24}, i_{s31}, i_{s32}, i_{s33}, i_{s34}) switches S_1 – S_{12}.

(iii) Case III: $V_{s(max)}$ = 130 V, Full-Load

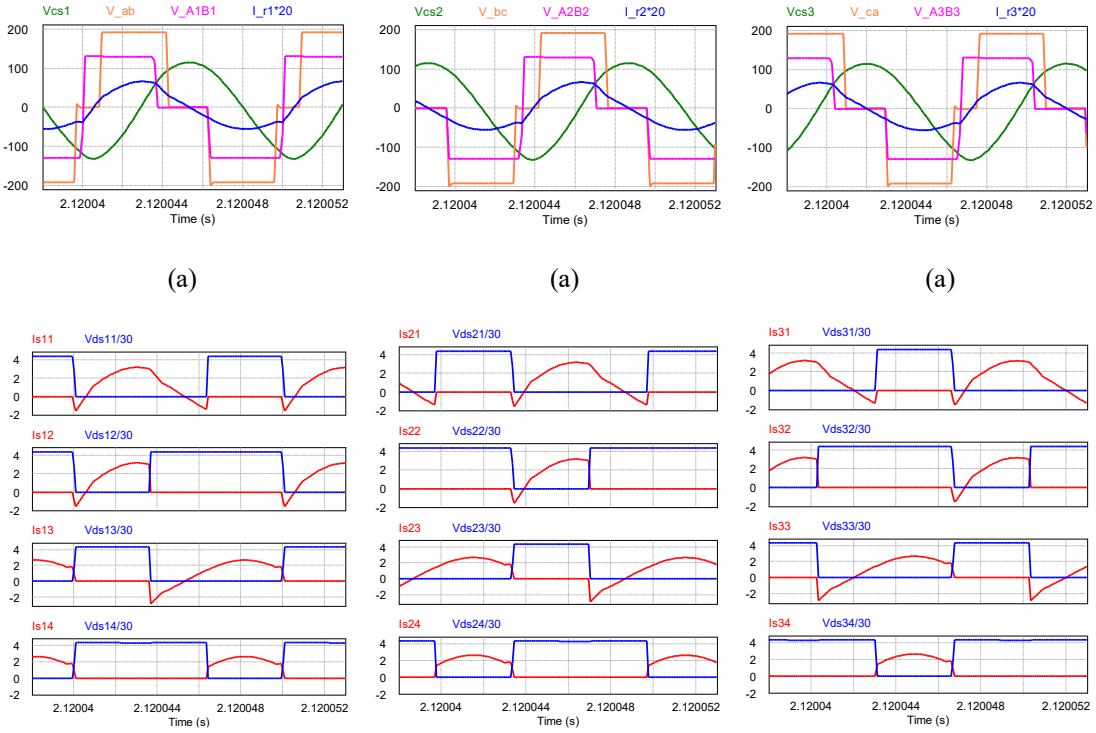


Fig. 5.12: PSIM simulation results for maximum input voltage $V_{s(max)}$ = 130 V for full-load condition, where, (a) resonant inductor currents i_{r1}, i_{r2}, i_{r3}; inverter output voltages v_{A1B1}, v_{A2B2}, v_{A3B3}; rectifier input voltages v_{ab}, v_{bc}, v_{ca}; resonant capacitor voltage v_{Cs1}, v_{Cs2}, v_{Cs3}. (b) voltage across the switches (v_{ds11}, v_{ds12}, v_{ds13}, v_{ds14}, v_{ds21}, v_{ds22}, v_{ds23}, v_{ds24}, v_{ds31}, v_{ds32}, v_{ds33}, v_{ds34}) and respective current through (i_{s11}, i_{s12}, i_{s13}, i_{s14}, i_{s21}, i_{s22}, i_{s23}, i_{s24}, i_{s31}, i_{s32}, i_{s33}, i_{s34}) switches $S_1 - S_{12}$.

(iv) Case IV: $V_{s(max)}$ = 130 V, 20% of Full-Load

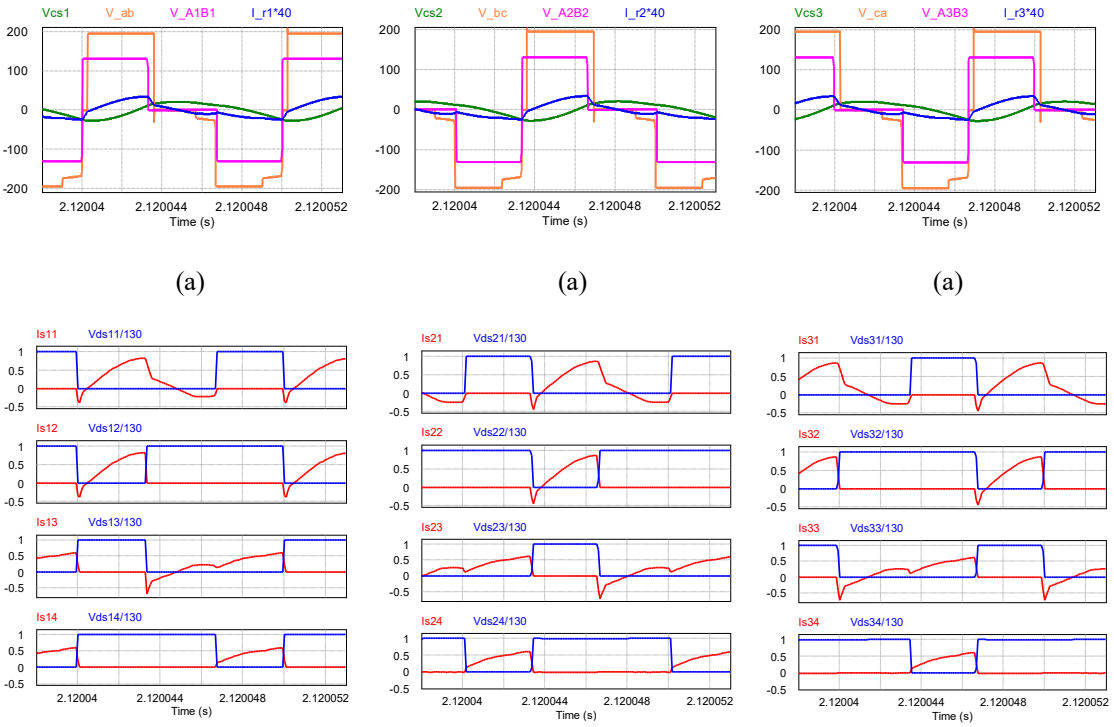


Fig 5.13: PSIM simulation results for maximum input voltage $V_{s(max)}$ = 130 V for 20% of full-load condition, where, (a) resonant inductor currents i_{r1}, i_{r2}, i_{r3}; inverter output voltages v_{A1B1}, v_{A2B2}, v_{A3B3}; rectifier input voltages v_{ab}, v_{bc}, v_{ca}; resonant capacitor voltage v_{Cs1}, v_{Cs2}, v_{Cs3}. (b) voltage across the switches (v_{ds11}, v_{ds12}, v_{ds13}, v_{ds14}, v_{ds21}, v_{ds22}, v_{ds23}, v_{ds24}, v_{ds31}, v_{ds32}, v_{ds33}, v_{ds34}) and respective current through (i_{s11}, i_{s12}, i_{s13}, i_{s14}, i_{s21}, i_{s22}, i_{s23}, i_{s24}, i_{s31}, i_{s32}, i_{s33}, i_{s34}) switches $S_1 - S_{12}$.

Table 5.3: Comparison of results.

Parameter	$V_{s(min)}$ = 110 V				$V_{s(max)}$ = 130 V			
	Full-Load		20% of Full-Load		Full-Load		20% of Full-Load	
	Cal.	Sim.	Cal.	Sim.	Cal.	Sim.	Cal.	Sim.
V_o (V)	200	194.08	200	194.24	200	194.33	200	194.35
I_o (A)	3	2.911	0.6	0.582	3	2.915	0.6	0.583
R_L (Ω)	66.667	66.667	333.33	333.33	66.667	66.667	333.33	333.33
$I_{r1(r)}$ (A)	2.083	2.099	0.442	0.492	2.083	2.056	0.442	0.448
$I_{r2(r)}$ (A)	2.083	2.098	0.442	0.491	2.083	2.053	0.442	0.448
$I_{r3(r)}$ (A)	2.083	2.098	0.442	0.49	2.083	2.053	0.442	0.448
$V_{Cs1(r)}$ (V)	83.362	83.191	17.667	18.579	83.363	81.41	17.667	16.611
$V_{Cs2(r)}$ (V)	83.362	83.165	17.667	18.542	83.363	81.32	17.667	16.617
$V_{Cs3(r)}$ (V)	83.362	83.178	17.667	18.511	83.363	81.30	17.667	16.613
δ (deg.)	179.9	178	165.91	150	133.81	129	131.82	116
$\%\,\eta$	95.28	96.65	95.69	96.04	90	93.7	74.17	92.62

5.5 Conclusion

A three-phase interleaved CLL resonant DC-DC converter with fixed frequency modified PWM gating scheme is presented. The interleaving resonant converter achieves higher power level, low output ripple current, high conversion efficiency and the operation of the converter at high-frequency achieves high power density. The three identical full bridges with CLL resonant tank on the primary side of high-frequency (HF) transformer are connected in parallel. The operating modes of the converter for different intervals is described with the operating waveforms. The steady state analysis of the converter is carried out by using fundamental harmonic approximation approach and the design procedure is explained. The PSIM simulations are carried out to substantiate calculated predictions of the converter for various operating conditions.

The proposed converter for medium to high power applications is able to provide ZVS to all the 12 switches when minimum input voltage is applied for wide variations in loading conditions. When maximum input voltage is applied to the converter, only 3 switches lose ZVS resulting more efficient than the converter applied with phase-shift gating scheme where 6 switches lose ZVS.

Chapter 6

CONCLUSIONS AND FUTURE SCOPE

This chapter provides a description of the research work completed, a review of the contributions and some suggestions for the work to be performed in future. The layout of this chapter is as follows: The detailed summary of the research work done for this dissertation is given in Section 6.1. The contributions made in this dissertation are outlined in Section 6.2. Some suggestions for future work are described in Section 6.3.

6.1 Summary of the Work Done

DC-DC converters are needed for several renewable energy applications in regulating the output voltage for wide range of variations in input voltage and loading conditions. The DC-DC converter plays an important role in conditioning the fluctuating power into a usable constant power. High-frequency resonant DC-DC converters are used to reduce the switching losses, electromagnetic interference (EMI) and increase the power density and efficiency. The challenge is to achieve high performance of the converter for variations in input voltage and loading conditions. The converters are often used with electrical isolation for connecting renewable energy sources (e.g., fuel cells, solar energy) with the utility grid. Hence, the dissertation deals with the study of high frequency transformer isolated resonant DC-DC converters for the applications involving variations in input voltage and loading conditions.

In Chapter 2, the literature review on resonant power converters and gating control schemes is described. The selection of the resonant converter topology and a suitable gating control scheme is explained.

In Chapter 3, a high-frequency full bridge CLL resonant DC-DC converter operated with phase-shift gating scheme (PGS) and modified PWM gating scheme (MGS) is proposed. Various modes of the converter operation with both the gating schemes are described and examined in detail. Detailed modeling and the steady-state analysis of the converter is performed by using fundamental harmonic approximation approach. The procedure for optimum design of the converter is described with the help of a flowchart and typical design curves for a sample converter of 200 W rating operated with a switching frequency of 100 kHz. PSIM simulation is carried out and the experimental prototype is built in the laboratory to substantiate theoretical performance predictions. The power loss breakdown analysis of the converter applied with phase-shift gating scheme (PGS) and modified PWM gating scheme (MGS) has been performed. The performance of the converter when operated with PGS and MGS is studied using PSIM simulations and verified experimentally for wide variations in input voltage and loading conditions. The theoretical, simulation and experimental results of the converter for input voltage 40 V and 80 V at full-load, 75% load and 20% load respectively are presented.

In Chapter 4, a modified PWM gating scheme with a zero-voltage transition (ZVT) auxiliary circuit is proposed for a fixed frequency full-bridge CLL resonant DC-DC converter with a capacitive output filter. An approximate complex ac circuit approach is used for the steady state analysis of the converter. The optimum design of the converter is illustrated with the help of design curves. The converter with applied gating scheme and ZVT auxiliary circuit provides zero-voltage switching (ZVS) to all the switches for the entire variations in loading and input voltage conditions, ensuring higher conversion efficiency. PSIM simulations are carried out to verify theoretical predictions about the performance of the converter for various operating conditions. Finally, experimental model of 200 W converter is built in the laboratory and the experimental results are provided to verify the feasibility of the proposed converter. The converter operates with ZVS for all the switches for the entire variations in loading and input voltage conditions and the secondary side rectifier diodes operate with ZCS. Hence, this converter is a good choice for applications involving fluctuating power

which is typical of a renewable energy source. The theoretical, simulation and experimental results are given and discussed in detail.

In Chapter 5, a three-phase interleaved CLL resonant DC-DC converter operated with a fixed frequency modified PWM gating scheme is proposed. The operating modes of the converter for different intervals is described with the key operating waveforms and equivalent circuit diagrams. The steady state analysis of the converter is carried out by using fundamental harmonic approximation approach and the design considerations of 600 W sample converter are illustrated with the help of design curves. The PSIM simulations are carried out to substantiate theoretical predictions of the converter for various operating conditions. The proposed converter for medium to high power applications is able to provide ZVS to all the 12 switches when the minimum input voltage is applied for wide variations in loading conditions. When maximum input voltage is applied to the converter, only three switches lose ZVS resulting in better efficiency than the converter applied with phase-shift gating scheme where six switches lose ZVS.

6.2 Contributions

This dissertation presents modeling, analysis and design of high-frequency full bridge transformer isolated resonant DC-DC power converters for their use in interfacing the renewable energy sources with the utility grid/load. The simulation and experimental results of the converters are described in the dissertation.

The main contributions of this research are outlined as follows:

1. A high-frequency full bridge CLL resonant DC-DC converter operated with phase-shift gating scheme (PGS) and modified PWM gating scheme (MGS) is proposed. The detailed modeling, steady state analysis and optimum design of the converter is carried out. The performance of the converter is studied with PSIM simulations and verified with the experimental prototype of 200 W converter. The efficiency of the converter operated with MGS is better compared to that with PGS for applications with wide variations in input voltage and load. This work has resulted

in two publications (Patil and Harischandrappa 2020; Patil and Nagendrappa 2018).

2. A modified PWM gating scheme and a zero-voltage transition (ZVT) auxiliary circuit is proposed for a fixed frequency full-bridge CLL resonant DC-DC converter with a capacitive output filter. The analysis, design in selecting the converter parameters and the design of ZVT auxilary circuit is carried out. The performance of the proposed converter is evaluated with PSIM simulations and experimental setup built in the laboratory. The proposed converter operates with ZVS for all the switches for entire variations in input voltage and load. This work has resulted in one publication (Patil and Harischandrappa 2019).
3. A 3-phase interleaved CLL resonant DC-DC converter operated with a fixed frequency modified PWM gating scheme is proposed for medium to high power applications. The modeling and analysis of the converter are presented and the design procedure is explained. The PSIM simulations are carried out to substantiate calculated predictions of the converter for various operating conditions and the performance of the converter is evaluated. The proposed converter provides good efficiency for variations in input voltage and loading conditions.

6.3 Suggestions for Future Work

From this dissertation, the following are the suggestions for future research.

1. The performance evaluation of three-phase interleaved CLL resonant DC-DC converter with a fixed frequency modified PWM gating scheme has to be experimentally verified.
2. The regulation of the output voltage of the proposed converters in this dissertation are done by open-loop control. Therefore, the closed-loop control can be implemented in the future.
3. The small signal analysis, transient response and the impact of thermal distribution on the performance of the converter can be studied in detail in the future.

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B. Refereed International Conference Proceedings

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