DESIGN AND ANALYSIS OF RECONFIGURABLE RF FRONT END AMPLIFIERS FOR WIRELESS BROADBAND MULTIMEDIA COMMUNICATION

Thesis

Submitted in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

by

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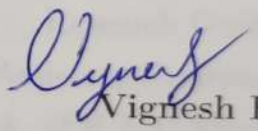
DECLARATION

I hereby *declare* that the Research Thesis entitled **DESIGN AND ANALYSIS OF RECONFIGURABLE RF FRONT END AMPLIFIERS FOR WIRELESS BROADBAND MULTIMEDIA COMMUNICATION** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this research thesis has not been submitted to any University or Institution for the award of any degree.



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Dedicated to
My Dear Parents

Abstract

This research work focuses on the design and implementation of Microwave Low Noise Amplifiers (LNAs) with built-in techniques for wireless broadband multimedia communications. The RF front-end blocks account for the majority of the system's Noise Figure (NF). As a result, low noise designs are being researched to improve the device's signal-to-noise ratio (SNR). Enhancing the SNR and linearity of the front-end amplifiers significantly boosts receiver performance. The proposed LNAs' primary objective is to produce low NF, high flat gain, and excellent linearity while minimizing power consumption at the microwave and millimeter (mm) wave bands of operation.

Firstly, a Suspended Substrate Line (SSL) integrated CMOS LNA is proposed for low-power 5G wireless receiver systems which are operated in the range of 28GHz to 32GHz. It comprises two stages cascode topology for high gain, better reverse isolation, and improved stability at mm-wave frequencies. A novel SSL-based parallel series network is incorporated between the two cascode stages to provide the required network matching and help in enhancing the bandwidth. Prior to incorporation into the design, the proposed SSL is designed and characterized for optimum EM compatibility. The proposed CMOS LNA, which incorporates these novel approaches, will overcome the device's parasitic and electromagnetic (EM) losses. EM losses in bulk active and passive components have been incurred utilizing built-in approaches to improve LNA linearity. The proposed mm-wave LNA enables each component in its family to prevent EM wave leakage and its associated parasitic losses in the layout. The simulation and measurement results demonstrate the minimum NF of 2.5dB, the maximum gain of 25dB, and high linearity and stability in the desired band of operation.

Secondly, A novel Quasi circulator (QC) integrated LNA operating in 8GHz to 12GHz (X band) is implemented using a two-stage inductive degeneration common source (CS) topology with current reused techniques and variable impedance load. QC provides the minimum insertion loss of 0.9dB with good return and isolation losses. Incorporating QC and opti-

mizing the LNA, the highest flat gain of 30dB with only 0.5dB variation across the entire 4GHz bandwidth and minimum NF of 1dB are achieved simultaneously. The proposed QC-LNA is highly linear, and third-order harmonics are suppressed considerably. It consumes low power and is highly compact.

Thirdly, an integrated LNA with a Folded Butterfly Stub Stepped Impedance Resonator (FBSSIR) is also developed by employing packaging technology for a satellite navigation receiver system in the range of 1.6GHz to 2.5GHz. The proposed FBSSIR achieves a more compact structure, controllable transmission zero, adjustable center frequency, and adjustable bandwidth by applying a new structural deformation of a stepped-impedance-resonator (SIR). The core LNA circuit incorporates the proposed FBSSIR as it acts as a filter and the input-output matching network. The proposed FBSSIR-LNA achieves good gain, decent NF, and good linearity by consuming decent power.

Finally, a switch-free dual-band reconfigurable LNA in the range of 18GHz to 40GHz (K/Ka-band) is also designed for ultra-wideband wireless applications. It is realized by incorporating inter-stage and output-stage Suspended-Substrate Coupled-Lines (SSCL). The cascaded CS topology with source degeneration is used in the respective amplifier stages. The proposed inter-stage SSCL splits the amplified input signal from the broadband driving stage into two parallel single band stages. The corresponding High-band (Ka) and Low-band (K) stages amplify two split-band signals. At the output, the proposed SSCL output stage combines the amplified two single bands. Also, the proposed SSCL provides the necessary network matching to the LNA. A single band of operation can be obtained by simply shutting off the drain voltage of the unused transistor band. The proposed LNA achieves an incredibly flat gain of 27dB, ultra-low NF of 1.2dB, and best linear performance with good third-order harmonics suppression at the same time.

All the proposed CMOS LNAs are fabricated using a commercial 65nm CMOS process operating with 1.2V supply. DoE and statistical analysis are additional novel contributions towards this thesis work for analyzing

the proposed LNA designs. Design of Experiment (DoE) is a new analysis technique to find the individual device parameter's contribution to the final gain, NF, and return loss. Statistical analysis is also performed to find the yield so that the robustness of the proposed designs is satisfied.

Keywords: Low Noise Amplifier; Suspended Substrate Line; Quasi Circulator; SSCL; FBSSIR;

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Abbreviations

SSL	Suspended Substrate Line
LNA	Low Noise Amplifier
THD	Total harmonic distortion
MOSFET	Metal oxide semiconductor field effect transistor
NMOS	N-channel metal oxide semiconductor
PMOS	P-channel metal oxide semiconductor
CMOS	Complementary metal oxide semiconductor
EM	Electro Magnetic
RF	Radio Frequency
NF	Noise Figure
QC	Quasi Circulator
SoC	System-on-chip
QN	Quasi Newton
SD	Source degeneration
FBSSIR	Folded Butterfly Stub Stepped Impedance Resonator
SIR	Stepped Impedance Resonator
SNR	Signal to noise ratio
FoM	Figure-of-merit
DoE	Design of experiment
DC	Direct current
SSCL	Suspended Substrate Coupled Line
PVT	Process, supply voltage and temperature
IIP	Input Intercept Point
OIP	output Intercept Point
RFIC	Radio Frequency Integrated Circuit
PCB	Printed Circuit Board
ADS	Advanced Design System
DUT	Device Under Test
MSL	Microstrip Line
PDK	Process Design Kit
PNA	Programmable Network Analyzer
IRNSS	Indian Regional Navigational Satellite System
BJT	Bipolar Junction transistor

.

Notations

f	Frequency in Hz
ω	Angular frequency in radians per second
f_c	Cut-off frequency in Hz
g_m	Transconductance
γ	Excess drain noise coefficient
δ	Excess gate noise coefficient
Q	Quality factor
c	Correlation coefficient
L	Channel length of the MOSFET
W	Channel width of the MOSFET
V_{GS}	Gate-source voltage of the MOSFET
V_{DS}	Drain-source voltage of the MOSFET
k	Boltzmann Constant
T	Absolute temperature
μ_n	Mobility of electrons
C_{ox}	Gate-oxide capacitance
g_{d0}	Drain conductance for zero drain-source voltage
g_g	Frequency dependent gate conductance
Z_0	Characteristic Impedance
ε_{eff}	Effective dielectric constant
λ	Wavelength

.

Chapter 1

INTRODUCTION

The phrase "communication" refers to the sharing of information between two individuals or groups of individuals using a medium for transmission. The communication process will succeed when the receiver provides positive feedback to the sender on the received signal. The term "Multimedia" refers to the simultaneous use of different modes of communication such as audio, text, video, images, graphics, animation, and so on at the same time.

Telecommunications' basic purpose was connectivity with mobility. As Technology evolved the services provided with it began to grow. Currently, services are not limited to voice and text messaging. A Long-term Evolution (LTE) known as 4G communication with a new and updated infrastructure was introduced in 2009, which provided very high data rates of more than 28Mbps. The world is mostly using this advanced version of 4G communications, which provides multi-services such as mobile banking, multimedia browsing such as video streaming, video calling, etc. The latest survey on networking shows that more than 90% of network data traffic is of multimedia content.

The purpose of the Wireless Broadband Multimedia Communication Systems (WBMCS) is to provide users with radio access to broadband multimedia services that are either supported by customer premises networks or directly provided by public fixed networks. WBMCS will provide a non-wired, mobile (or at least movable) extension to wired networks for data speeds greater than 300 Mbps, with applications in wireless Local Area Network (LAN) or mobile broadband systems.

WBMCS is being researched in the microwave (3-30GHz) and millimeter wave (30-300GHz) bands to meet the required bandwidth. The topic of WBMCS research has

garnered considerable attention as a result of the growing importance of multimedia and computer applications in communications. The latest development is the next generation communication system known as 5G developed from the LTE advanced, which provides multi services than 4G with a high data rate of 1 Gbps and accuracy.

1.1 RF Frontend

The RF front end is the heart of any wireless communication system. The term RF front end refers to modules located near the antenna. The block diagram of a typical RF front end is shown in Figure 1.1. It consists of a filter, amplifier, and converter. The amplifier used in the transmitter is called a Power amplifier because it focuses on multiplying the signal's power density before transmission. In contrast, the amplifier in the receiver is called Low Noise Amplifier (LNA) because it mostly determines the noise performance of the entire RF receiver. Three critical signal processing processes are performed by an RF front end, both in the transmitter and receiver signal paths(Baltus 2004):

- Frequency translation is used to convert a stream of signals to a frequency suitable for transmission or processing.
- Amplification of a signal to obtain an amplitude suitable for further transmission or processing.
- Signal filtering, to exclude undesired signal components created by other transceivers or the transceiver's signal-processing circuits.

The frequency conversion happens with the help of mixers and local oscillator signals. It can also be performed in two or more conversion stages, which reduces the performance requirements for the individual filter, gain, and mixer blocks. A straightforward antenna interface is seen here, with distinct, single-antenna transmits and receives antennas. In fact, it is generally beneficial to share the transmitter's antenna with the receiver to save money and space. Between the circuits and the antenna, this requires switches or duplex filters. Additionally, many systems today employ multi-band radios, necessitating the use of several antennas or numerous antenna feeds, which necessitates the addition of additional switches or, in some cases, variable capacitors.

Frequency conversion oscillators are frequently tunable to enable channel selection at the radio's front end, hence decreasing the dynamic range needs of the filters, IF

(Intermediate Frequency) amplifiers, and data converters. These tunable oscillators are often controlled by a synthesizer loop, which significantly complicates the front end in terms of transistor count. Even yet, an RF front end is composed of a small number of active devices, frequently in the hundreds or thousands. The silicon area of the front-end lowers as IC technology advances, resulting in device shrinkage in physical dimensions. Current RF front-end integrated circuits are only a few square micrometers in size. Additionally, with enhanced transceiver architectures such as single-conversion receivers and greater radio digitization, the needed functionality, and hence the number of active devices lowers.

After the RF front ends, the signal will be sent to the RF back end, which refers to the module far away from the antenna or also known as the baseband processing module. The role of the receiver is more crucial than the sender in the communication process. The LNA is the most crucial part of the receiver module. This thesis focuses primarily on the Low Noise Amplifier design.

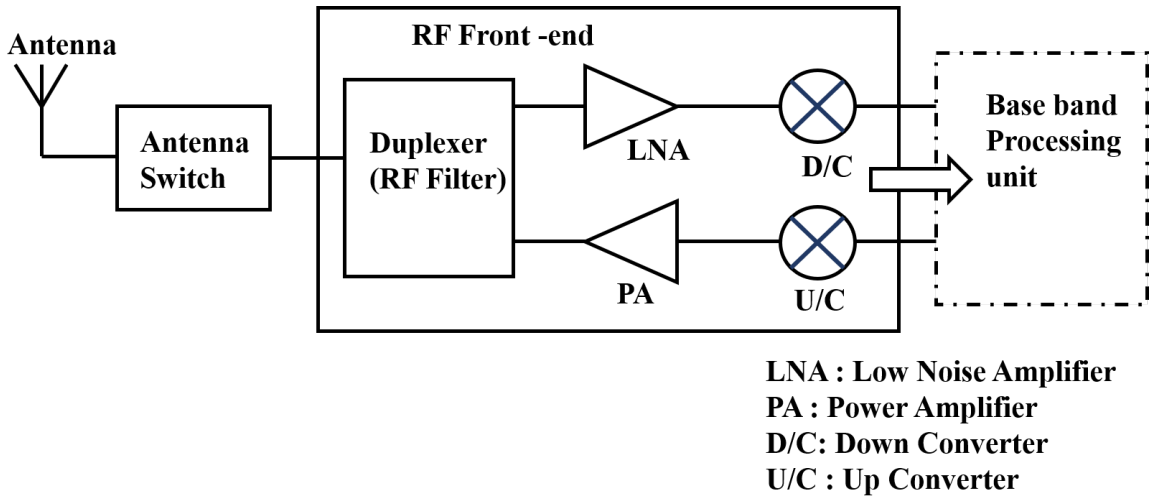


Figure 1.1: Simple block diagram of typical RF frontend

1.2 Issues in RF Frontend

Wireless Broadband Multimedia Communication Systems (WBMCSs), which support data rates greater than 20 Mb/s, are rapidly emerging (da Costa and Yang 2020). The RF design is quite challenging because a good understanding of multidiscipline knowledge is needed. Even if we focus on the RFIC design, mainly the receiver

or transmitter, they also possess many trade-offs among noise, power, linearity, gain, frequency, and supply voltage. This is depicted as an RF design hexagon in Figure 1.2 (Razavi 2013). These trade-offs in the RFIC design create numerous architecture designs based on the requirement and applications used.

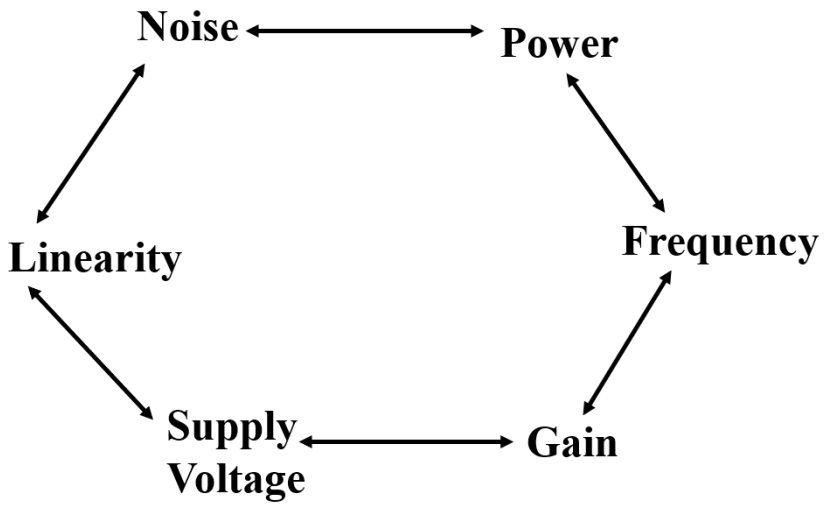


Figure 1.2: RF design Trade-offs

The RFIC performance depends on many factors and is mainly classified into two variables: device-level variables and board-level variables. The main parameters affecting the RFIC performance are depicted in Figure 1.3 (Das 2013). It is noted that the devices level variables such as device geometry. Process technology and parasitics depend purely on the silicon technologies such as CMOS, BiCMOS, and so on. Each technology has distinct advantages and disadvantages and is chosen only for the purpose of meeting the requirements and applications. This gives the researcher the opportunity to work with various device technologies in the RFIC design. The circuit and board-level variables also allow the researcher to illustrate numerous designs based on requirements and applications. In short, the research gap in RFIC design is depicted as:

- Demands for enhanced performance, cost savings, and functionality continue to create new obstacles.
- These trade-offs and advancements in technology make the RFIC design more challenging and never-ending scope in the future.

- As communication evolves rapidly, such as 5G, the need to invent new RFIC chips is mandatory. This gives a significant scope in working in the field of RFIC design.

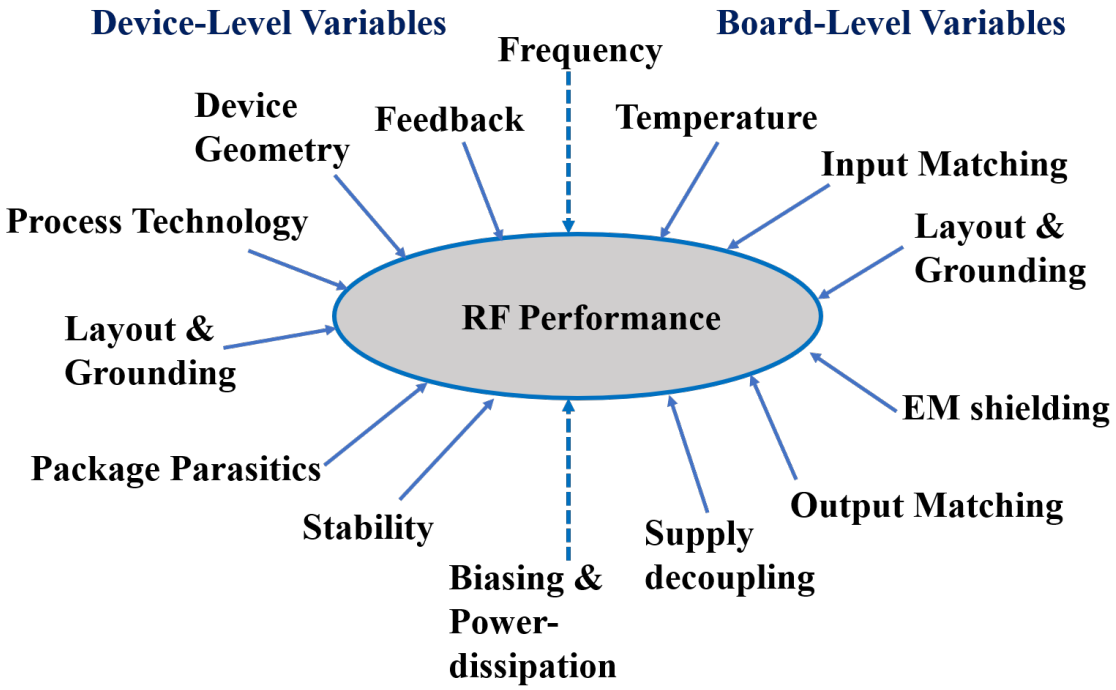


Figure 1.3: Parameters impacting RF performance

1.3 Motivation

The Low noise amplifier (LNA) is the most crucial signal processing block in any RF receiver as it decides almost all the important parameters of the receiver. The RF design tradeoffs, as in Figure 1.2, allows the researcher to propose the new design trade-offs in the LNA to achieve high performance at reduced cost, power, and size. Moreover, the combination of device-level variables and circuit-level variables allows one to propose and test a new LNA design topology to enhance the receiver performance better.

The incorporation of the microwave techniques and components into the design of the LNA pave the way for the new dimensional performance analysis. These microwave techniques and components help in controlling the signal in the circuit, such

as controlling the direction of the wave, splitting the wave, phase shifting of the wave, and so on. One such component is the suspended substrate line which allows the designer to optimize the performance of the LNA for better trade-offs. This urges the RF designer to work on developing new methodologies by using microwave techniques for the LNA design.

1.4 Objectives

- To design a wideband LNA by using a suspended substrate line in order to achieve high gain and low noise figure.
- To design and analyze Quasi-Circulator integrated LNA using Quasi Newton Algorithm optimization to achieve ultra-low-noise figure and stable flat gain over a broadband frequency range of operation.
- To design and analyze stepped impedance resonator integrated LNA to get yield estimation and robustness of the design.
- To design and analyze a switchless reconfigurable ultra-wideband LNA to achieve flat gain, ultra-low noise figure, good linearity, low power consumption, and compact size.
- To carry out all CMOS designs from layout to commercial 65nm CMOS chip fabrication.

1.5 Organization and contribution of thesis

The thesis's aim is to build novel LNA designs with built-in techniques for broadband applications. Based on the technological background and motivation, the primary interest is in building integrated circuits for LNA with the best power, noise, and impedance matching. Additionally, this LNA should have a high gain and linearity to enhance receiver performance.

Chapter 2 details the significance and definition of LNA performance metrics that are used to evaluate RF design, such as noise figure, gain, 1-dB compression point, Figure of merit, input intercept point, S-Parameters, and dynamic range. Additionally, a brief description and comparison of the conventional LNA topologies are provided.

Chapter 3 details the proposed techniques of the Suspended Substrate line (SSL) based LNA for a 5G communication system in the frequency range of 28-32GHz.

Primarily, structural analysis of the SSL is presented with the simulation results. Second, the analytical modeling of SSL inspired parallel series network with the layout and simulation results are provided. Then a detailed discussion on the proposed CMOS LNA based on the built-in techniques is given. Finally, the measurement and simulation results and their discussion are provided to compare state-of-the-art.

Chapter 4 discusses the Quasi circulator (QC) integrated LNA for X-band RF front-end systems working in the frequency range of 8-12GHz. The design of the Quasi circulator based on the CMOS process and its simulation results are given primarily. A detailed discussion of the CMOS LNA design topology is presented secondly. The optimization algorithm, namely the Quasi-Newton algorithm, is given afterward. Finally, a detailed discussion is provided for the simulation and measurement results with the state-of-the-art comparison table.

Chapter 5 details the wide bandwidth Folded Butterfly Stub Stepped Impedance Resonator (FBSSIR) integrated LNA for satellite navigation systems operating in the frequency range of 1.6-2.5GHz. Firstly, the proposed FBSSIR design fundamentals and analysis with the PCB layout and results are provided. Secondly, the proposed LNA design based on the integration with FBSSIR is provided in a detailed manner. Finally, a detailed discussion of the measurement results is provided with the state-of-the-art comparison table.

Chapter 6 discusses the switchless reconfigurable CMOS LNA based on the Suspended Substrate Coupled line (SSCL) operating in the full K/Ka-band (18-40GHz) is presented. Firstly, the coupled lines are discussed in-depth with analysis and simulation results to show the potential of the proposed SSCL with the conventional coupled lines. Secondly, the design topology of CMOS LNA is discussed in detail with simulation results. Finally, a detailed discussion of the measurement results is provided with the state-of-the-art comparison table. .

The conclusion of this thesis is given in Chapter 7, highlighting the contribution of the work and throwing hints at possible future works. All the LNA designs proposed are fabricated and tested with measurement results. They are also compared with the respective state of art LNA in each chapter.

Chapter 2

LNA PERFORMANCE METRICS AND ANALYSIS

2.1 Introduction

When designing a complete wireless radio receiver, it is critical to evaluate the low noise amplifier and other blocks to have a complete understanding of their performance. The performance of a receiver design is determined by a number of factors, including the receiver's sensitivity, selectivity, and susceptibility to reception mistakes. The RF design engineer's primary objective is to maximize the front-end performance, with a particular emphasis on the first amplifying device. To reliably retrieve the contained information, high-end receivers require a good LNA to discriminate the desired signal from the noise in the environment. Certain properties of the LNA are controllable by the designer and have a direct effect on the receiver's sensitivity: noise figure, gain, bandwidth, linearity, and dynamic range. Controlling these properties, on the other hand, demands a grasp of the active device, impedance matching, fabrication, and assembly details in order to design an amplifier with the fewest possible trade-offs.

The set of variables affecting LNA performance at the device and board design levels is depicted in Figure 1.3. It is the designer's responsibility to reduce the impact of external variables while identifying the most appropriate trade-offs between conflicting qualities in order to maximize receiver sensitivity, selectivity, and information integrity. The trade-offs at the device level are determined by the process technology, transistor shape, and package parasitics. All of these parameters have a substantial effect on noise performance and should be taken into account when designing the

LNA. In fact, implementing a high-performance LNA is difficult due to parameter trade-offs. The recent reported works in the LNA are provided in the Table 2.1 for getting insights into the performance reported so far.

Reported Works	Technology	Frequency (GHz)	Gain (dB)	NF (dB)	Power (mW)	Area (mm^2)
Qin and Xue 2017*a*	65nm CMOS	16-30	10.2	5.7	19	0.37
Qin and Xue 2017*b*	65nm CMOS	8-29	10.7	5.6	12.1	0.3
Davulcu *et al.* 2018	130nm SiGe CMOS	8-12	20	1.4	100	0.72
Çalışkan *et al.* 2019	130nm SiGe BiCMOS	6-12	10	1	20	0.4
Wang and Zhang 2020	130nm SiGe BiCMOS	22-47	22	4.3	10	0.13
Yu *et al.* 2021	65nm CMOS	22-40	28	3.2	32	0.4

Table 2.1: Reported works on LNA

2.2 Noise

In communication systems, noise is defined as an unwanted signal because it reduces the overall system's sensitivity. There are numerous sources of noise, each with its own unique method of noise generation. Shot noise, flicker noise, and thermal noise are the three primary causes of noise in integrated circuits. Shot noise is primarily created by electric charges hopping across a potential barrier and is characteristic of nonlinear devices such as diodes and transistors. The only source of shot noise in MOS devices is the DC gate leakage current, and thus it is not regarded as a significant issue (Lee 2004). This is in contrast to bipolar transistors, which can drastically reduce the receiver's overall performance due to base and collector shot noise.

Flicker noise (alternatively called pink noise) originates as a result of charges being trapped in the flaws and impurities in the channel area of MOS devices. Larger MOS devices, on average, exhibit less flicker noise. (Lee 2004) provides the spectral density of this noise.

$$\overline{i_{fn}^2} = \frac{K \cdot g_m^2}{fWLC_{ox}^2} \tag{2.1}$$

Here, K denotes a device constant, g_m denotes the MOS device's transconductance, f denotes the operating frequency, C_{ox} denotes the gate-oxide capacitance per unit area, and W and L denote the MOS device's width and length, respectively.

2.2.1 Thermal noise

Thermal noise is generated when carriers in a conductor are agitated, and its spectral density is defined by the following number, referred to as available noise power (Lee 2004).

$$P_{NA} = kT\Delta f \tag{2.2}$$

where k denotes the Boltzman constant ($1.38 \times 10^{-23} J/K$), T is the absolute temperature in Kelvins, and Δf denotes the noise bandwidth in Hz. P_{NA} is -174dBm for a 1 Hz noise bandwidth at room temperature (290K) and is frequently referred to as the system's noise floor. The noise floor is a critical parameter in determining the receiver's sensitivity (Lee 2004).

2.2.2 MOS devices dominant noise sources

Figure 2.1 (Molavi 2005) illustrates the various sources of noise in a MOS device. In the saturation area, the MOS device behaves like a trans-conductor; in the triode region, it behaves like a resistor. As a result, thermal noise associated with carriers in the channel will be identical to the noise associated with carriers in a conductor. (Van der Ziel 1986) deduced the expression for the drain current noise (also known as channel thermal noise) in MOS devices, which is given as

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f \tag{2.3}$$

where g_{d0} is the drain conductance at zero drain-source voltage and γ is a technology-dependent parameter with a value of around 2/3 for long-channel devices at saturation (it is bigger in short-channel devices and has a value of 3 for 180 nm technology) (Molavi 2005). A comprehensive investigation of the noise characteristics of a MOS device indicates that channel thermal noise does not capture all of the noise produced by the device (Shahani *et al.* 1997). To simulate the additional noise, a frequency-

dependent gate conductance can be introduced:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{2.4}$$

And an equivalent gate current noise is expressed as:

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{2.5}$$

where δ denotes the gate noise coefficient, which is a technology-dependent metric. Its value is 4/3 in the case of long channel and 6 in the case of 180 nm technology (Van der Ziel 1986). The correlation coefficient between gate current noise and channel thermal noise is provided as:

$$c = \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}} \cdot \sqrt{\overline{i_{nd}^2}}} \tag{2.6}$$

where c is a complex number with a theoretical value of roughly $0.395\,j$ for long channel devices as defined in Van der Ziel Aldert (1986) and $-0.55\,j$ for 180 nm technology. Another type of noise in MOS devices that may contribute to the total noise of LNA is the distributed resistance of the poly-silicon gate (Lee 2004). The value of this resistance is as follows:

$$R_g = \frac{R_\square W}{3n^2 L} \tag{2.7}$$

where $R_\square$ is the gate terminal's sheet resistivity, n is the number of gate fingers, and W and L are the width and length of the MOS device, respectively.

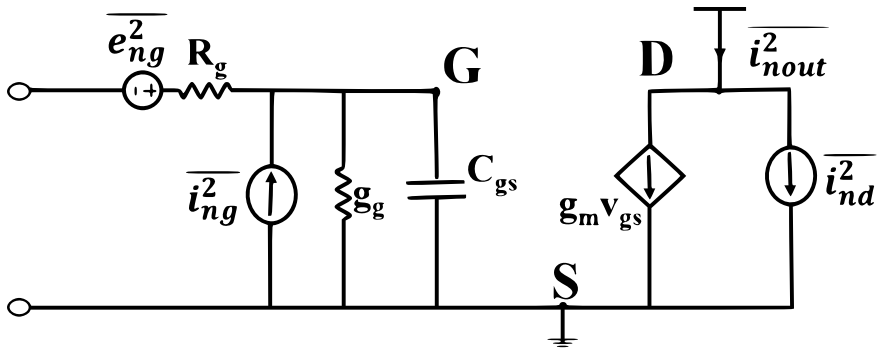


Figure 2.1: MOS transistor Dominant noise sources representation

2.3 Basic LNA Topologies

For comparison with the most relevant parameters, familiar LNA topologies have been considered. The three familiar topologies of the LNA are Common Source (CS), Common Gate (CG), and Cascode. Based on the reported works on these topologies it is noted that to construct narrow-band systems, the common source topology is more appealing. Stability and linearity are enhanced by the cascode connection of the same topology. On the other hand, the common gate topology's $1/g_m$ input impedance makes it suitable for wide-band applications. Table 2.2 compares the three basic topologies(Razavi 2013). The basic topologies can be modified to enhance their

PARAMETERS	Common Source	Common Gate	Cascode
Gain	moderate	low	high
Noise Figure	best	better	good
Sensitivity to PVT	more	less	less
Reverse isolation	low	good	best
Bandwidth	low	very wide	wide

Table 2.2: Basic LNA topologies comparison

performance accordingly.

2.3.1 Common source Topology

The Figure 2.2 represents the basic common source topology. We can modify the common source topology by having inductive load, resistive feedback, capacitive feedback, inductive degeneration, and so on. The resistive termination and voltage degradation are the bottlenecks in this topology and is quite useful in broadband matching than narrow-band. The noise factor at low frequency for this topology can be expressed as (Razavi 2013).

$$Nf = 2 + 4\frac{\gamma}{\alpha}\frac{1}{g_m R} \tag{2.8}$$

where α is $\frac{g_m}{g_{d0}}$. The noise factor exceeds 3dB even for low value of γ. This topology has an extremely high noise factor, which is incompatible with typical front-end architectures. Additionally, it is susceptible to transistor parasitics. The solution to this lies in degeneration of source through inductor known as inductive source degeneration common source topology as shown in Figure 2.3. This is traditionally used for narrow

band application but some works shown that by proper optimizing and matching we can make this for broadband application too. In this topology, simultaneous high gain and low noise can be achieved. Additionally, it provides excellent impedance matching without the use of a real resistor. From (Perrott 2005) and (Reddy 2019), the total drain noise current is depicted as

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\left(|\eta|^2 + 2\,\mathrm{Re}\left\{cX_d + Z_{gsw}\right\} + X_d^2\,|Z_{gsw}|^2\right) \tag{2.9}$$

where

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma g_{d0},\ \eta = 1 - \left(\frac{g_m Z_{deg}}{Z_{deg} + Z_g}\right),\ Z_g = R_S + j\omega L_g, Z_{deg} = j\omega L_{deg},$$

$$X_d = \frac{g_m}{g_{d0}}\sqrt{\frac{\delta}{5\gamma}}\ and\ Z_{gsw} = \frac{1}{j\omega C_{gs}} \| \frac{Z_{deg} + Z_g}{1 + g_m Z_{deg}}.$$

The auxiliary inductor (L_g) offers freedom to set resonance frequency (ω_0) and Z_{in} separately. For technology below 180 nm it equation 2.9 can be modified as

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\left(|\eta|^2 + 2\,\mathrm{Re}\left\{-j|c|X_d^* Z_{gsw}\right\} + X_d^2\,|Z_{gsw}|^2\right) \tag{2.10}$$

where $\eta = 1/2, Z_{gsw} = \frac{1}{2}\left(2Q_{in} - j\right)$ and Q_{in} denotes the quality factor of the input RLC network and is expressed as

$$Q_{in} = \frac{1}{2\omega_0 R_S C_{gs}} = \frac{\omega_0\left(L_g + L_{deg}\right)}{2R_S} \tag{2.11}$$

Equation 2.10 is simplified as

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\frac{1}{4}\left(1 - 2|c|X_d + \left(4Q^2 + 1\right)X_d^2\right) \tag{2.12}$$

The noise generated by the input source is specified as

$$\overline{i_{\text{nout}}^2} = \left(g_m Q_{\text{in}}\right)^2 \overline{v_{nR_S}^2} \tag{2.13}$$

The noise factor can also be defined as

$$Nf = \frac{\text{Total output noise power}}{\text{Output noise due to input source}} \tag{2.14}$$

Noise factor of inductive degeneration common source stage is written as

$$\begin{aligned} Nf &= \frac{\left(g_m Q_{in}\right)^2 \overline{v_{nR_S}^2} + \overline{i_{ndg}^2}/\Delta f}{\left(g_m Q_{in}\right)^2 \overline{v_{nR_S}^2}} \\ &= 1 + \left(\frac{\omega_0}{\omega_t}\right) \gamma \underbrace{\left(\frac{g_{d0}}{g_m}\right)\left(\frac{1}{2Q_{in}}\right)\left(1 - 2|c|X_d + \left(4Q_{in}^2 + 1\right) X_d^2\right)}_{\text{Noise scaling factor}} \end{aligned} \tag{2.15}$$

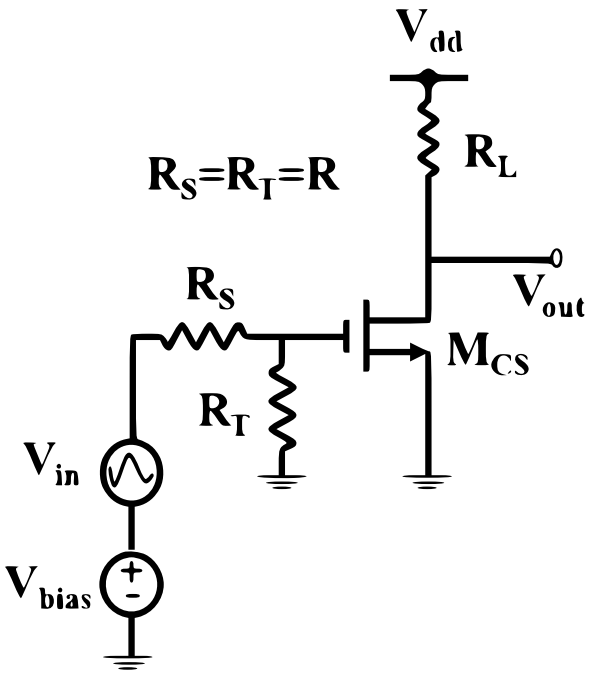


Figure 2.2: Common source Topology with no degeneration

2.3.2 Common Gate Topology

The common gate stage's low input impedance makes it an appealing choice for LNA design. The basic CG topology is shown in Figure 2.4. Without the use of a resistor, this topology provides impedance matching. While CG architecture has a lower noise factor than resistive terminated CS, it worsens at higher frequencies. The noise factor

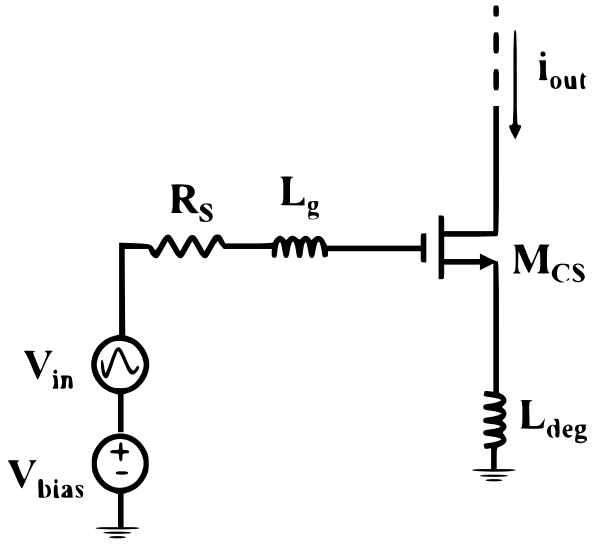


Figure 2.3: Common source Topology with inductive source degeneration

can be expressed as (Razavi 2013).

$$\begin{aligned} Nf &= 1 + \tfrac{\gamma}{\alpha}\tfrac{1}{g_m R_S} \\ \Rightarrow Nf &= 1 + \tfrac{\gamma}{\alpha}\left(\because \tfrac{1}{g_m} = R_S\right) \end{aligned} \tag{2.16}$$

This topology can also be modified to enhance the noise factor performance in the desired frequency range.

2.3.3 Cascode Topology

The cascode topology is a combination of CS and CG topologies and is shown in Figure 2.5. To minimize the noise contribution of M_{CG}, the inductor L_{deg} is used as source degeneration. This also allows the input to get isolated from the load, such as inductive load or resistive load. The real part and imaginary part impedance matching at the input is done by the degeneration inductor. The minimum noise factor of the cascode topology is expressed as (Nguyen *et al.* 2004).

$$Nf = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta\left(1 - |c|^2\right)\,|} \tag{2.17}$$

where

$$\omega_T = \frac{g_m}{C_{gs}}.$$

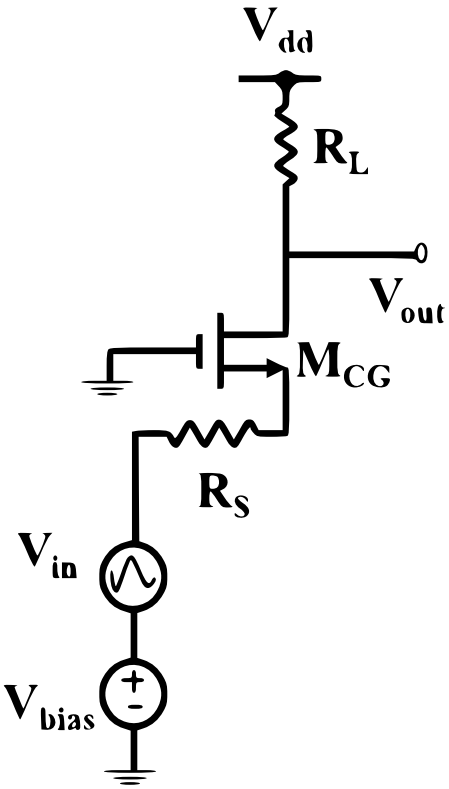


Figure 2.4: Common gate Topology

c is channel thermal noise correlation coefficient, δ is the gate noise coefficient and γ is a technology dependent parameter.

2.3.4 S-Parameters

Generally, we use Z, Y, and h-parameters while evaluating two-port networks at low frequency. To determine these parameters, open and short circuit tests must be performed, but at higher frequencies, this is extremely difficult due to the presence of parasitic capacitance and inductance. Due to the impossibility of conducting short and open circuit testing and the potential of causing damage to the circuit during these tests, (Collin 2001) recommends using an alternative method to characterize the network at high frequencies. One typical technique is the use of S-parameters (S stands for scattering), which define the four variables as incident (reflected) input (output) voltage (or power) waves. S-parameters are defined in such a way that they take advantage of the fact that a transmission line terminated at its characteristic impedance does not reflect any power at its termination (Lee 2004). Consider the

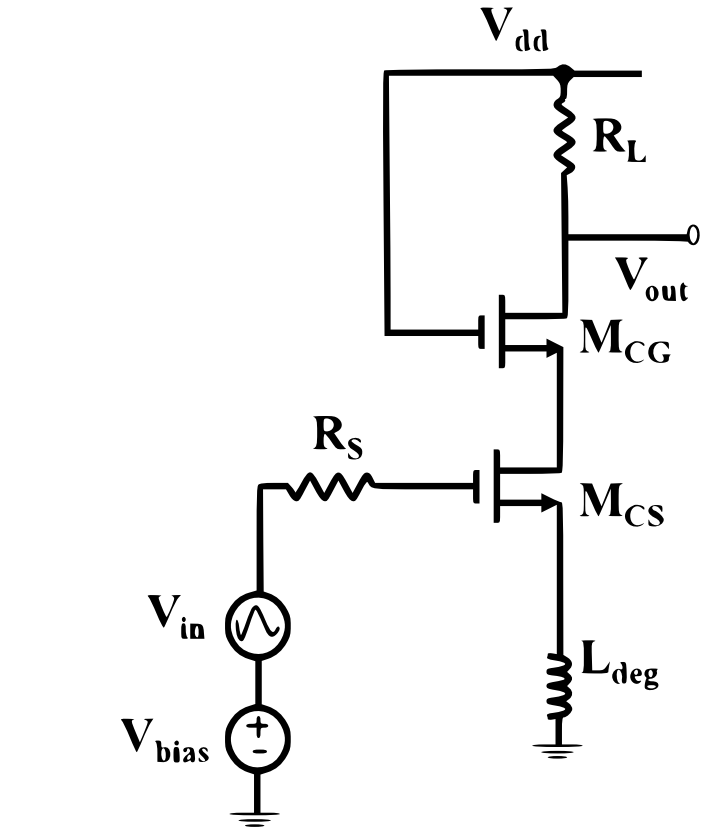


Figure 2.5: Cascode Topology with degeneration

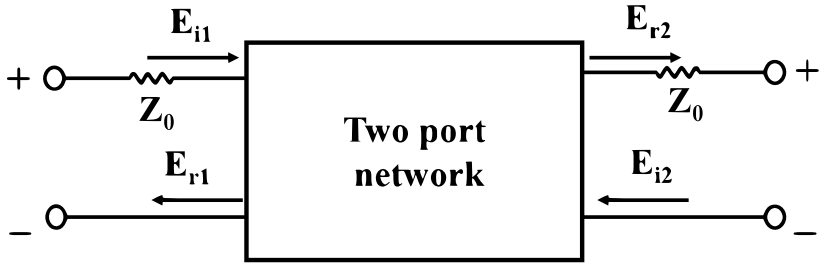


Figure 2.6: Port network for evaluating S-Parameters

block diagram of a two-port network illustrated in Figure 2.6, where Z_o denotes the impedance of the source and load terminations and E_{i1} and E_{r1} denote the magnitudes of the incident and reflected voltage waves, respectively. The coefficients of the S-parameters are as follows:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \tag{2.18}$$

where

$$a_1 = \frac{E_{i1}}{\sqrt{Z_0}},\ a_2 = \frac{E_{i2}}{\sqrt{Z_0}}, \quad b_1 = \frac{E_{r1}}{\sqrt{Z_0}}\ and\ b_2 = \frac{E_{r2}}{\sqrt{Z_0}}$$

The square of the magnitudes of a_i and b_i are equal to the incident and reflected power at both ports after normalization to the square root of Z_o. Now, if we end the second port with Z_o, which equalizes a_2, and connect port one to a power source, we have the following relationships:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = \frac{E_{r1}}{E_{i1}} \tag{2.19}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \frac{E_{r2}}{E_{i1}} \tag{2.20}$$

where S_{11} is referred to as the input reflection coefficient and is a practical measure of the LNA's input port impedance matching, and S_{21} is the amplifier's forward gain. On the other hand, if port one is connected to Z_o and power is supplied from port 2, the following relationships exist:

$$\begin{aligned} S_{12} &= \left.\frac{b_1}{a_2}\right|_{a_1=0} = \frac{E_{r1}}{E_{i2}} \\ S_{22} &= \left.\frac{b_2}{a_2}\right|_{a_1=0} = \frac{E_{r2}}{E_{i2}} \end{aligned} \tag{2.21}$$

where S_{12} denotes the reverse transmission or gain, and S_{22} denotes the network's output reflection coefficient. Using these definitions, we can predict that a good amplifier should have a large S_{21} for maximum gain, low S_{11} and S_{22} for optimal input and output matching, and a very low S_{12} for stability and reverse isolation. S_{21} is > 10 dB, S_{12} is < -40 dB and the input and output reflection coefficients are less than -10 dB; however, these values may vary depending on the application.

2.4 Noise Figure

The noise figure (NF) is a metric that indicates how the signal's signal-to-noise ratio (SNR) degrades as it travels through the receiver front-end. 'Harold Friis' defined the noise factor (Nf) mathematically as the ratio of the system's input SNR to its output

SNR. Nf is denoted by (Razavi 2013).

$$Nf = \frac{SNR_{i/p}}{SNR_{o/p}} \tag{2.22}$$

Additionally, the noise factor can be stated as

$$Nf = \frac{P_{sig}/P_{nR_S}}{SNR_{o/p}} \tag{2.23}$$

Where P_{sig} is the power of the input signal and P_{nR_S} is the power of the source resistance noise per unit bandwidth. As a result:

$$P_{sig} = P_{nR_S} \times (Nf) \times SNR_{o/p} \tag{2.24}$$

Because the power of the input signal is dispersed over the channel bandwidth, the total mean square power can be expressed as

$$P_{\text{sig,tot}} = P_{nR_S} \times (Nf) \times SNR_{o/p} \times B \tag{2.25}$$

where B is the channel bandwidth. The noise performance of a system determines the dynamic range's lower limit. The Nf value is typically expressed in decibels (dB) and is referred to as the noise figure (NF).

$$NF = 10\log_{10}(Nf) \tag{2.26}$$

Now the ultimate equation for NF from 2.25 is obtained as

$$NF = P_{sig,\text{min}}(dB) - (-174(dBm/Hz)) - SNR_{o/p,\text{min}}(dB) - 10\log_{10} B \tag{2.27}$$

NF can be specified for both individual blocks and the full receiver. NF_{LNA}, for example, determines the inherent noise of LNA, which is amplified with the signal. Friis deduced the noise factor for a cascaded system of m stages in 1947, and it is denoted by

$$Nf_{\text{tot}} = Nf_1 + \frac{Nf_2 - 1}{A_{p1}} + \frac{Nf_3 - 1}{A_{p1}A_{p2}} + \ldots + \frac{Nf_m - 1}{A_{p1}A_{p2}\ldots A_{p(m-1)}} \tag{2.28}$$

where Nf_i and A_{pi} are the noise factor and power gain of the i^{th} stage, respectively. As seen in equation 2.28, the noise contribution of each step reduces as the gain of the preceding stage grows. Thus, the gain and noise factor of the first stage determines the overall noise performance of the receiver. In practice, because the LNA is the first active block in the receiver chain, it is responsible for high gain, low noise, and the ability to handle significant unwanted signals.

2.5 Sensitivity

It is the signal level at which a receiver/LNA can identify an acceptable signal with acceptable quality. Acceptable quality is defined as a sufficient SNR. Generally, it should be as low as feasible for a strong receiver. It is mathematically written as (Razavi 2013):

$$P_{\text{sen}}\,(dBm) = -174(dBm/Hz) + NF(dB) + SNR_{o/p,\min}(dB) + 10\log_{10} B \quad (2.29)$$

where B denotes the RF system's bandwidth in Hz and $SNR_{o/p,\min}$ denotes the system's/minimum amplifier's SNR in dB at the output.

2.6 Distortion and intermodulation

While linear models can approximate the small-signal analysis of RF circuits, real-world circuits display some degree of nonlinearity, resulting in harmonic distortion (Razavi 2013).

2.6.1 Harmonic distortion

When a sinusoidal signal (i.e., $A\cos\omega t$) is applied to a nonlinear memoryless system, the output frequency is not only fundamental but also integer multiples of the input frequency (also called as harmonics). The general mathematical expression of a nonlinear system is as follows:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots \quad (2.30)$$

where $x(t)$ and $y(t)$ are the non-linear system's input and output, respectively. The gain of nonlinear systems now decreases as a function of $\left(\alpha_1 A + \frac{3}{4}\alpha_3 A^3\right)$, where A is the magnitude of the input signal. Gain compression is the process by which gain deviates from its ideal characteristics. The 1-dB compression point and third order intercept point (IP_3) are the most often used non-linearity indicators.

2.6.2 1-dB compression point

The 1-dB compression point is defined as the point at which the actual power gain deviates by 1 dB from its ideal value. The peak voltage of 1-dB compression is determined mathematically by

$$A_{in,1dB} = \sqrt{0.145 \left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.31}$$

2.6.3 Input intercept Point

Above this point, the circuit becomes highly nonlinear due to the presence of intermodulation components. It should be as high as possible for a decent receiver/LNA. If a weak signal is accompanied by two strong interferers that exhibit third-order non-linearity, one of the intermodulation (IM) products will fall within the band of interest, thereby contaminating the desired component. The term 'intercept point' (IP) was used to describe signal distortion caused by third-order intermodulation between two neighboring interferers. It is determined via a two-tone test in which two signals of identical amplitude are used. The level of the input signal at which the third-order IM product has the same power as the fundamental is referred to as the two-tone input-referred third-order intercept point (IIP_3), while the corresponding output level is referred to as the output third-order intercept point (OIP_3). The dynamic range of a receiver is defined as the ratio of the highest input level that it can tolerate to the lowest input level that it can detect. Generally, it should be as high as feasible for a proficient receiver. The maximum level of the input signal determines the amount of distortion produced by the circuit. The circuit's noise contribution determines the lower limit on the input (P_{MDS}). The Figure 2.7 illustrates the calculation of IIP_3, P_{1dB} and dynamic range.

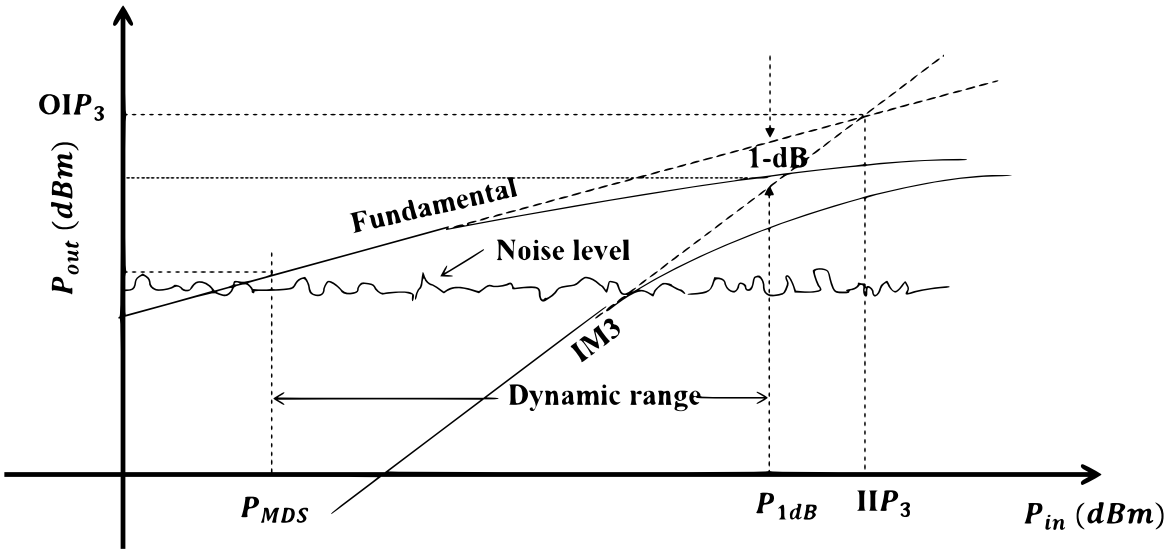


Figure 2.7: IIP_3, P_{1dB} representation (log scale)

2.7 Figure of Merit

The Figure of Merit (FoM) is a quantitative measure of equipment, system, or method's performance in comparison to its alternatives. In engineering, figures of merit are frequently developed for certain materials or devices to ascertain their relative value for a given application. Likewise, the figure of merit for LNA performance analysis is given by relating all the LNA metrics discussed above, such as gain, NF, power consumption, area, and IIP_3. (Wang and Zhang 2020) define the FoM in the following equations 2.32, 2.33 .

$$FoM = \left(\frac{Gain\,[abs] \times B.W\,[GHz]}{P_{dc}\,(mW) \times (NF\,[abs] - 1)} \right) \tag{2.32}$$

$$FoM_{IP3} = \left(\frac{Gain[abs] \times B \cdot W[GHz] \times IIP3(mW)}{P_{dc}(mW) \times (NF[abs] - 1)} \right) \tag{2.33}$$

2.8 Statistical Analysis

Given the Process Voltage and Temperature (PVT) volatility in device parameters, yield analysis is critical for calculating the real yield and confidence levels. The area under a normal Gaussian curve over a specified number of standard deviations is the confidence level. Monte Carlo yield analysis techniques have long been widely utilized

and accepted as a method for yield estimation. The procedure is as simple as conducting a series of trials. Each trial is generated by randomly generating values for yield variables according to statistical distribution parameters, simulating the output, and comparing it to stated performance specifications. The strength of the Monte Carlo method is that its accuracy is independent of the number of statistical variables used and makes no simplifying assumptions regarding the probability distribution of component parameter values or performance responses. The disadvantage of this method is that each trial requires a full network simulation and that a large number of trials is necessary to acquire a high degree of confidence and an accurate estimate of yield. Fortunately, the simulator takes advantage of cutting-edge approaches to dramatically improve the Monte Carlo method's efficiency while maintaining its universality. Statistical analysis or yield analysis estimates the yield by performing a series of trials. Each trial results from randomly generating yield variable values according to statistical distribution specifications, performing a simulation, and evaluating the result against the stated performance specifications. We have performed the Statistical analysis using Keysight Advanced Design System (ADS). The confidence level is the area under a normal Gaussian curve over a given number of standard deviations (σ). ($\sigma = 1$) gives 68.3%, ($\sigma = 2$) gives 95.4% and ($\sigma = 3$) gives 99.7%, of confidence levels respectively. The equation relating number of trials, confidence level, percent error is given by (Miller 2008) :

$$N = \left(\frac{C_\sigma}{\varepsilon}\right)^2 \cdot Y(1-Y) \tag{2.34}$$

Here, N denotes sample size, C_σ is the confidence expressed as a number of standard deviations, ε is the percent error, and Y denotes the yield.

2.9 DoE Analysis

Design of Experiments (DOE) is a data-driven technique for a resilient design that enables you to understand how each design variable contributes to attaining the preceding aim. This method is very helpful for the circuit and design designers to improve the yield (Miller 2008). A typical DoE includes three primary steps:

- Plan the experiment
  - Assess the experimental resource budget

  - Identify the input and response variables
  - Assign levels (values) to input variables
- Perform the experiment and collect response data
- Analyze the data using statistical methods

This methodology can be applied sequentially to improve the statistical performance of a given circuit or system. Due to the inherent trade-off between predictive accuracy and the number of input variables, a screening experiment is used to discover variables that significantly contribute to performance variation. Following that, a refinement experiment might be performed to focus attention on the desired statistical response. In general, DOE procedures are designed to account for the types of errors that occur in any experiment. However, because circuit and system simulators produce similar findings for any analysis with equal input values, the complexity associated with designing, running, and analyzing tests is decreased. Because the experiment is being conducted on a computer, a more full characterization of the input/output interactions may be accomplished. Finally, because the computer conducts the onerous bookkeeping responsibilities during the trial, the likelihood of human error is significantly reduced.

DOE is mostly used to characterize an unknown process. In-circuit or system simulation, the unknown process is used to forecast the behavior of the under-test design (DUT). A straightforward strategy for characterizing a device under test (DUT) is to perturb each input variable (factor) in turn and record the ensuing output response. This strategy, however, fails when the response to a change in one element is dependent on the value of another factor. This computer simulation is done through the Advanced Design System RF platform software by Keysight.

2.10 Fabrication and measurement process

The Fabrication of RF circuits is mainly classified into three types namely CMOS technology, Monolithic Microwave Integrated Circuits (MMIC) and Microwave Integrated Circuit (MIC) or Printed Circuit Board (PCB) fabrication. In that PCB is a board level design using the RF components, while the other two CMOS and MMIC is chip level fabrication. The general CMOS fabrication process is given in the figure 2.8. The Measurement process is usally done through the Vector Network analyzer for

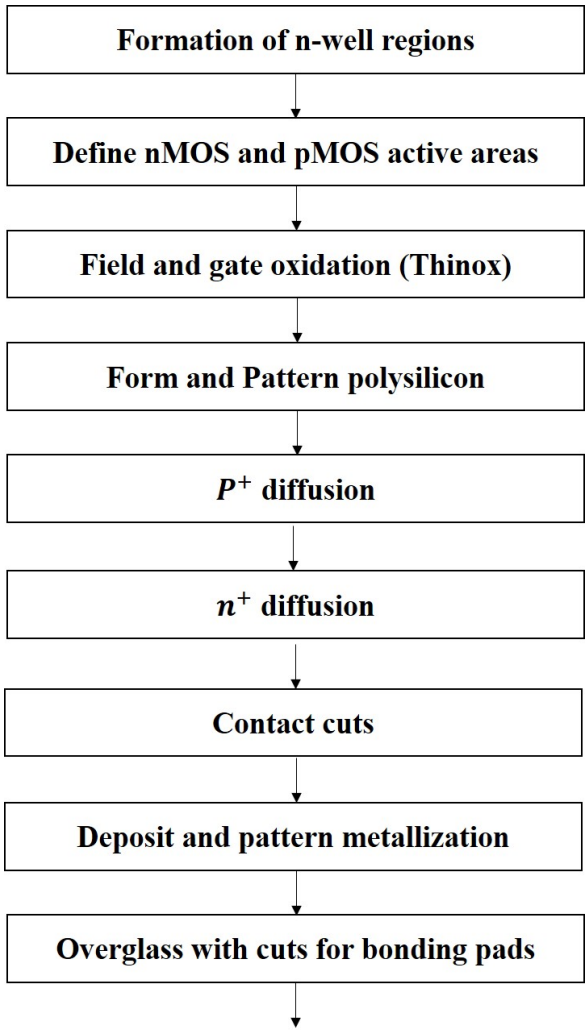


Figure 2.8: CMOS fabrication process flowchart

the calculation of the S-parameter, impedance calculation and Linearity. Nowadays other parameters such as Noise figure can also be calculated using a advanced vector network analyzer such as PNA-X (N5245B) without the need of the other additional equipment. Micro probing station is also needed to probe the die level chip to the PNA.

Chapter 3

BROADBAND LNA DESIGN USING SSL

3.1 Introduction

As 5G wireless networks evolve, the performance of a radio's front end becomes an increasingly crucial component of the RF receiver signal path, particularly in relation to the low-noise amplifier (LNA). With the advent of new process technologies for LNAs such as silicon germanium (SiGe), gallium arsenide (GaAs), and silicon on insulator (SOI), designers must re-evaluate the performance trade-offs associated with LNA parameters such as noise, gain, sensitivity, bandwidth, and power in order to utilize them effectively (Schweber 2018).

The front end's relevance cannot be emphasized because it significantly dictates the system's ultimate performance in weak signal circumstances and achievable bit error rate. If the LNA performance is inadequate, the remaining circuitry and receive channel management design attempts to achieve 5G performance will be in vain. Though LNA determines the overall performance of the RF front-end receiver, the design of the LNA becomes a challenging task due to its operation on a very high frequency. Although there are many 5G bands available, special attention is given to the minimum atmospheric absorption band (28GHz) for integrated mm-wave SoC transceivers (Agiwal *et al.* 2016 and Rappaport *et al.* 2013). A broadband LNA with optimal power, gain, NF, and linearity would be preferable for building an efficient front-end receiver for 5G wireless communication.

3.2 Prior Work

Many works have been reported to design the 5G wireless systems using many topologies such as cascode topology, 4-stage CS, cascaded CG, and CS stages. The traditional design of LNA with these topology does not deliver good design tradeoffs. They either have a good gain or low NF. Recently many microwave components such as coplanar waveguide (CPW), coupler, etc are incorporated into the LNA design to enhance the performance. One such recent notable work based on this is reported in (Keshavarz Hedayati *et al.* 2018), where a 33GHz LNA for 5G wireless systems is designed in 28nm Bulk CMOS. This uses 2 stage cascode stage with microwave components such as CPW. The issue with the reported work is they work in narrowband with bandwidth less than 500MHz and have NF around 5dB. Additionally, metal transmission lines such as coplanar waveguides (CPW), microstrip lines (MSL), and stub lines are far more challenging to integrate into SoC integrated packages due to their electromagnetic (EM) waves fringing around silicon substrates. As a result, they may impair the performance of the LNA. As a result, this work proposes a unique suspended substrate line (SSL) with compatible SoC integrated solutions. SSLs incorporate air cavities into their structure to minimize electromagnetic (EM) losses into the substrates, and so improve the performance of an active component design. The 65nm technology PDK, on the other hand, takes a more suitable approach to SSL in order to ensure excellent electromagnetic compatibility. Samsung's 65nm technology is distinguished by a twin or triple well CMOS process on P-substrate, shallow trench isolation, low resistance nickel salicided polysilicon and diffusion, wire-bond pads or controlled collapse chip connections, and optional electrically programmable fuses. At millimeter-wave frequencies, the design accuracy of active and passive components must be extremely high in order to resolve parasitic connection concerns (Adabi *et al.* 2007) and (Sanduleanu *et al.* 2006).

With new built-in methodologies focusing on high-performance characteristics, LNA design becomes complicated. Additionally, this work prioritizes low loss, low power, and excellent electromagnetic compatibility by evaluating the effects of metal fill and layout design of LNA with SSL and T-shape Junction (MTEE). The authors of (Vigilante and Reynaert 2016), (Elkholy *et al.* 2018), and (Medra *et al.* 2014) recently demonstrated a variable gain in LNAs by changing bias supplies or tunable resistors. (Zhang and Zhao 2018) describes the implementation of a wideband low noise ampli-

fier operating at frequencies spanning from 21GHz to 27GHz for millimeter 5G base stations when the gain is compromised. A low noise amplifier for 5G wireless networks with a forward gain of 15dB and a noise figure of 1.5dB. It was designed in the 3.4GHz to 3.8GHz frequency band. However, this configuration is incompatible with millimeter-wave 5G communication (M Fan wei and J Tseng 2018). A low noise amplifier (LNA) has been reported for a 28GHz communication system for 5G applications, achieving a gain of 30.5dB with a gain ripple of 0.3dB between 24GHz and 30GHz and a minimum noise figure (NF) of 2.05dB at 25.5GHz (Zhou *et al.* 2018).

3.3 Conceptualization and Implementation

While there are numerous LNAs that employ an inductor and a transformer, a transmission line-based feedback LNA is designed to take advantage of the transmission line feedback path's noise cancelling and derivative superposition capabilities(Keshavarz Hedayati *et al.* 2018). This type of LNA exhibits a high degree of linearity and a low noise figure. Using the transmission line, we develop and incorporate unique SSL-based built-in approaches into the LNA design.

3.3.1 SSL Structural Analysis

Few authors such as (Zhen-Qi Huang and Quan-Rang Yang 1988), (Chu *et al.* 2019), (Wang and Ma 2019), and (Wang *et al.* 2017) have recently reported their work on Substrate Integrated Suspended Line (SISL) architectures. These structures were fabricated on Duroid substrates or Duroid/FR4 hybrids with low-loss tangents. However, these structures are needed to interface with other microwave components and are not included in the transceiver's active blocks. (Ke *et al.* 2018) describes the implementation of a dual-band LNA based on the SISL platform on a PCB board, achieving a high-power gain of 28.4dB and ultra-low noise of 1.1dB. However, this printed circuit board structure is incompatible with wideband applications. Additionally, it is incompatible with mobile receiver applications due to its larger area in mm. As a result, this research outlines the process of implementing the SSL structure using wafer technology. Figure 3.1 depicts the suggested suspended substrate line (SSL) in three dimensions, while Figure 3.2a depicts the slicing of individual layers. During the simulation, the left side of the figure serves as Port 1 and the right side serves as Port 2.

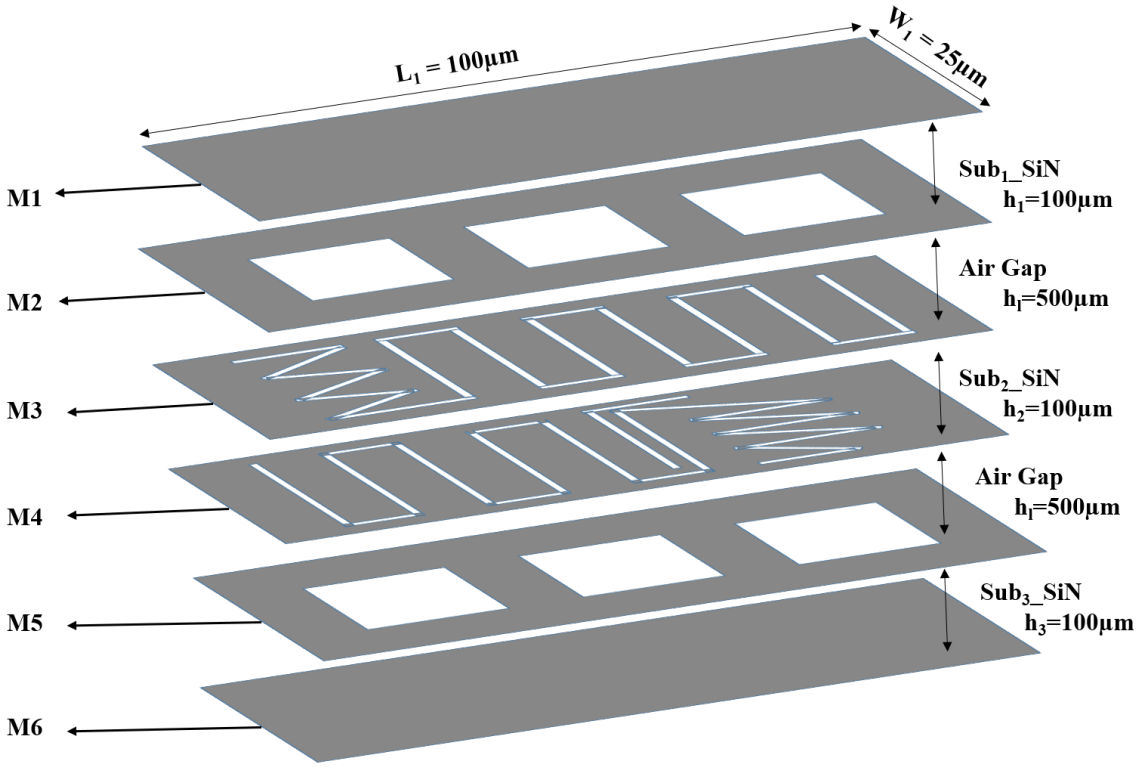


Figure 3.1: 3D Geometric view of proposed SSL

Three substrate layers are stacked in the following order: $Sub_1 - SiN$, $Sub_2 - SiN$, and $Sub_3 - SiN$. To maximize packaging wafer technological flexibility, each substrate is made up of dielectric silicon nitride (SiN) layers with a dielectric constant of 8.5, a loss tangent of 0.0036, a thickness of 100μm, and a maximum operating frequency of 33GHz. M1 to M6 are the metal layers comprised of copper interconnects that are positioned on each side (top and bottom) of the substrate. The thickness of the top metal layer M1 and the bottom metal layer M6 is 12.5μm, which is greater than the thickness of the other dielectric layers, which are 2.5μm, in order to minimize the loss of the electromagnetic (EM) field created inside.

Figure 3.2b illustrates the cross-section of the proposed geometry. The EM fields generated in metal layers M3 and M4 are restricted to the air cavity alone in this case. The vias link the metal layers (M1-M2, M3-M4, M5-M6, and M1-M6). M1 and M6 serve as the ground, whilst M2 and M5 serve as the defective ground for metal layers M3 and M4. The air cavity that exists between all of the substrates traps the majority of the EM fields generated inside, significantly reducing loss and dispersion.

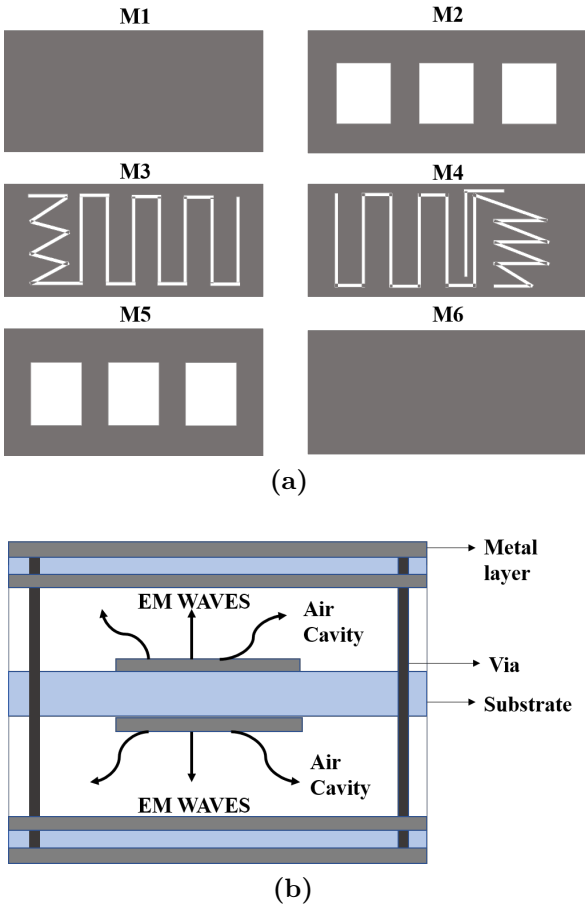


Figure 3.2: SSL component with (a) with splicing of layers (b) side view

As dielectric loss diminishes, the thermal noise generated by the dissipated energy decreases. These impacts are visible in Figure 3.2b cross-sectional area. Hollowed-out metal layers M2 and M5 increase the air cavity between the two substrates. The core substrate, which contains M3 and M4 metal layers, is slotted in such a way that the desired operating frequency is achieved. While the slot pattern in M3 is formed like a W-shaped with rotatory trays similar to the back of a refrigerator, it is noted that this new slotted design functions as a radiator and a way of heat convection. The slotted pattern's width and the airgap (h_l) between the substrate are predicted to be 0.7μm and 500μm, respectively. The vias are utilised to excite all layers between M1 and M6. To characterise the proposed SSL, full-wave electromagnetic simulations using the Methods of Momentum (MoM) are done on the RF ADS platform. The maximum pad radius of 3 via radii and the snap distance of 0.0004 is used to appropriately mimic

the parasitic. Surface current density is depicted in Figure 3.3 using post-processing

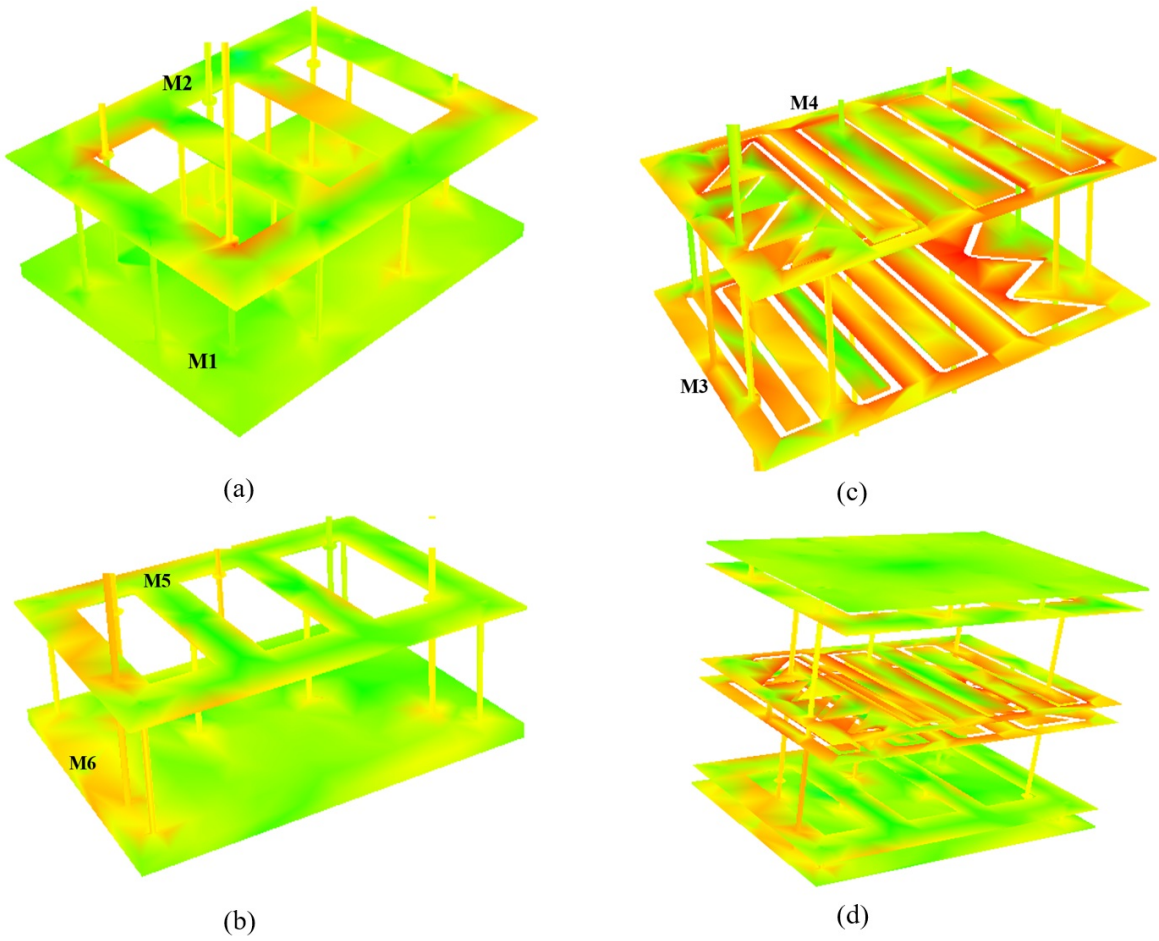


Figure 3.3: Surface Current density of SSL (a. M1 and M2 layers (b) M5 and M6 layers (c) M3 and M4 layers (d) Complete layers

EM simulations and is defined using physics model equations. SSL's characteristic impedance may be modelled using the equations 3.1 (Ma *et al.* 2017), (Chen *et al.* 2018), and (Vecchi *et al.* 2009).

$$Z_0 = 60 \ln \left[\frac{f(r)}{r} + \sqrt{1 + \frac{4}{r^2}} \right] \tag{3.1}$$

where $f(r) = 6 + (2\pi - 6)e^{-(30.666/r)^{0.7528}}$ and $r = \frac{L}{h+h_l}$, L is the length of the M3 layer, h is the thickness of the substrate and h_l is the air gap between substrates. The

effective dielectric constant (ε_{eff}) can be expressed as provided in equation 3.2.

$$\varepsilon_{eff} = \frac{1}{\left[1 + \frac{h}{h_l}\left(h_1 - h_{l1} \ln \frac{L}{h_l}\right)\left(\frac{1}{\sqrt{\varepsilon_r}} - 1\right)\right]^2} \tag{3.2}$$

Where

$$h_1 = \left(0.8621 - 0.1251 \ln \frac{h}{h_l}\right)^4$$

$$h_{l1} = \left(0.4986 - 0.1397 \ln \frac{h}{h_l}\right)^4$$

On layers M3 and M4, the W-shaped structure is embedded back to back with a rotatory tray slot structure. The maximum current intensity on layers M3 and M4 is depicted in Figure 3.3(c). This is evident in Figure 3.3(a) and 3.3(b) as a reflection of the current path on the M2 and M5 layers. The reflection is caused by radiation losses caused by the slotted pattern on layers M3 and M4. On M2 and M5, the hollow rectangular-shaped slot receives surplus current reflection on its surface, resulting in wideband performance. The validity of this assumption is demonstrated by the fact that the effective dielectric constants of suspended metal layers span a large range and may be stated as given in equation 3.3

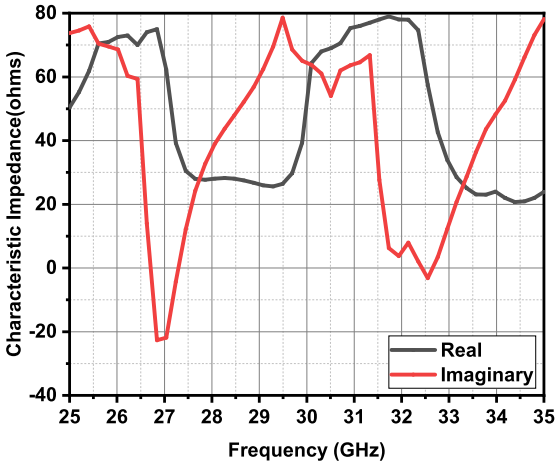
$$\varepsilon_{eff} = \frac{1}{(1 - f_1 f_2)^2} \tag{3.3}$$

Where, $f_1 = 1 - \frac{1}{\sqrt{\varepsilon_r}}$ and $f_2 = \frac{1}{\sum_{i=0}^{3} c_i \left(\frac{w}{h_l}\right)^i}$ and function C_i can be defined as equation 3.4

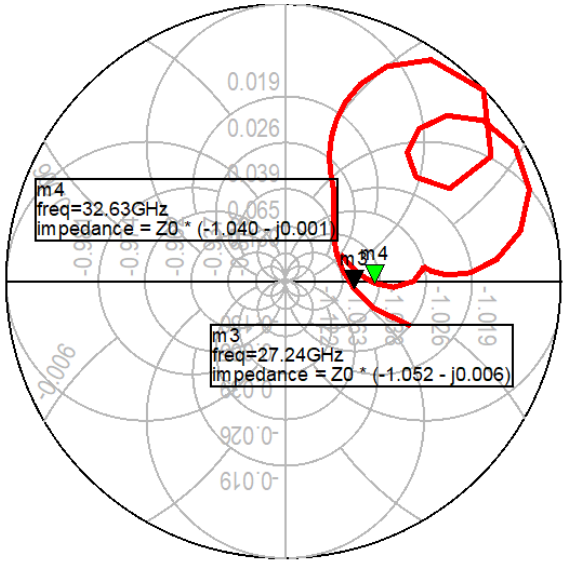
$$C_i = \sum_{j=0}^{3} d_{ij} \left(\frac{h_l}{h}\right)^j \tag{3.4}$$

SSL's characteristic impedance is determined using the above-mentioned relationships, which are illustrated in Figure 3.4a. While Figure 3.4b illustrates the smith chart plot. From an observational standpoint, it is evident that impedance values are almost real for two resonant frequencies of 27.2GHz and 32.6GHz, respectively. And it is observed that the curve is almost entirely within the inductive zone. The proposed SSL's performance measures are initiated with EM wave simulation and analysis. Figure 3.5 illustrates the return loss simulation by altering the air gap between the substrates. To begin, the proposed SSL is designed to operate at a targeted operating frequency of 27GHz and a 500μm air gap distance. At a 500μm air gap, the desired resonance

frequency of 27.2GHz is reached. The complete SSL displays dual-band performance



(a)



(b)

Figure 3.4: Impedance performance of SSL with its (a) characteristic impedance and (b) smith chart

at 27.2GHz and 32.6GHz resonant frequencies, respectively. SSL's linearity versus frequency curve at a 500μm air gap is depicted in Figure 3.6. The fluctuation of resonant frequencies with regard to the airgap between the metal layers of SSL is depicted in Figure 3.7. After accounting for the 0.5mm air gap, it is seen that the initial

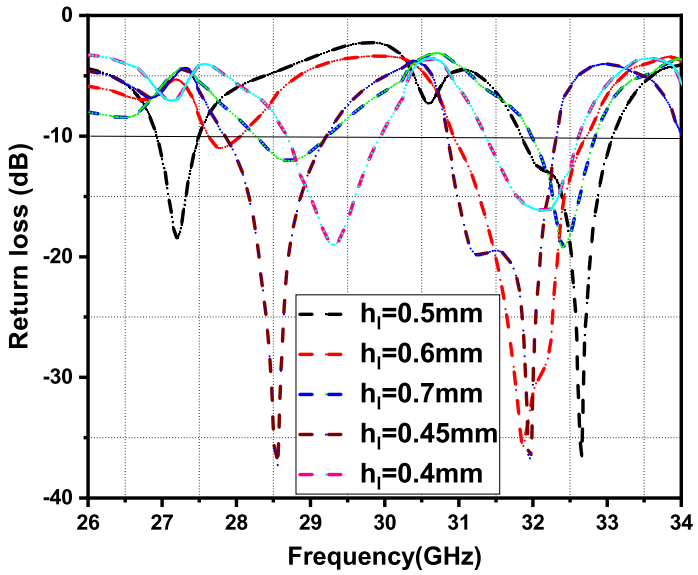


Figure 3.5: Return loss Versus Frequency

resonant band (i.e., 27.2GHz) changed to a higher operating frequency. By contrast, the second resonant band (32.6GHz) lowered the operation frequency down. This is owing to the fact that radiation losses on metal layers are taken into account. This is illustrated in Figure 3.6 by the fact that phases are inverted at both 27.2GHz and 32.6GHz resonating frequencies. Figure 3.8 and Figure 3.9 illustrate the proposed SSL's simulated far-field pattern when phi is set to 90^0. At the first resonating frequency of 27.2GHz, E-phi and H-theta exhibit figure-of-eight forms, whereas E-theta and H-phi exhibit significant lobes oriented more toward 180^0. When the eight-shaped figure begins rotating in the direction of 45^0 at the resonant frequency of 32.6GHz, E-theta and H-phi have large lobes that are inverted towards the direction of 0^0.

3.3.2 Analytical Modeling of SSL Inspired Parallel-Series Network

This subsection covers the design and analysis of an SSL-based parallel-series network, as seen in Figure 3.10a, as well as the layout design in Figure 3.10b. The parallel-series network is motivated by its dual-band operation, which is achieved by the selection of appropriate inductors and capacitors. However, designing high quality-factor on-

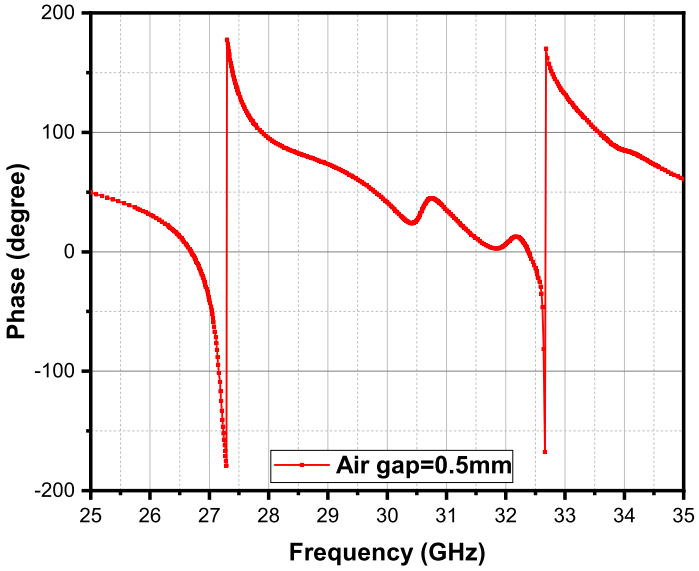


Figure 3.6: Phase versus Frequency

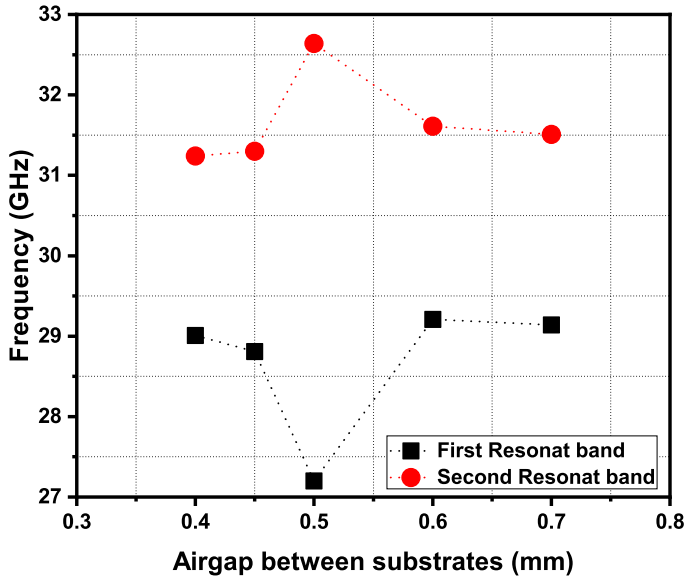


Figure 3.7: Variation of resonant frequencies with respect to airgap between metal layers of SSL

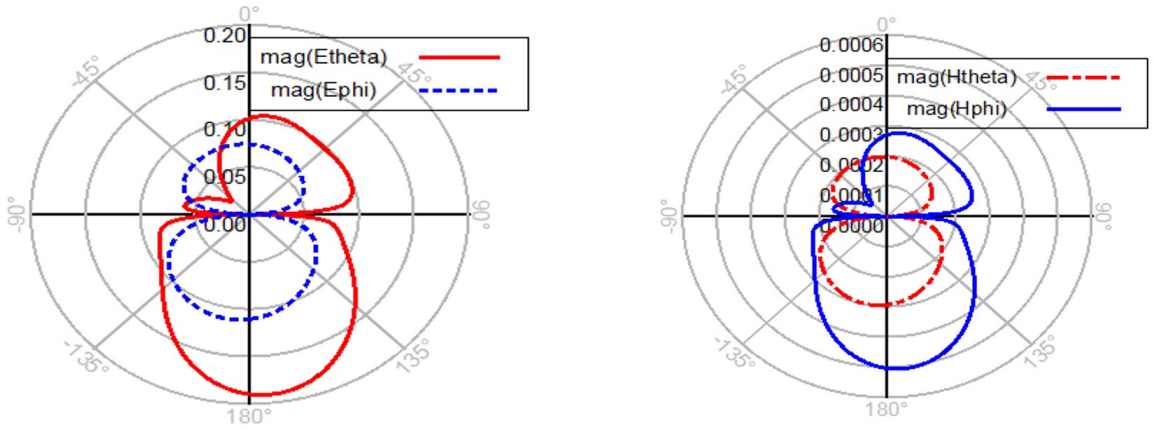


Figure 3.8: The far-field pattern of the slotted metal layer (a) E-theta and E-phi at 27.2GHz and (b) H-theta and H-phi at 27.2GHz

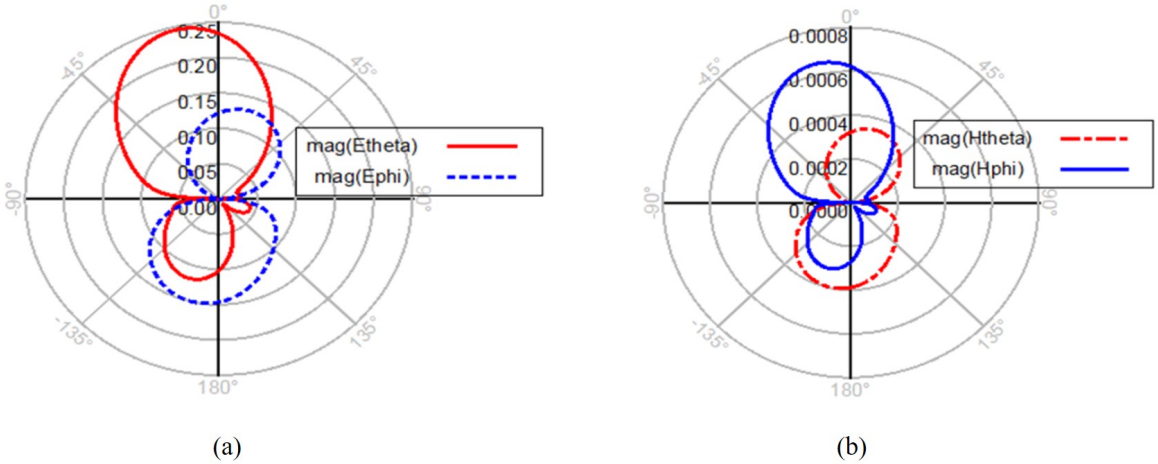


Figure 3.9: Far-field pattern of a slotted metal layer (a) E-theta and E-phi at 32.6GHz and (b) H-theta and H-phi at 32.6GHz

chip inductors at millimeter frequencies is a difficult task, resulting in the network's performance degradation. To circumvent such on-chip design issues, incorporating SSL into such an electrical network is an ideal solution. SSL has a high Q, a wide bandwidth, excellent temperature stability, and is also EM compatible. A parallel-series SSL-based network is made up of a parallel SSL-C network and a series SSL-C network.

This network aspires to have a broad bandwidth. To do this, the proposed network is analyzed for proper impedance matching using the smith chart method. The

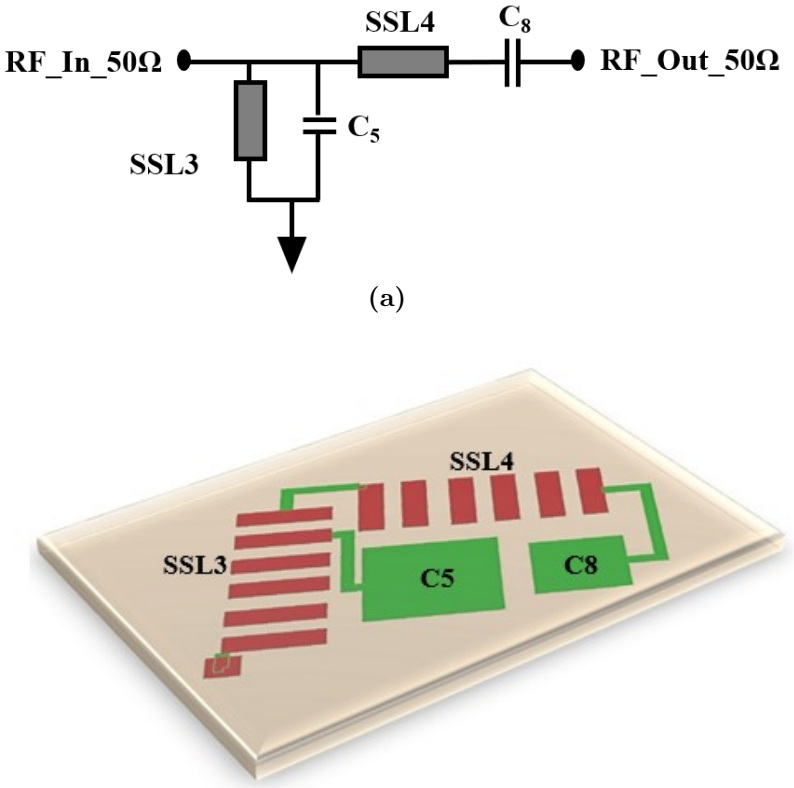


Figure 3.10: SSL based parallel-series network with its (a) schematic and (b) layout design

millimeter-wave technique is based on the assumption of a parallel-series network and the formulation of impedance values using the EM signal of operations. The input source is set to 50Ω to ensure compatibility with the parallel SSL-C network. Similar to the series SSL-C network, a parallel SSL-C network has a shunt output impedance that matches the series SSL-C network. As illustrated in Figure 3.11, the impedance values of both combined networks are estimated using a smith chart for the frequency range of 27GHz to 34GHz. The technique for selecting the optimal load is determined by the matched series SSL-C network's impedance. The optimal impedances are determined between 27GHz and 34GHz, where 27GHz is the network's highest operational frequency. The smith chart graph demonstrates that half of the curve is composed of inductive impedances, while the other half is composed of capacitive impedances. At the operating frequency of 27GHz, the actual impedance is estimated as $(0.904 + j0.512)\Omega$ multiplied by the SSL characteristic impedance. At the last

operating frequency, the impedance is $Z_0 \times (1.035 - j0.544)\Omega$. The ADS platform's

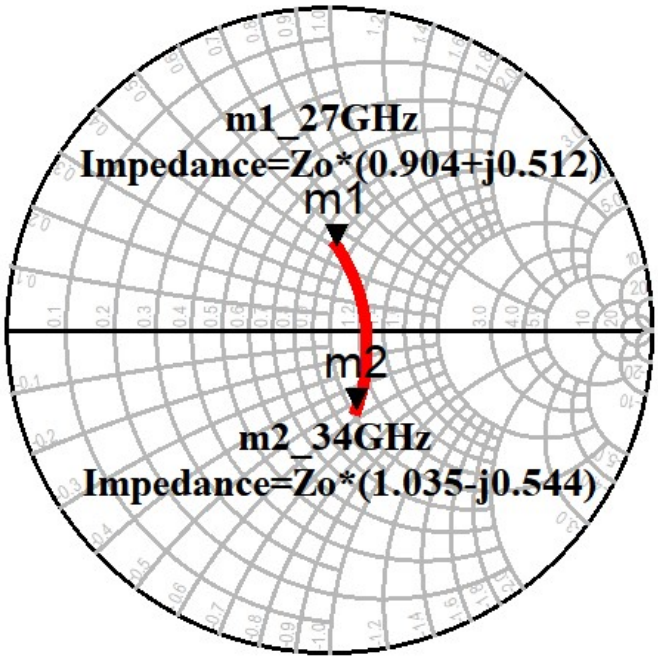


Figure 3.11: Smith chart plot of SSL parallel-series network

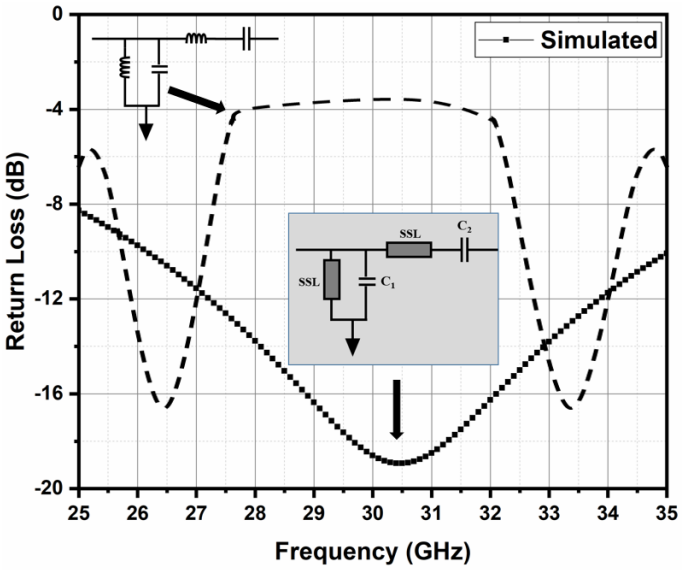


Figure 3.12: Reflection of power versus frequency

EM full-wave simulation generates a return loss curve versus frequency, as depicted

in Figure 3.12. The return loss was seen in both inductor-based and SSL-based networks. The parallel-series network with an inductor displays dual-band performance at two resonant frequencies of 27GHz and 32.5GHz, despite the fact that the output resistance is greater than the input resistance.

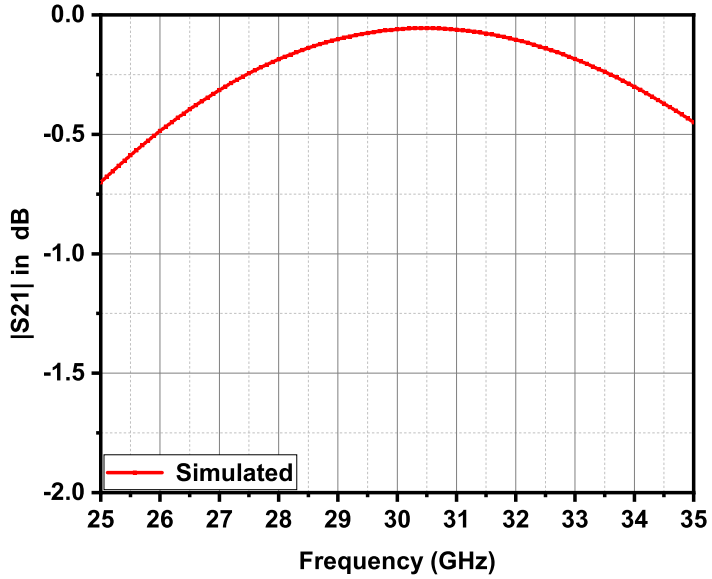


Figure 3.13: Transmitted power versus frequency

On the other hand, an SSL-based parallel-series network operates over a broad frequency range of 27GHz to 34GHz, with a minimum of 30.5GHz. Due to the network's wideband performance, a wide variety of impedance values can be tuned for the proposed LNA architecture. On-chip inductors do not degrade performance; rather, they provide dual-band operation. Because our goal is wideband, we picked SSL. Additionally, inductors are large and generate more noise than a transmission line. The S_{21} performance of the SSL-based parallel series network is shown in Figure 3.13, where the insertion loss fluctuates between -0.4dB at 27GHz and -0.3dB at 34GHz, with a minimum of -0.06dB at 30GHz, producing an inverted U-shape. S_{21} requires that passive components do not induce attenuation of the forward signal and should remain at 0dB. Figure 3.14 illustrates the input impedance of the real and imaginary values of an SSL-based parallel-series network. The values of the input impedance indicate that the network has adequate matching constraints and performs satisfactorily within the required operating band.

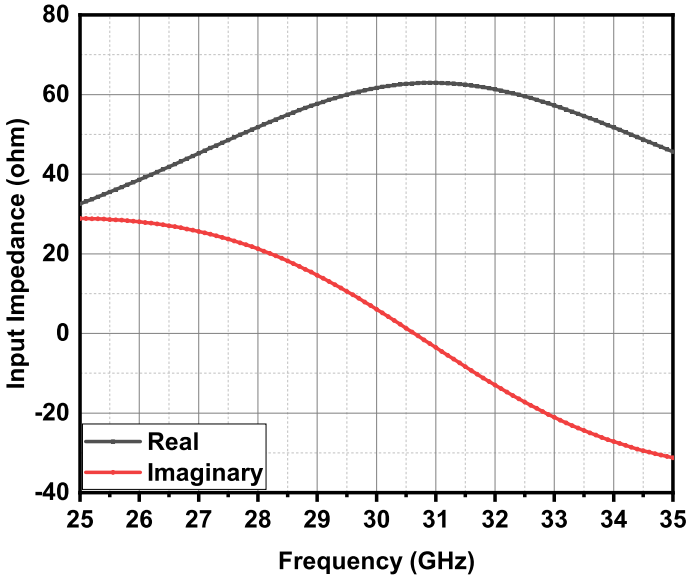


Figure 3.14: Input impedance versus frequency

3.3.3 Built-In Techniques Based CMOS LNA Design

This subsection discusses the design and implementation of a CMOS LNA that incorporates the proposed built-in approaches in order to attain the desired wideband performance. The proposed schematic CMOS LNA architecture is depicted in Figure 3.15. The proposed design features a two-stage cascode topology with an on-chip suspended substrate line (SSL), a T-shape junction (MTEE), inductors, and a MOM capacitor. SSL, MTEE, inductors, and Metal oxide Metal (MoM) capacitors are investigated and characterized using EM full-wave simulations and then optimized for a large Q value. SSL's distinctive individual performance is demonstrated in the preceding section, which demonstrates dual-band operation. SSL transmission lines, designated SSL_1 and SSL_2, are used at the back-end of transistor M2 and M4 to minimize parasitic losses and act as a shield to prevent EM waves from fringing into the lossy silicon substrate, resulting in a high Q value (Vecchi *et al.* 2009). These SSL lines provide the necessary resistance to prevent the current pathway from reversing from cascode topology and to avoid power losses. Other transmission line components, such as SSL_3, SSL_4, and MoM capacitors, have been combined to create a parallel-series network that works as a bridge between the two cascode topologies. It utilizes input

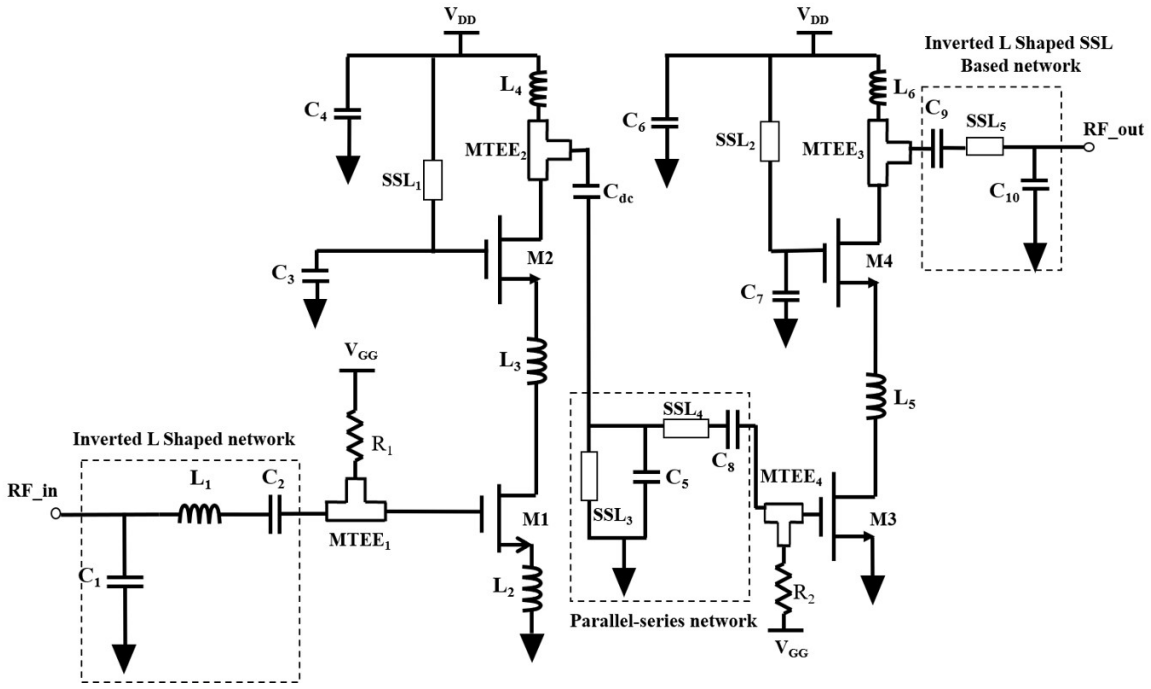


Figure 3.15: Proposed schematic of built-in techniques-based CMOS LNA

inverted L-shaped (IIL) and output inverted SSL-based L-shaped (IIL-SSL) networks to achieve perfect alignment. Though there are other methods for matching inputs, we utilize a simple inverted L shape network because it is straightforward and appropriate for this design. A millimeter-wave complete simulation approach is used to solve both IIL and IIL-SSL networks. The T-shape junction (MTEE) supplies power and connects the SSL transmission lines with little loss. A precise design of the SSL and T-junction is critical for optimizing the architecture utilizing the PDK technology, as parasitic interconnects present a significant obstacle. The transistor layout was created in order to minimize interconnect parasitics, optimize device sizes, and design accurate mm-wave circuits for maximum performance in 65nm CMOS. Each stage of the proposed LNA adopts a cascode topology to improve reverse isolation, gain, and stability at mm-wave frequencies. The inductor L_3 (500pH) with a quality factor of 27 connects the drain-source interconnection's common gate (CG) and common source (CS) transistors for increased gain and to cancel out parasitic capacitances at these nodes. The second stage is meant to provide a higher gain than the first stage while maintaining a slightly lower NF due to the absence of source degeneration inductor L_2. The intra-stage inductors L_3, L_5 (500pH and 122pH with a quality factor of 27)

Comp	Value	Comp	Value	Comp	Value	Comp	Value
L_1	475.8 pH	C_1	1 fF	C_7	2.56 fF	R_1	21.2 KΩ
L_2	613.5 pH	C_2	276 fF	C_8	5 fF	R_2	21.2 KΩ
L_3	500 pH	C_3	0.0021 fF	C_9	36 fF	$M2_W$	39.37μm
L_4	325.4 pH	C_4	0.0101 fF	C_{10}	35 fF	$M3_W$	75.3125μm
L_5	122.215 pH	C_5	189.27 fF	C_{dc}	2.2 fF	$M4_W$	144.025μm
L_6	229.28 pH	C_6	0.0109 fF	$M1_W$	63.875μm		

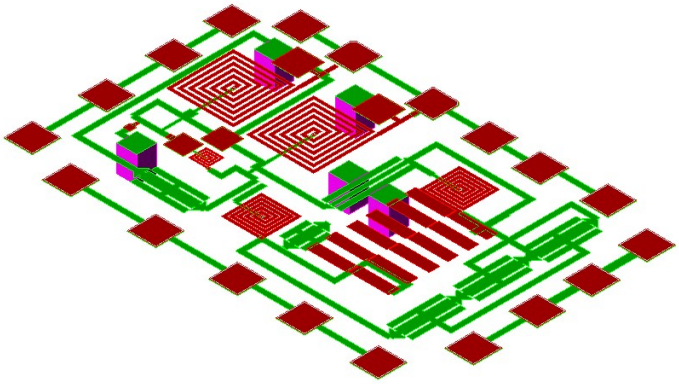
Table 3.1: Optimized values of designed LNA components

and transistor sizes are changed and optimized to transform the source impedance for noise impedance optimization. The aspect ratios of the device designs are employed to optimize the circuit, i.e., $M1 = 63.87/0.065$ μm, $M2 = 39.34/0.065$ μm, $M3 = 75.31/0.065$ μm, and $M4 = 144/0.065$ μm. M1 and M2 have 30 fingers, while M3 and M4 have 32; the finger width is set to 1μm. Matching the input impedance Z_{in} employs inductive degeneration at the first CS stage: L_2 of 613.5pH with a quality factor of 18 degenerates the source of M1 and nearly equalizes the real part of Z_{in} to 50Ω; while L_1 of 475.8pH with a quality factor of 30 in series with the gate nearly cancels out the imaginary part. L_1's quality factor is deliberately selected higher than L_3's because the input inductor's Q has a significant effect on NF. Between the output of the first cascode stage and the matching network is incorporated the capacitor C_{dc}. This is to prevent V_{DD} from being shorted to ground via L_4, $MTEE_2$, and SSL_3.

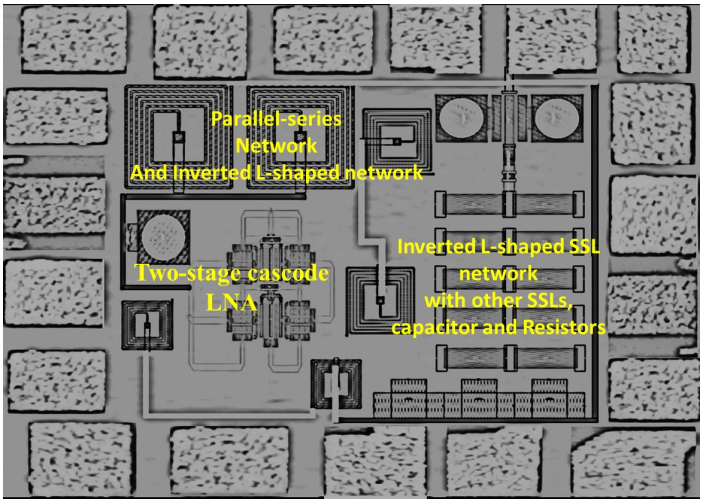
Tuning is used to optimize the load inductors and capacitors for interstage and output conjugate matching. The wideband gain response is obtained by adding the parallel series SSL-capacitor circuit between the first stage's CG and the second stage's CS and allowing it to function at the interstage matching network's resonant frequency. Two frequencies with zero input reactance can be produced using a good parallel to series interstage matching approach. In the 28-32GHz LNA, the parallel SSL-capacitor tank comprised of C_5 and SSL_3 not only resonates at 28.5GHz but also exhibits a broad response spectrum. The second cascode stage provides a larger gain than the first cascode stage while contributing the least amount of noise to the overall circuit. The parameter's value of the proposed LNA design is depicted in Table 3.1. All SSL's width (W) and Length (L) are chosen to be 25μm and 100μm respectively. Similarly, all the magic Tee MTEE dimensions W_1, W_2 and W_3 are chosen to be 25μm , 25μm , and 50μm, respectively.

3.4 Results Discussion

This section discusses the simulation and measurement results. Figure 3.16a and 3.16b illustrate the proposed LNA's layout and die microchip photograph. LNA has an estimated area of $0.35 \times 0.22mm^2$. The LNA is implemented in 65nm PDK technology and is produced utilizing a Magna Hynix Samsung RF 65nm process. The chip is fabricated layer by layer using substrates and MOM capacitors.



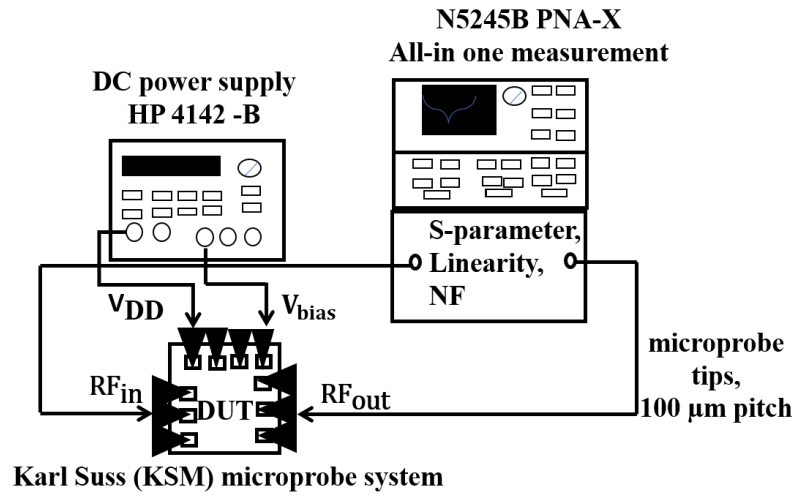
(a)



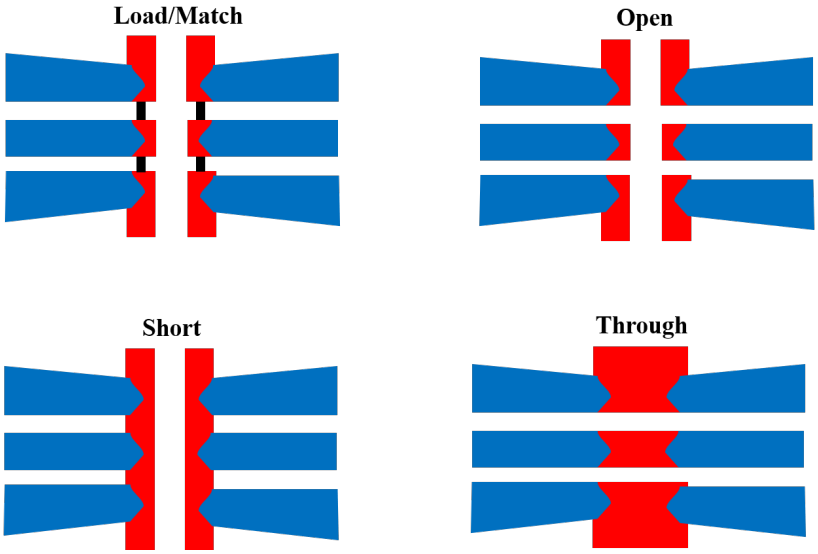
(b)

Figure 3.16: Photographs of LNA with (a) 3D layout and (b) die microchip photograph

On the silicon substrate, SSL and T-junctions are fabricated using the metal-insulator-metal (MIM) arrangement in three modes. The six-layer copper interconnects are produced utilizing a 65nm method that utilizes nanoclustering silica. These



(a)



(b)

Figure 3.17: LNA measurement with its (a) experimental set-up and (b) on-wafer calibration standards

six layers are stacked on silicon wafers alongside other LNA components in 65nm to give flexibility and prevent parasitic losses caused by the CMOS mm-wave process. The passive components are mounted on the silicon chip using the quasi-mode layer method. Full-wave simulations and measurements of LNA performance parameters have defined performance parameters with optimal dimensions to achieve high performance over a wideband of operation. Figure 3.17a illustrates the experimental setup

for LNA measurement. S-parameters are measured for on-wafer LNA utilizing microprobe sets such as the Karl Suss (KSM) microprobe system, Keysight's PNA-X (N5245B) technology up to 50GHz, and Cascade Microtech microprobe tips with a 100μm pitch. Prior to performing measurements, the PNA and micro-probes must be calibrated. Microprobe systems have been calibrated using the short-open-load-through technique. Figure 3.17b illustrates an on-wafer calibration standard. Gold short circuits (Short), gold open pads (Open), and gold plus thin film resistors are included in the calibration sets (Load or Match). These calibration sets are used to accurately get the measured results of the Device Under Test (DUT). Figure 3.18

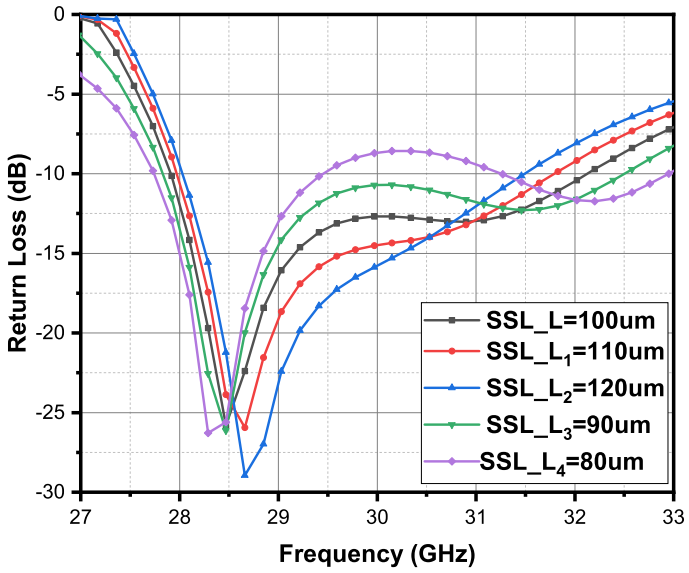


Figure 3.18: Simulated return loss Vs frequency of LNA with varying SSL length

illustrates the simulated return loss versus frequency plot obtained by increasing the SSL duration from 80μm to 120μm. As the length increases, it is noted that the upper sidebands are affected. This is because the surface current density converges at the SSL's edges, increasing the amount of current flowing through the return path. After examining the simulation results, the optimal value of L is deemed to be 100μm. To determine the optimal forward gain of the LNA, the SSL and input-output matching networks are characterized. By varying the length of SSL from 80μm to 120μm, the maximum peak gain of 25dB is achieved for the optimized value of 100 µm, and that can be seen in Figure 3.19. It is also found that at a cut-off frequency of 28GHz,

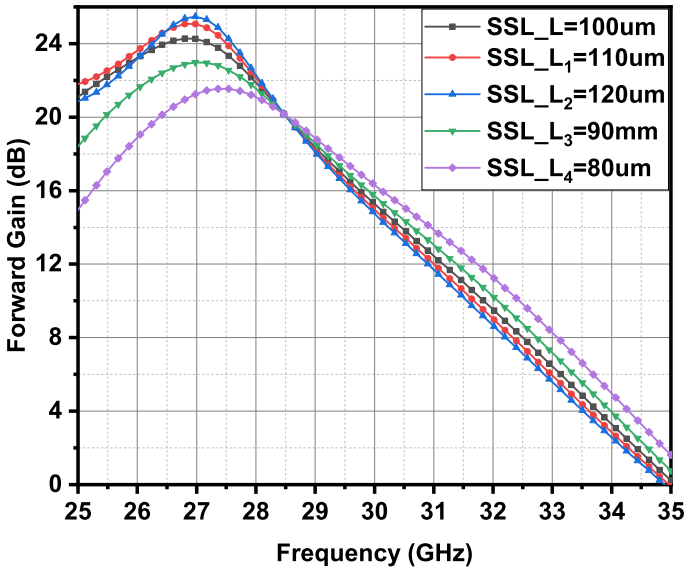


Figure 3.19: Simulated Forward gain Vs frequency LNA with varying SSL Length

maximum gain of 21.5dB is achieved. However, substantial gain is required in 5G

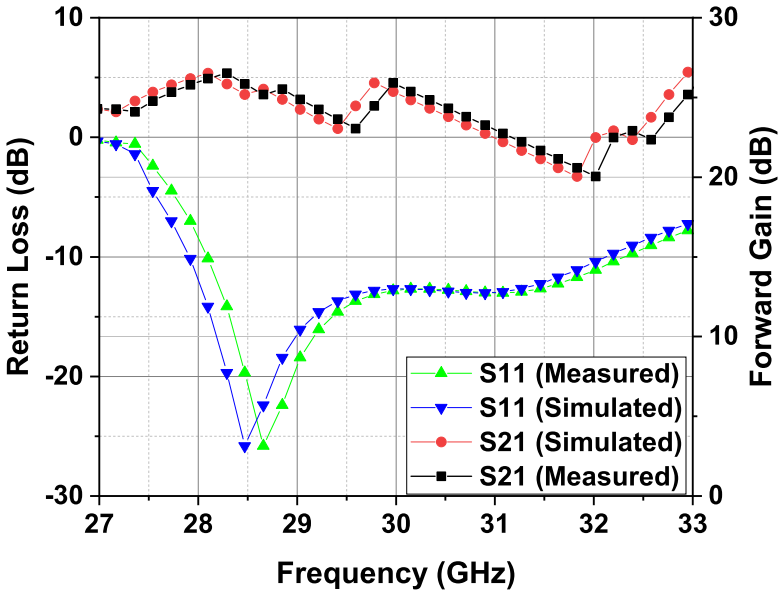
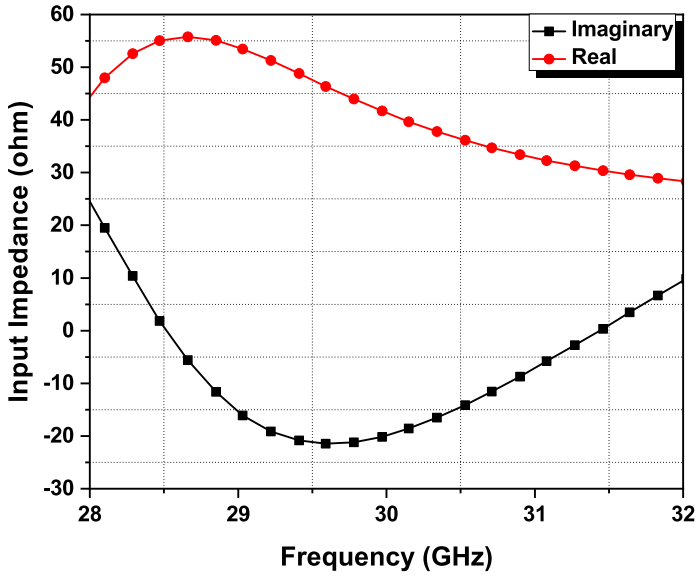
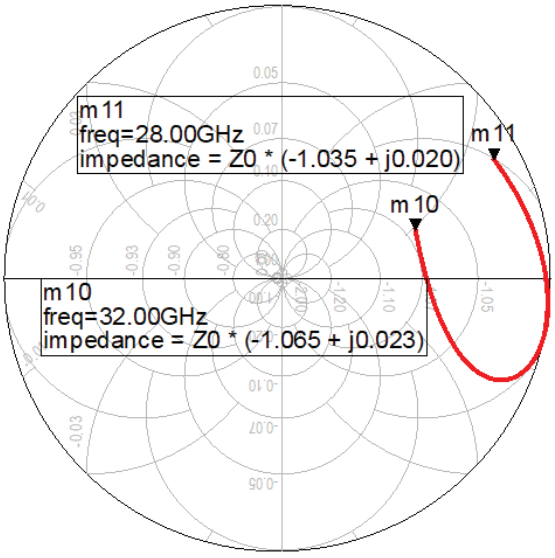


Figure 3.20: S-parameter Vs frequency of LNA with proper matching

wireless networks to achieve intermodulation below the noise floor level. As a result, LNA designs incorporate IIL and IIL-SSL networks as input and output matching networks.



(a)



(b)

Figure 3.21: Simulated input impedance curve versus frequency (a) Rectangular Plot (b) Smith chart Plot

To acquire a wide impedance bandwidth, these networks are solved using a millimeter-wave technique. Figure 3.20 illustrates the variations in return loss and the wide bandwidth achieved between 28GHz and 32GHz. Simultaneously, the forward gain plot in

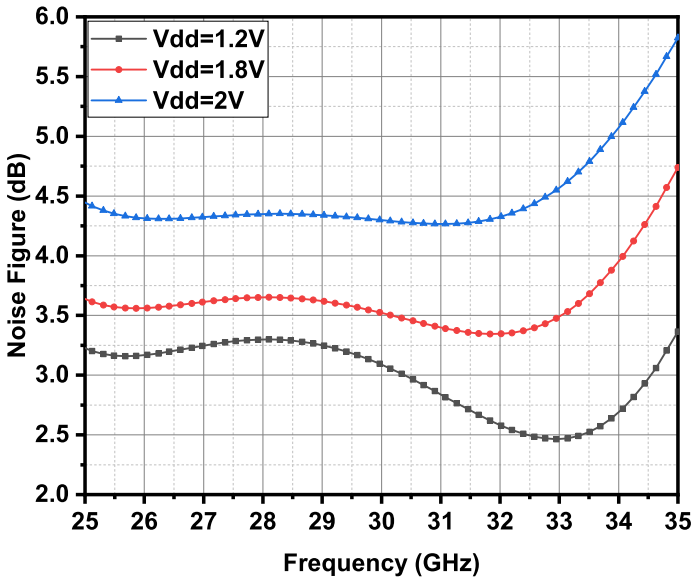


Figure 3.22: Noise figure versus frequency

the Figure 3.20 achieves a gain of 26dB at 28GHz and a gain of 20dB at 32GHz. Additionally, the highest peak gain of 26dB is attained across the intended wide operating band. Gains decrease from 28GHz to 29.5GHz and 30GHz to 32GHz, respectively. This is because of the loading effect caused by cascade stages and SSL-based parallel-series networks that are implemented into the LNA design. Figure 3.20 also illustrates measured return loss and forward gain. The disparity between the measured and simulated values of S_{11} at low frequencies is most likely due to an inaccurate assessment of electromagnetic parasitic effect and concentric inductor impedance.

In Figure 3.21a, the real and imaginary input impedances of the LNA design are plotted, while the smith chart impedance is shown in Figure 3.21b. The above Smith chart plot demonstrates that the U-shaped pattern varies between the first and fourth quadrants. The bandwidth of the LNA design is posses variable inductance mixing both inductance and capacitance and has 50Ω matching limitations. Apart from this, the noise figure of the LNA is determined by varying the dc supply voltage from 1.2V to 2V, as illustrated in Figure 3.22. The optimal noise figure of the LNA is between

3.1dB and 2.5dB when supplied with 1.2V. The rationale for the improved noise figure at lower supply voltage is related to the cascode LNA topology's utilization of inductive load. At higher frequencies, the inductance drops dramatically, allowing for stronger resonant behavior at L_4, C_4, and L_6, C_6. As a result, these product components compensate for internal parasitics, resulting in the lowest noise figure possible for this design. For the RF frequency range, the stability is determined by using the Stability

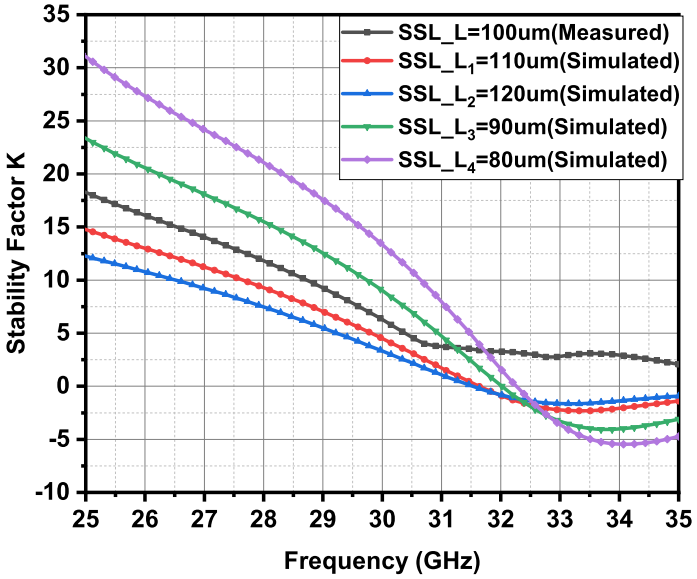


Figure 3.23: Stability factor K of LNA

factor K (SFK) that depends on S-parameters. To achieve stability, it is required to have $SFK > 1$ and $\Delta < 1$. Both SFK and Δ are given by the equations given below

$$\text{SFK} = \frac{1 - |\text{S}_{11}|^2 - |\text{S}_{22}|^2 + |\text{S}_{11}\ \text{S}_{22} - \text{S}_{12}\ \text{S}_{21}|^2}{2\,|\ \text{S}_{12}\ \text{S}_{21}|} \tag{3.5}$$

$$\Delta = |\text{S}_{11}\ \text{S}_{22} - \text{S}_{12}\ \text{S}_{21}| \tag{3.6}$$

LNA stability is measured and plotted in Figure 3.23, where a positive stable point is achieved when L is at 100μm, while for other values of L, the stability falls below 0. The linearity of LNA is measured and plotted in Figure 3.24. The linearity parameter a 1dB compression point (IP_{1dB}) of -19dBm, is achieved at the frequency of 30.5GHz.

The yield estimation of LNA utilizing Monte-Carlo simulation for return loss,

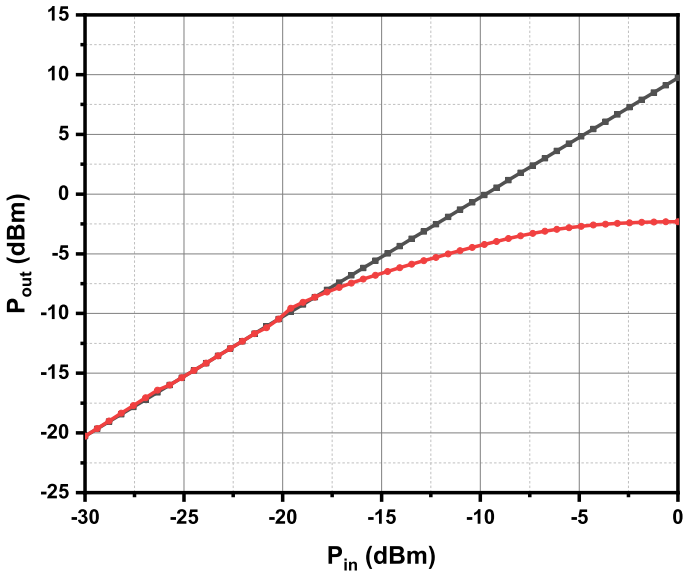
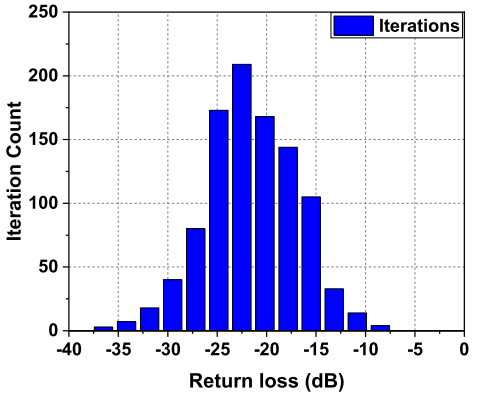


Figure 3.24: Measured 1-dB compressed point of LNA

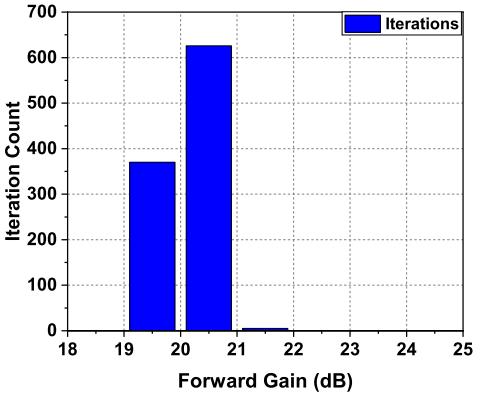
forward gain, and noise figure is presented in Figure 3.25(a), (b), and (c). Under 1000 iterations, the yield percentage is 53.9% with a tolerance of 2% on all components. The figure of merit (FoM) of the CMOS LNA is calculated to be 31.04 at low noise and 18.11 at high noise, respectively. The expression to compute the FoM is given in equation 2.32 Table 3.2 compares the state-of-the-art of LNA to previously published ones.

3.5 Summary

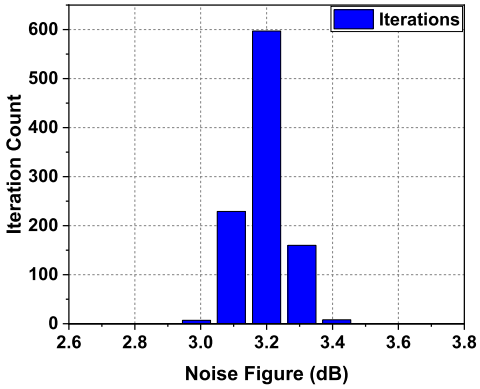
This work discusses a CMOS LNA with a broad bandwidth of 28GHz to 32GHz for a 5G wireless cellular front-end receiver system. The proposed work is the product of extensive experimentation with numerous built-in techniques, including SSL, SSL parallel-series network, and full-wave mm-wave simulation. The SSL is meant to operate in two bands with 50Ω matching limitations. The LNA is constructed using integrated methodologies to achieve high-performance system-on-chip (SoC) IC solutions. Additionally, the fabricated LNA has a wide bandwidth and a maximum forward gain of 26dB. At mm-wave frequencies, a minimum noise figure of 2.5dB is attained with a 1.2V supply voltage. Measurements and simulations are also used to



(a)



(b)



(c)

Figure 3.25: Yield estimation of LNA with (a) Iteration count vs return loss (b) Iteration count vs forward gain and (c) Iteration count vs noise figure

determine the appropriate linearity and stability parameters. The analysis of LNA revealed that the proposed CMOS LNA had the best performance and excellent electromagnetic compatibility, making them ideal for 5G cellular front-end receivers.

Table 3.2: Comparison of the LNA performance with prior works found in the literature.

Parameters	Technology	Topology (μm)	Frequency (GHz)	Gain (dB)	NF (dB)	Power (mW)	IP_{1dB} (dBm)	Area (mm^2)	FoM
Keshavarz Hedayati *et al.* (2018)	28nm CMOS	2-stage cascode	33	18.6	4.9	9.7	-25.5	0.23	8.1
Qin and Xue (2017*b*)	65nm CMOS	CG-CS	7.6-29	10.7	5.6	12.1	–	0.3	10.52
Qin and Xue (2017*a*)	65nm CMOS	cascode	15.8-30.3	10.2	5.7	12.4	-0.5	0.18	10.88
Yu *et al.* (2017)	65nm CMOS	4-stage CS	54.4-90	17.7	7.4	19	-15.4	0.37	10.3
Huang *et al.* (2009)	65nm CMOS	2-stage cascode	50-60	16	3.8	10	–	0.25	15.9
Ameen *et al.* (2017)	65nm CMOS	2-stage CS	26-30	11	1.79	–	–	–	–
This Work	65nm CMOS	2-stage cascode with SSL	27.8-32.5	25	2.5	7.2	-19	0.08	31

– Not calculated

Chapter 4

QUASI CIRCULATOR INTEGRATED LNA FOR X-BAND SYSTEMS

4.1 Introduction

The most important X-band applications include satellite communication, radio astronomy, broadcasting satellites, and radar. The majority of these applications require a low noise receiver to achieve the required sensitivity. The LNA is a critical component of the receiver circuit, amplifying the received signal while minimizing additional noise. The noise figure indicates the amplifier's performance; the lower the NF, the better. The design of the LNA circuit is critical in the receiver. It must consume little power without impairing gain or NF.

Also, the requirement for low-cost, durable, integrated SoC transceivers led the path for developing integrated RF front-end systems that include a circulator, LNA, and PA. One such solution is the RF front end, which is made of nano-ferrite material reported in Jadormio *et al.* 2017. Nonetheless, integrating a CMOS LNA with a ferrite-based circulator results in a significant insertion loss. Generally, circulators were constructed utilizing magnetic ferrite passive devices. A CMOS-based QC is used in this application, a novel design that enhances its performance in terms of gain and low-noise to the amplifier. The LNA is critical in the receiver chain block because it manages the signal-to-noise ratio (SNR), which requires a high gain to amplify a weak signal. Considering both the integrated SoC and performance of LNA, a novel

Quasi circulator integrated LNA, which maintains the highest flat gain, ultra-low NF, low power, and high linearity, is proposed for a full X-band of 8-12GHz in this work.

4.2 Prior Work

The authors in Lu *et al.* 2016 describe a viable design for an X-band LNA with 44dB gain and 7.5dB NF. The authors in Shang *et al.* 2012 report a 55dB increase of LNA with 4.9dB NF. These high gain LNAs are nonlinear and have an extremely high NF, which has an effect on the receiver system as a whole. The authors in Meghdadi *et al.* 2018 describe a very linear X-band LNA with a gain of only 13.6dB. Although the works Kanar and Rebeiz 2014 and Çalışkan *et al.* 2019 describes ultra-low noise LNAs with NFs of 0.77dB and 1.2dB, they have a gain deficit of roughly 10dB. A UWB LNA with a maximum gain of 18.57 dB and a noise figure of 2.4 dB is attained in Kumar and Deolia 2019. This optimises its design using a specific sort of optimization (particle swarm optimization). The disadvantage is that it did not consider harmonics such as third-order intercepts or 1-dB compression points when determining the linearity of the constructed circuit. The authors in Arshad *et al.* 2015 describes a sub-10mW wideband LNA for UWB applications. While the harmonics and linearity are superior to the work in Kumar and Deolia 2019, the gain is only 10.3dB and the minimum NF is 3.68dB. A UWB LNA with double capacitor cross-coupled feedback is stated to have a gain of 21 dB and a noise figure of 2.38 dB in Ghaneei Aarani *et al.* 2019. The work in Meghdadi *et al.* 2020 describes a reconfigurable transceiver device for X band phased arrays with 13.5dB gain and 8.2dB NF.The authors in Dai 2017 presents a low power LNA operating at 0.6V and producing just 11.2dB gain and 3.8dB NF. The authors in Wang and Teng 2016 proposes a variable gain LNA with an interstage reflection type attenuator for the X band. Numerous LNAs with similar topologies are described in Liu *et al.* 2011, Chang *et al.* 2013 and Schwindt *et al.* 2005. The commonality in all of the above-mentioned works is that they have either a high gain with a high NF or an ultra-low NF with a low gain. The aforementioned publications mentioned above concentrated exclusively on LNA design. In X-band wireless transceivers, the CMOS integrated LNA with circulator is used. A CMOS-based quasi circulator for WLAN applications is disclosed in Hsieh *et al.* 2014. It employs a phase cancellation approach for narrowband operation at 2.4 GHz.

4.3 Circulators

Circulators are fundamental three-port nonreciprocal functional blocks that are used to segregate incident and reflected waves in microwave and millimeter systems. The incident signal circulates in only one direction, either clockwise or anticlockwise, to reach the next port. Ports are connected in the reverse direction. Circulator operates in duplex mode by using the same antenna for the transmitter and receiver. The simple circulator pictorial representation is depicted in Figure 4.1. The circulator's three primary parameters are return loss, isolation loss, and insertion loss. The circulator's S-parameters are a three-dimensional matrix comprised of nine entries numbered S_{11} to S_{33}. S_{21} (insertion loss), S_{23}, and S_{32} are critical LNA design parameters for the circulator (isolation). To avoid signal cross-over in duplex mode, the transceiver requires strong isolation, yet it requires low insertion loss to receive a signal. In conjunction with LNA design, the circulator must accomplish the aforementioned two objectives. This is a difficult endeavor, and the proposed Quasi circulator must accomplish these objectives, which will be detailed in greater detail in the following section.

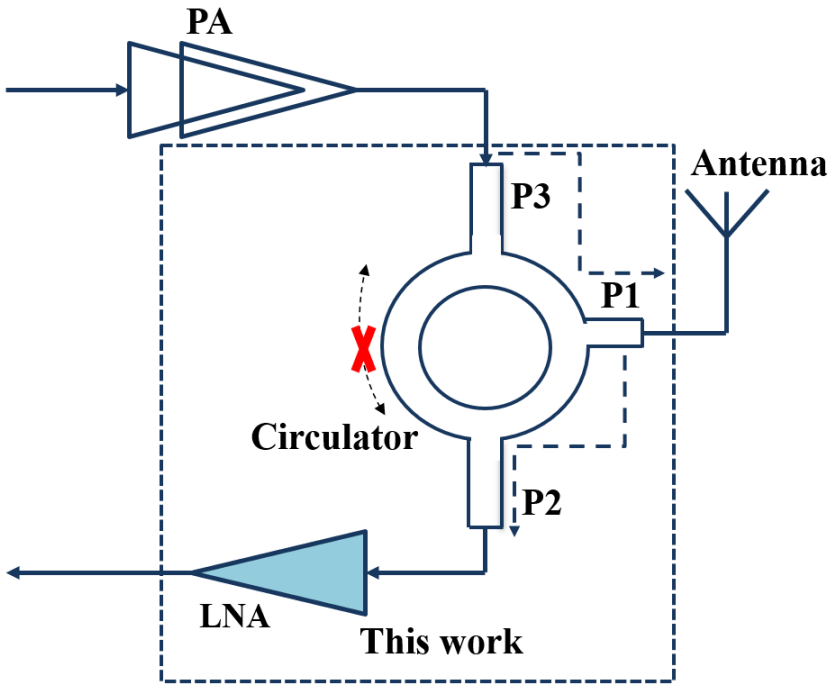


Figure 4.1: Simple Circulator representation

4.4 Quasi circulator

The authors in Shin *et al.* 2008 used the term "quasi circulator" to refer to the circulator's electronic realisation. A quasi circulator is analogous to a circulator, except those two of the three ports are completely isolated in both clockwise and anticlockwise directions. A quasi circulator is one in which power is transferred from the port antenna to the port receiver and from the port transmitter to the port antenna, but not from the port receiver to the port transmitter. The proposed active Quasi circulator with a frequency range of 8 to 12 GHz is depicted schematically in Figure 4.2 as a stage-1. Ports 1, 2, and 3 are used to connect the antenna, receiver, and transmitter, accordingly. Transistors M_{N1} and M_{N2} are included in the current reused cascode stage, which reduces the insertion loss from the antenna to the receiver and improves the receiver's isolation from the antenna. Transistors M_{P1} and M_{P2} are included in another current reusing cascode stage to improve the circuit's stability. L_1, L_2, C_1,

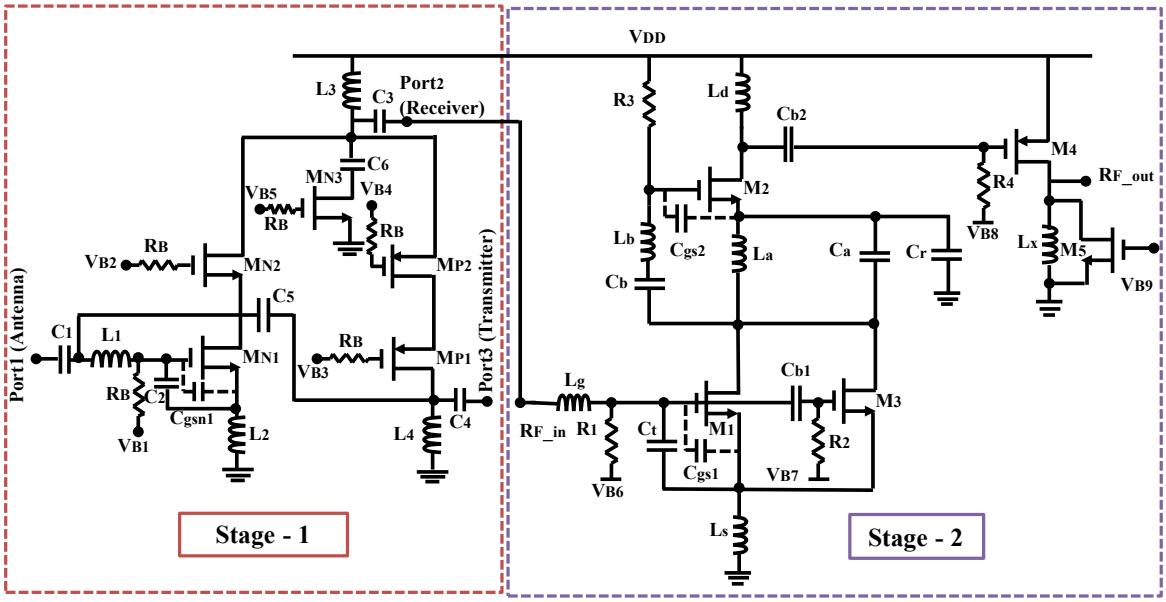


Figure 4.2: Schematic of Proposed QC-LNA

C_2 give input impedance matching to the antenna, while C_4 and L_4 offer transmitter impedance matching. The antenna signal is sent into M_{N1}'s common source stage, which amplifies it. It is transmitted to the receiver via M_{N2}. If sufficient optimization is performed, a minimum gain of roughly 1dB can be attained by gently easing the isolation loss in the receiver path. The M_{N3} with C_6 functions as a magnitude adjustment circuit, taking into account fluctuations in Process, Voltage, and Tem-

perature (PVT) (Hsieh *et al.* 2014). By adjusting the bias voltage of M_{N3}, one can alter the loading capacitance (capacitance in the path of C_6 to ground via M_{N3}), i.e. the magnitude response from receiver to transmitter. This M_{N3} operating in a weak inversion zone will isolate the receiver from the transmitter by enabling the majority of the signal from the antenna to travel through C_3 and a little portion of the signal to the ground via the loading capacitance discussed previously. The signal from the transmitter to the antenna is routed through capacitor C_4 to the source terminal of M_{P1}. It will connect to the antenna through C_5. The antenna's input impedance, Z_{in}, is provided below.

$$Z_{\text{in}} = \frac{g_{mn1} L_2}{C_{gsn1} + C_2} + j \left(\omega_0 \left(L_1 + L_2 \right) - \frac{1}{\omega_0 \left(C_{gsn1} + C_2 \right)} \right) \tag{4.1}$$

Here C_{gsn1} and $C_{gmn1}$are the gate-source parasitic capacitance and transconductance of M_{N1}. Quasi circulator has three ports whose S-parameter matrix is given below in equation. All the S-parameters are essential for the Quasi circulator.

$$[S]_{3\times3} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{4.2}$$

The S-parameters are divided into three categories: return loss (S_{11}, S_{22}, S_{33}), insertion loss (S_{21}, S_{13}), and isolation (S_{12}, S_{23}, S_{32}, S_{31}). S_{22}, S_{21}, S_{23}, and S_{32} are significant in relation to the LNA design that is attached to port 2 of this QC. Figure 4.3 illustrates the simulated S-Parameter plots of the proposed quasi circulator. At the antenna port S_{11}, the receiver port S_{22}, and the transmitter port S_{33}, the simulated input return losses are all greater than 12dB. Across the whole X-band, the simulated insertion losses S_{21} (from the antenna to the receiver) and S_{13} (from the transmitter to the antenna) are 1.1dB and 1.5dB, respectively. Across the full X-band frequency of operation, the isolation between S_{32} (receiver to transmitter), S_{12} (receiver to antenna), S_{23} (transmitter to receiver), and S_{31} (antenna to transmitter) is 40dB, 37dB, 17dB, and 14dB, respectively.

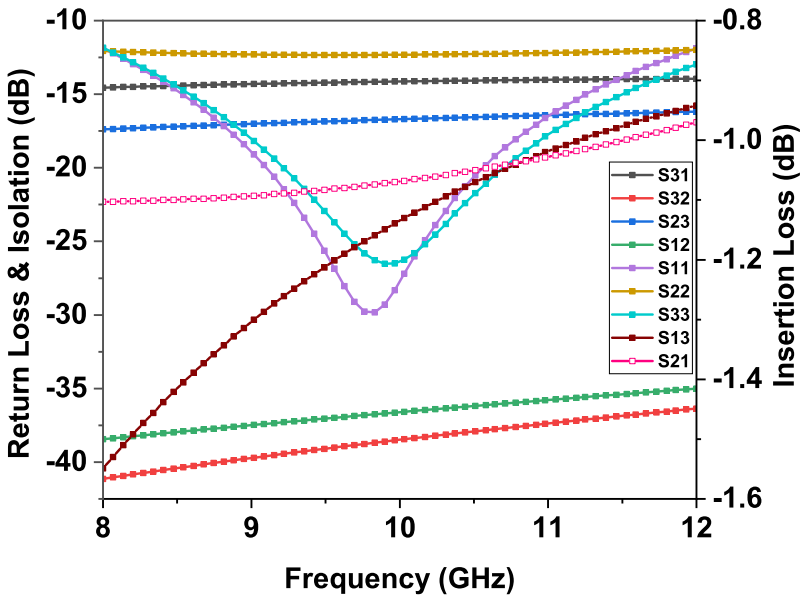


Figure 4.3: Simulated S-parameters variations of QC

4.5 LNA design

Figure 4.2 depicts the proposed QC-LNA. The antenna signal is available at port 2 of the quasi-circulator and is sent to the LNA block through a capacitor C_3. This block implements an input network using an inductive degeneration common source structure. This architecture is capable of delivering a high gain at a low NF and a low power consumption (Yueting *et al.* 2012). The inductor (L_s, L_g), capacitor c_t and gate-source parasitics of M_1 (C_{gs1}) create the required input matching condition. The Z_{in1} expression is given below.

$$Z_{in1} = \frac{g_{m1}L_s}{C_m} + j\left(\omega_0\left(L_s + L_g\right) - \frac{1}{\omega_0 C_m}\right) \tag{4.3}$$

Here g_{m1} is the transconductance of M_1 and $c_m = c_t + C_{gs1} + C_{gs2}$. The transistors M_1 and M_2 are biased with the same current. In DC mode, this LNA circuit block operates as a single stage; in AC mode, it operates as a two-stage. C_r will act as a grounding path for the M_2 source in AC mode, allowing for high gain. The signal is supplied to M_2's gate through L_a, which avoids signal leakage to ground. By avoiding signal leakage, the optimal value of $L_a$with a high Q factor ensures good gain. As a

result, this inductor La is more sensitive to gain. L_a and C_a form a parallel tank to provide a high impedance to the signal for grounding at the operational frequency. L_b and C_b, in turn, produce a series tank with a low impedance at the operating frequency required to transmit the signal to M_2's gate. This then connects the first and second sections of the reused structure. Parallel placement of transistor M_3 to M_1 ensures stability and cancels out third-order harmonics when suitably sized and biased. For a transistor M_1, the third-order intercept point IIP_3 and drain current are calculated as follows (Nikbakhsh *et al.* 2018).

$$IIP_3 = 20 \log \sqrt{\frac{4}{3} \left| \frac{g_{m1}}{g''_{m1}} \right|} \tag{4.4}$$

$$I_{d1} = g_{m1} V_{gs1} + g'_{m1} V_{gs1}^2 + g''_{m1} V_{gs1}^3 + \cdots \tag{4.5}$$

Here g_{m1} is the transconductance of M_1, also g'_{m1} and g''_{m1} are the second and third-order nonlinear coefficients of this transistor, respectively. According to Taylor series

$$g_{m1} = \frac{\partial I_{d1}}{\partial V_{gs1}} \tag{4.6}$$

$$g'_{m1} = \frac{1}{2!} \times \frac{\partial^2 I_{d1}}{\partial V_{gs1}^2} \tag{4.7}$$

$$g''_{m1} = \frac{1}{3!} \times \frac{\partial^3 I_{d1}}{\partial V_{gs1}^3} \tag{4.8}$$

According to equation 4.4, as g''_{m1} is decreased, IIP_3 is increased, and the circuit linearity is ameliorated. To keep g''_{m1} about zero for a wider range of V_{gs1} the transistor M_3 is employed in parallel to M_1. The M_3 works in the weak inversion region. It is biased and sized in a way that the positive peak of the g''_{m3} curve can cancel the negative peak of the g''_{m1} curve. Thus, this improves the IIP_3 of the circuit. The optimum value of g_m for every transistor is required to achieve high gain, and it depends on V_{gs} and W. By optimizing these two parameters, the best g_m could be achieved. The gain contribution by g_m through W will be shown in the next section. The LNA is designed so that it is unconditionally stable ($SFK > 1$) in the specified frequency range. The M_5 in parallel with inductor L_x acts as a variable impedance if it is biased in the deep triode region. To have a maximum gain, load matching is critical, and that can be done if the M_5 is biased in the deep triode region. By

choosing the proper value of V_{B9}, L_x, and W of M_5 that can be achieved, resulting in a high gain at the output. The expression for the total gain is given below.

$$A_{V,T} = A_{v-s1} \times A_{v-s2} \times A_2 \tag{4.9}$$

$$A_{v-s1} = -\frac{g_{m1}}{2} \times \frac{sL_a \left\| \frac{1}{sC_a} \right\| \frac{1}{sC_a} \| \left(sL_b + \frac{1}{sC_b} + \frac{1}{sC_{tot,c}} \right)}{\left(L_g + L_s\right) C_m s^2 + \left(sL_s \| \frac{1}{sC_{ps1}} \right) g_{m1} + 1} \tag{4.10}$$

$$A_{v-s2} = \frac{-g_{m2} C_{b2}}{C_{b2} + C_{tot,n}} \times \frac{C_b}{s^2 L_b C_b C_{gs2} + C_{gs2} + C_b} \times sL_d \left\| \frac{1}{sC_{pd2}} \right\| r_{02} \| \left[\frac{C_{b2} + C_{tot,n}}{sC_{b2} C_{tot,n}} \right] \tag{4.11}$$

$$A_2 = \frac{g_{m4} \omega_0 L_x}{1 + \omega_0 L_x \mu_n C_{ox} \left(W_5 / L_5\right) \left(V_{B9} - V_{th5}\right)} \tag{4.12}$$

Here A_{v-s1}, A_{v-s2}, A_2 are the gain of the first stage, second stage, and gain due to M_5, respectively. R_1-R_4 is large enough to be ignored in all equations. Here g_{m1}, C_{ps1} and C_{pd1} are the transconductance of M_1, the parasitic capacitance at source, and drain, respectively. Here g_{m2}, C_{ps2}, C_{pd2}, and r_{02} are the transconductance of M_2, the parasitic capacitance of source, the parasitic capacitance of drain, and channel resistance of the M_2. The second stage current reused structure, and the variable impedance load stage is modeled as $C_(tot, c)$ and $C_(tot, n)$.

4.6 Integrated CMOS LNA Design

Design optimization is an essential step to achieve the best performance of the QC-LNA circuit. The design goals of QC-LNA are:

- To achieve a flat gain across the entire X-band with minimum variation. It will be instrumental in the place where the signal strength is feeble.
- To achieve the noise figure less than 1.5dB to make a high SNR value.
- To achieve minimum insertion loss in the Quasi-circulator receiver path to avoid the incoming signal strength drop.
- To achieve better isolation above 20dB to avoid cross-interference during the duplex mode.

The Quasi-Newton (QN) control algorithm is utilised in this example because it is an effective way for solving nonlinear equations with a limited number of iterations. Each

objective is defined as a function of a nonlinear equation. The generalized algorithm procedure is reported in (Medra *et al.* 2014).

$$F(x) = 0 \tag{4.13}$$

Here F(x) is considered as a function of gain, NF, and return loss. If x_k is an approximate solution of equation 4.13 then the quasi-newton iterative formula can be described as follows:

$$\begin{cases} x_{k+1} = x_k + B_k^{-1} F\left(x_k\right), \\ B_{k+1}\left(x_{k+1} - x_k\right) = F\left(x_{k+1}\right) - F\left(x_k\right), \\ B_{k+1} = B_k + \Delta B_k, \quad \operatorname{rank}\left(\Delta B_k\right) = m \geq 1. \\ (k = 0, 1, \ldots), \end{cases} \tag{4.14}$$

Here B_k is Broyden rank. This formula is called quasi newton equation when $B_{k+1} = B_k + \left(y_k - B_k s_k\right) \frac{s_k^T}{s_k^T s_k}$ The design steps of the algorithm are shown as a flowchart shown in Figure 4.4. The optimized component values are listed in Table 4.1. Let us consider the circuit's gain; it depends on W_2, L_b, W_3, W_5, and so on. The gain expression is given in equation 4.9 is taken as $F(x)$. The initial value is provided to all the parameter values, such as the width of transistors, inductors, and capacitors which isx_k and it is input to the algorithm. It will compute the gain value and compare it with the goal (30dB). Generally, it will be less, then it will calculate $x_{(k+1)}$ and update the matrix, like this the cycle continues till $F(x_{(k+1)})$ reaches 30dB, which is our goal. The final $x_{(k+1)}$ matrix gives all the parameters values. Like this, all three goals are computed at the same time. By this way the optimized parameter value in the circuit design is computed with a minimum number of iterations also with a minimal computational time.

4.7 Performance Evaluation of QC-LNA

The LNA is implemented using RF 65nm process design technology and fabricated using the Magnachip Hynix Samsung process. The fabricated chip is a layer-by-layer formation using substrates and metal oxide metal (MoM) capacitors. The six-layer copper-interconnects are fabricated using nano-clustering silica. These six-layers are stacked up on silicon wafers along with other components of LNA to provide

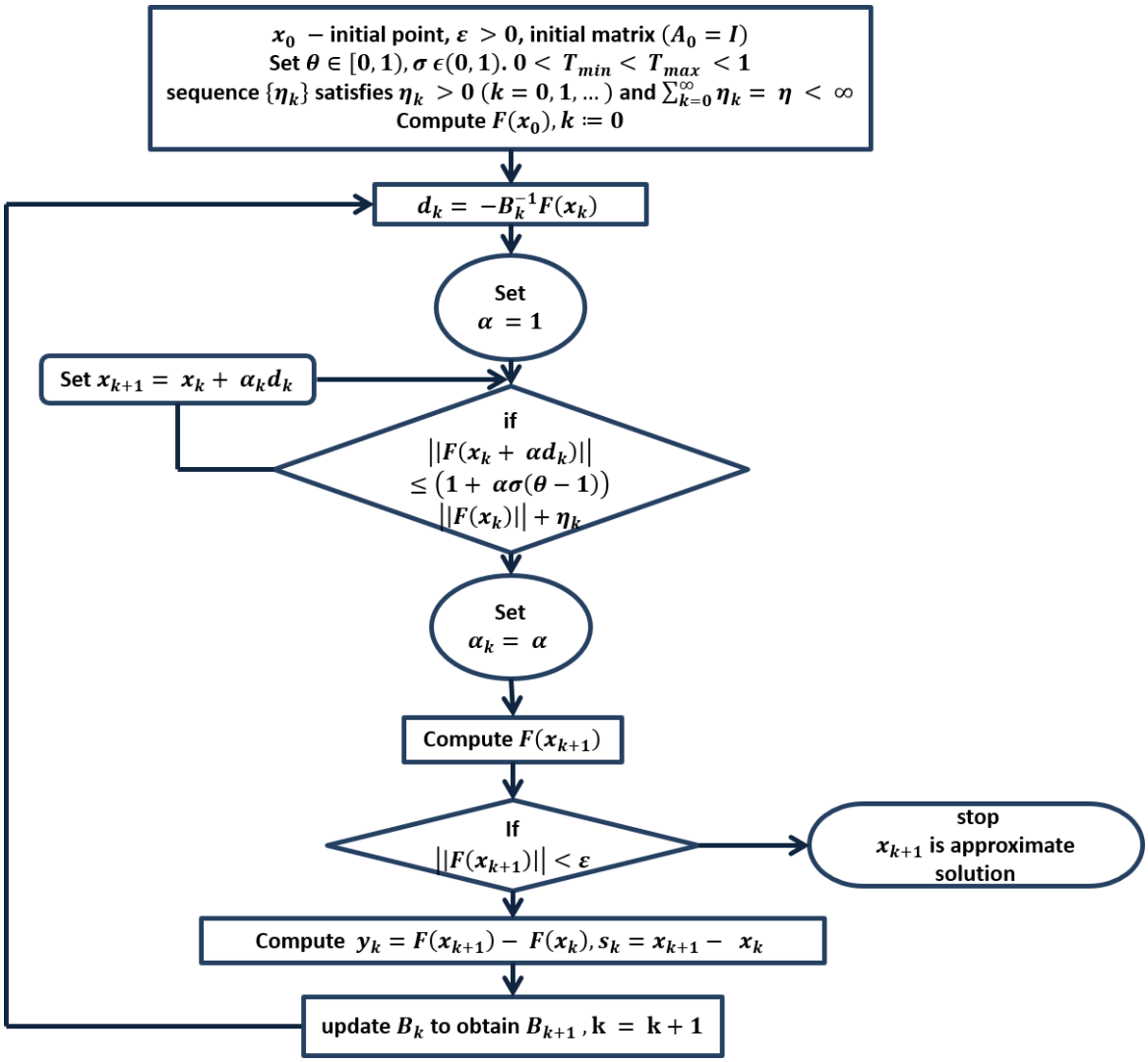


Figure 4.4: Proposed Flow chart for optimization using QN algorithm of QC-LNA

flexibility, which in turn avoids parasitic losses by CMOS mm-wave process. The coils were realized using an RFIC inductor toolkit pre-configured for an RF 65nm CMOS process technology for the Electromagnetic design system in ADS v. 2019. An octagonal inductor with width/spacing is chosen as 9μm/3μmm, and 2.3 of the number of turns have been employed. The stacking multi-layer process is used for mounting the passive components on the silicon die. The microchip die photograph is shown in Figure 4.5. The total core area of the chip is $0.84\times\ 0.52mm^2$. The full-wave simulation and measurement readings of LNA have characterized performance parameters with optimized dimensions to achieve high performance over a wideband

Comp	Value	Comp	Value	Comp	Value	Comp	Value
M_{N1W}	99 μm	C_1	1.6 pF	C_a	0.19 nF	L_d	2.1 nH
M_{N2W}	99.3 μm	C_2	14 fF	C_b	0.53 nF	L_a	2 nH
M_{N3W}	110 μm	C_3	1.2 pF	C_r	0.85 nF	L_b	4 nH
M_{P1W}	5.8 μm	C_4	0.3 pF	L_1	1.7 nH	L_x	1.9 nH
M_{P2W}	1 μm	C_5	0.5 pF	L_2	50 pH	R_1	25 KΩ
M_{1W}	33.8 μm	C_6	0.1 pF	L_3	1.1 nH	R_2	50 KΩ
M_{2W}	23.3 μm	C_t	91 fF	L_4	0.9 nH	R_3	64 KΩ
M_{4W}	99 μm	C_{b1}	0.2 nF	L_g	1.7 nH	R_4	50 KΩ
M_{5W}	99 μm	C_{b2}	0.7 nF	L_s	64 pH	R_B	50 KΩ

Table 4.1: Optimized values of designed QC-LNA components

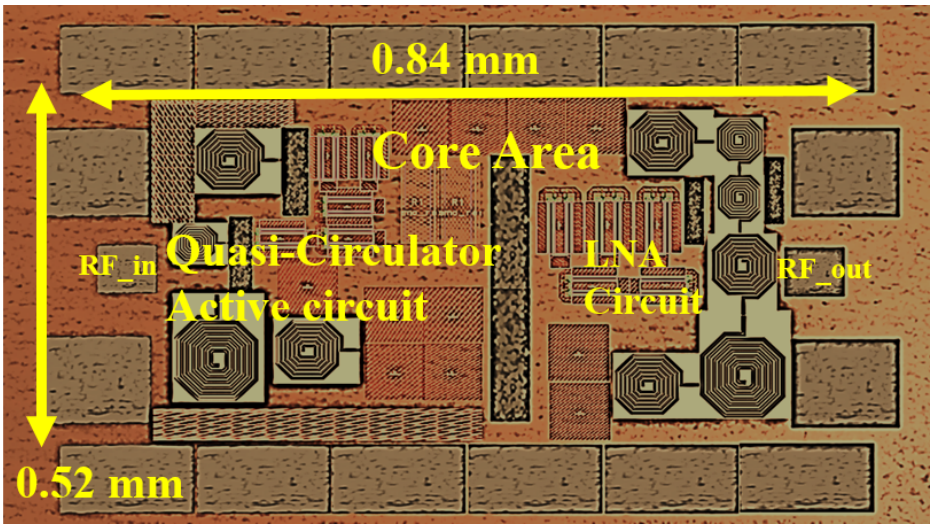


Figure 4.5: Microchip die photo of fabricated QC-LNA

of operation.

4.7.1 Statistical Analysis

As discussed in section 2.8 the yield analysis is essential in estimating the actual yield and the confidence levels. The designed LNA is tested for the error tolerance of 5% and 1% under Gaussian distribution. The results for Gain, NF, return loss are shown in Figure 4.6 (a), (b), and (c) respectively. It is noted that the stable gain of 30dB, NF of 1.5dB, and return loss of 12dB are achieved with 1% tolerance. It results in a yield estimation of 100% , giving a 100% confidence level for 1000 iterations. But for the 5% tolerance yield estimation, 13% of the iteration failed to result in the yield

of 87% . The parameters' limit is set as a minimum 28dB gain, maximum 2dB NF, and a minimum 10dB return loss. But usually, CMOS process PVT variations are less than 1% only, which means the designed QC-LNA provides a stable and accurate design.

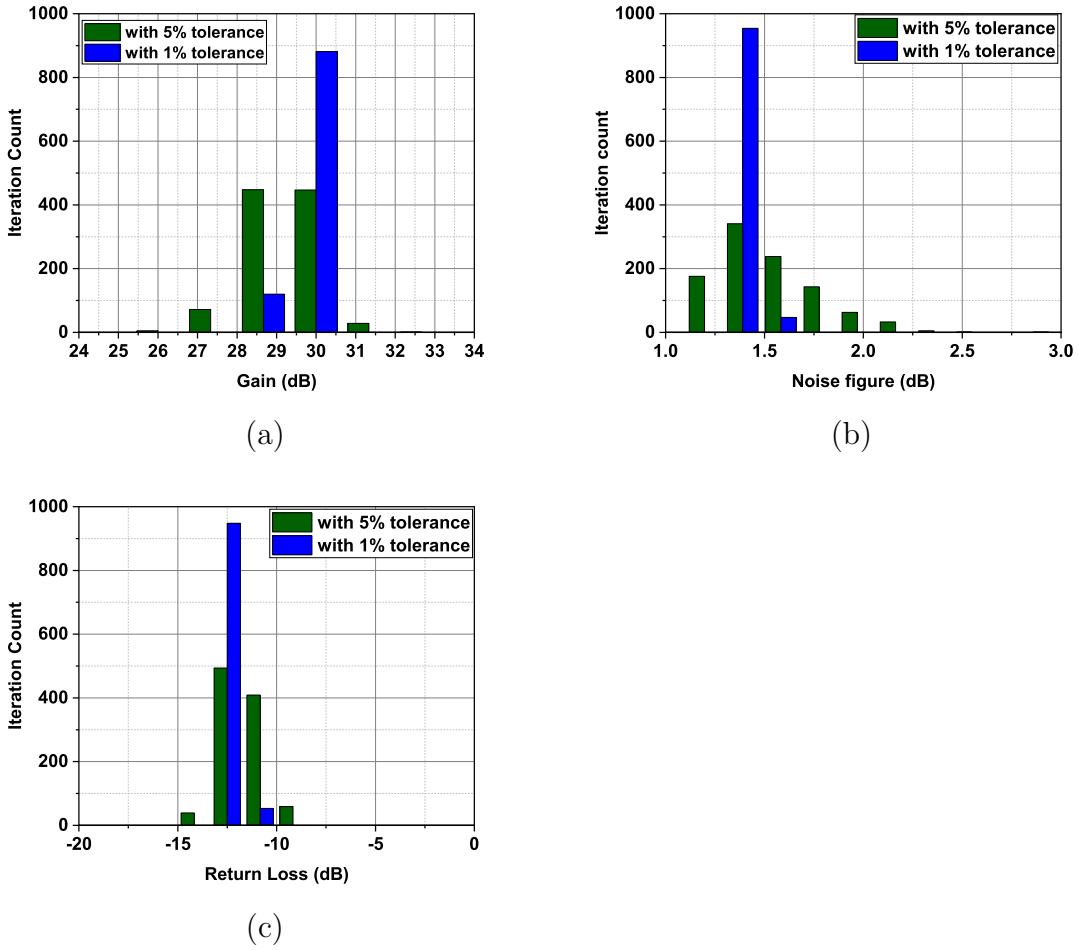
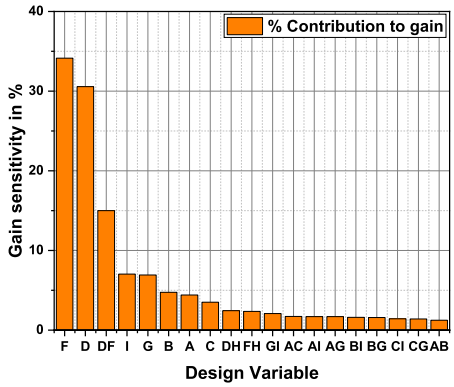


Figure 4.6: Yield estimation of QC-LNA (a) Gain (b) NF (c) Return Loss

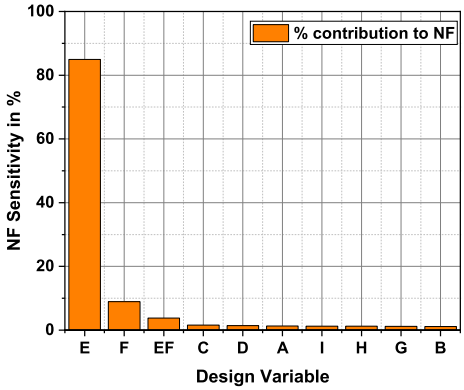
4.7.2 DoE Analysis

As discussed in section 2.9 Design of Experiments (DOE) is a data-driven technique for robust design to understand the design variable's contribution in achieving the final goal listed before. The main design variables and their assigned alphabet are listed in Table 4.2. The results of the design variables vs. contribution to the specific

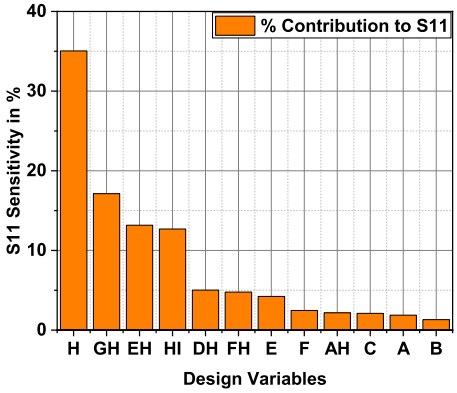
goal such as NF, Gain, and return loss are shown in Figure 4.7 (a), (b), and (c). It is noted that M_{2W}, L_b, and their interaction contribute more than 80% of the gain. So, these two parameters are more sensitive to gain. It is also noted that M_{1W} contributes more than 80% of NF. M_{4W} contributes more than 35% of return loss. The design variables which contribute less than 1% are neglected in Figure 4.7 for better clarity. Extra care has been taken for these sensitive and more contributing parameters while fabricating to get the dedicated, accurate response in the measurement results.



(a)



(b)



(c)

Figure 4.7: Design variable contribution to (a) Gain (b) NF (c) Return Loss

4.7.3 Experimental Analysis

S-parameters are measured for on-wafer QC-LNA using microprobe sets such as the Karl Suss (KSM) microprobe system, Keysight's PNA-X (N5245B) technologies up

Assigned Alphabet	Design variable	Assigned Alphabet	Design variable
A	C_a	F	M_{2W}
B	C_b	G	M_{3W}
C	L_a	H	M_{4W}
D	L_b	I	M_{5W}
E	M_{1W}		

Table 4.2: Design Variables assigned for DoE Analysis

to 50GHz, and Cascade Microtech microprobe tips with a 100μm pitch. Prior to performing measurements, the PNA and micro-probes must be calibrated. Microprobe systems have been calibrated using the short-open-load-through technique. Gold short circuits (Short), gold open pads (Open), and gold plus thin film resistors are included in the calibration sets (Load or Match). These calibration sets are made using the RF 65nm CMOS technology on a silicon substrate. The measurement setup is shown in the Figure 3.17a and 3.17b.

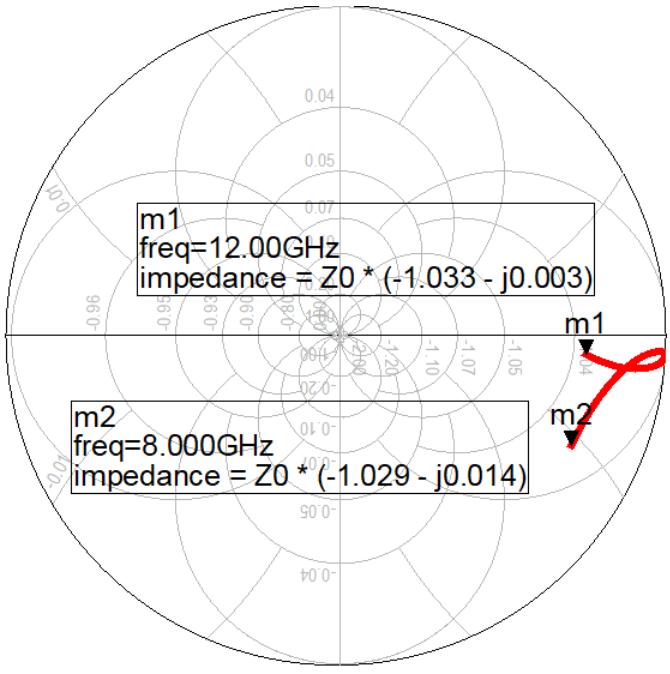


Figure 4.8: Simulated input impedance using smith chart plot

The input impedance of QC-LNA is shown as a smith chart in Figure 4.8. It is noted that the impedance is slightly capacitive due to the dominance of the capacitors C_1 and C_2. Stability of the LNA is mandatory for the circuit to function properly.

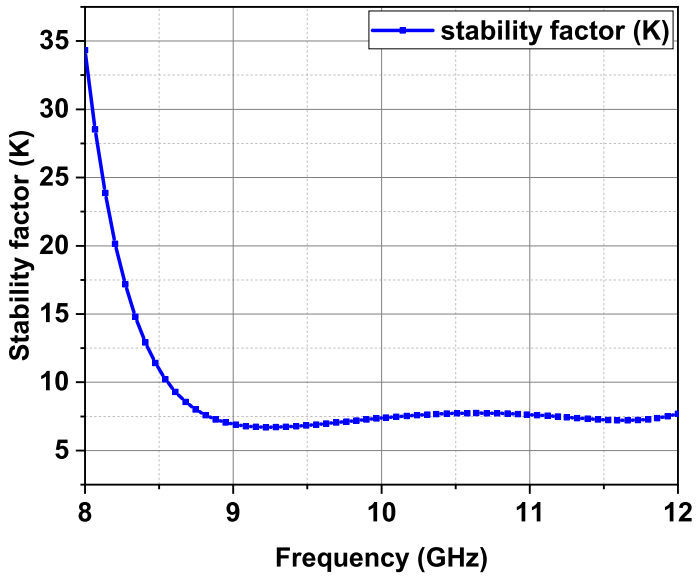


Figure 4.9: Stability factor K of QC-LNA

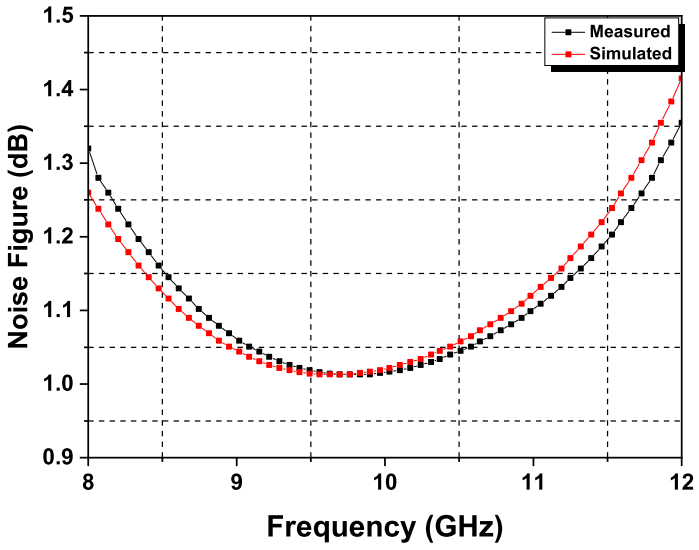


Figure 4.10: Noise figure of designed QC-LNA

The expression for the Stability factor K is expressed in equations 3.5 and 3.6. LNA stability is measured and plotted in Figure 4.9. It is noted that the designed QC-LNA is unconditionally stable in the desired frequency range of 8 to 12GHz.

Figure 4.10 and Figure 4.11 illustrate the measured and simulated NF and S-parameters for QC-LNA. It is noted that the NF ranges between 1.25dB and 1.4dB at 8GHz and 12GHz. At 9.5GHz, it has a minimum of about 1dB. Gain of 30dB is reached with only a 0.5dB variance across the frequency range of 8-12GHz. When compared to the previously stated works, this is phenomenal performance in terms of gain for having such a little variance across the full 4GHz bandwidth.

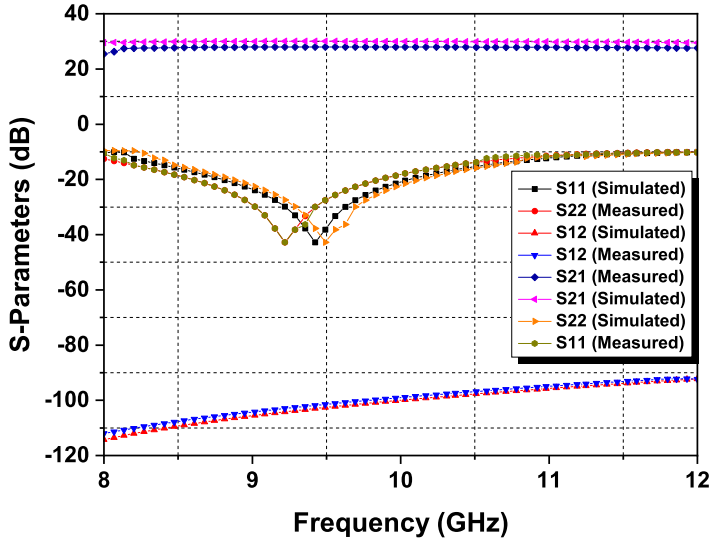


Figure 4.11: S Parameters of designed QC-LNA

The return loss (S_{11}) is sufficiently well below 10dB to avoid any reflection. Other parameters, such as S_{12} and S_{22}, also show satisfactory performance. In Figure 4.12, the measured P_{in} vs. P_{out} (fundamental @ 9.3 GHz) and Pin vs. Pout (Third-order harmonics) to get the IIP_3 and IP_{1dB} is plotted. It is worth noting that the compression point for the Input 1 dB (IP_{1dB}) is -15dBm. At +10dBm, the third-order input intercept point (IIP_3) is obtained. Additionally, the plot demonstrates that the developed QC-LNA achieves good third-order output intercept point (OIP_3) and Output 1dB compression point (OP_{1dB}) values of +40dBm and +13.8dBm, respectively. The Table 4.3 compares the state of the art of the designed LNA to previously published ones, and it shows a phenomenal FoM of 57.4, which is the highest among all the reported works.

Table 4.3: Comparison of the LNA performance with prior works.

Parameters	Technology	Frequency (GHz)	Gain (dB)	NF (dB)	Power (mW)	IP_{1dB} (dBm)	IIP_3 (dBm)	Area (mm^2)	FoM
Hayati *et al.* (2020)	180nm CMOS	3-10.6	13.4	2.3	11.56	-8	–	0.55	8.38
Davulcu *et al.* (2018)	130nm SiGe BiCMOS	8-12	20	1.4	100	-0.75	5.25	0.72	2.2
Li *et al.* (2017)	130nm CMOS	3-12	11.5	4.75	8.5	–	-7	0.86	3.41
Lee and Kwon (2018)	110nm CMOS	3-10	17.6	3.7	2.9	–	-4.6	–	18.6
Çalışkan *et al.* (2019)	130nm SiGe BiCMOS	6-12	10	0.77	19.8	1.5	–	0.4	10.1
Ghaneei Aarani *et al.* (2019)	180nm CMOS	3.1-10.6	21	2.4	4.34	–	-8	1.05	49
Choi *et al.* (2021)	65nm CMOS	6.7-15.3	20	2.1	12.8	-17	-9	0.15	13.3
This Work	65nm CMOS	8-12	30	1.05	10.44 5	-15	+10	0.437	57.4

– Not calculated

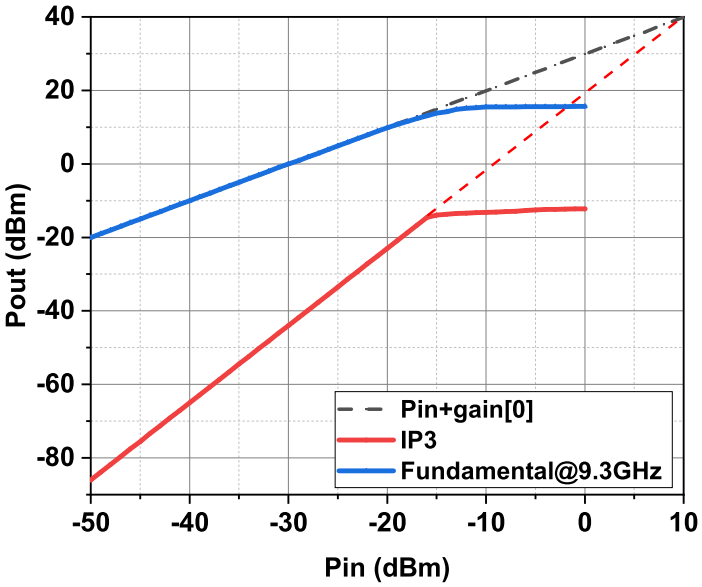


Figure 4.12: Input power(P_{in}) vs. Third order harmonics(IP_3) and Output Power (P_{out} fundamental)

4.8 Summary

The integrated QC-LNA in 65nm CMOS is reported in this work using a two-stage current reuse approach improved using the QN algorithm. The statistical and DoE analyses are presented to evaluate the design's yield and robustness. This QC-LNA produces a constant gain of 30dB with a variance of only 0.5dB throughout the whole 4GHz bandwidth. It achieves an extremely low noise floor of 1dB. By dissipating only 10.44mW of power, the developed QC-LNA achieves IP_{1dB} of -15dBm, IIP_3 of +10dBm, OP_{1dB} of +13.8dBm, and OIP_3 of +40dBm. Losses and mismatches are decreased by integrating QC with LNA. The comparison to state of the art demonstrates that the developed QC-LNA produces reasonably good mean values for all parameters, resulting in the highest FOM.

Chapter 5

LNA INTEGRATED WITH RESONATOR FOR SATELLITE NAVIGATION SYSTEMS

5.1 Introduction

Due to the rapid growth of wireless communication infrastructure in recent years, there is a need for low-cost, robust, and high-performance receivers. Satellite navigation systems are one of the most efficient forms of wireless communication. For instance, a receiver for the Indian Regional Navigational Satellite System (IRNSS) can work in the L and S frequency bands between 1GHz and 3GHz. This study is primarily focused on producing an integrated FBSSIR LNA prototype for the IRNSS receiver, which will be used in smart city projects for intelligent transportation, vehicle monitoring, and precise timing. Figure 5.1 illustrates a typical block diagram of an IRNSS-based transportation management system. Transportation management requires a central server to oversee and monitor all operations, as well as an IRNSS receiver system to communicate between satellites and other devices. This system can monitor the functions of all buses and other vehicles via GSM/GPRS, which is controlled by a central server. The IRNSS satellite transmits continuous signals to the device's IRNSS receiver system and other components (Karthick and Kashwan 2015). The IRNSS receiver device's primary block is a filter and gain stage, often a Low Noise Amplifier (LNA). This work focuses on designing LNA integrated with resonator for satellite navigation systems.

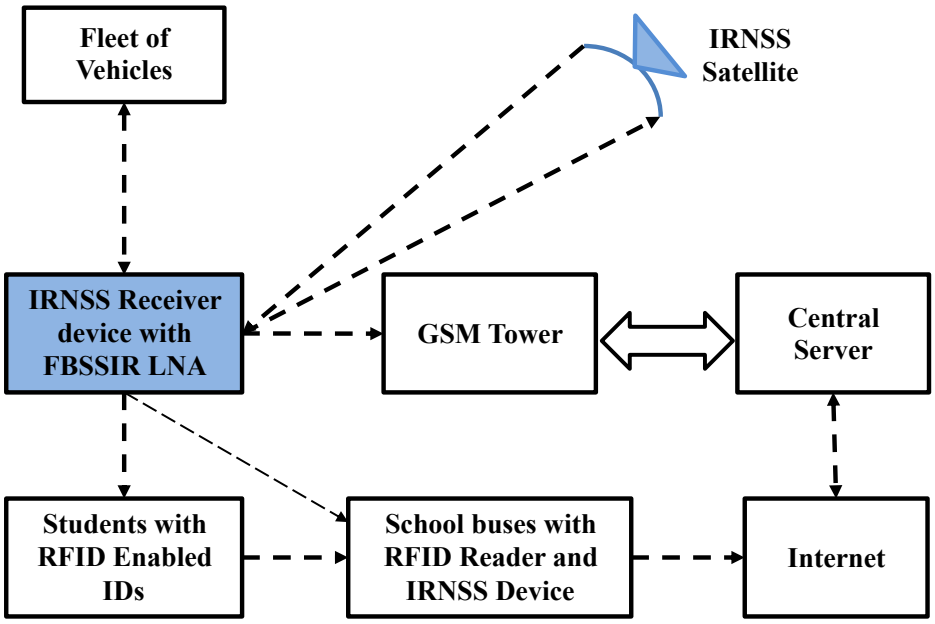


Figure 5.1: Block diagram of a transportation management system using IRNSS receiver

5.2 Prior Work

The primary filters are constructed using either LC or transmission line technology. Inductors and capacitors have higher losses at RF frequencies, and at high frequencies, L might act like C and vice versa. Additionally, a high-value Q inductor increases the circuit's cost. The most cost-effective solution is to use transmission line-based filters. The first microstrip dual-mode resonators is reported in Wolff 1972. Other researchers such as Zhu and Wu 1999, Hong *et al.* 2007, Lee *et al.* 2000, Liao *et al.* 2007 and Zhang *et al.* 2008 later proposed dual-mode filters with varied geometry. (Hong *et al.* 2007) and (Lee *et al.* 2000) demonstrate E-type dual-mode resonators and a non-uniform T-type open stub, respectively. Second-order harmonics were generally seen at $2f_0$ in a standard E-type uniform dual-mode impedance resonator, where f_0 is the center frequency reported in Liao *et al.* 2007. Additionally, there are now four methods for fabricating multi-band Band Pass Filters, with a multimode resonator being the most fundamental of these four. In Luo *et al.* 2011 and Sun *et al.* 2013 ring multimode resonators are shown that combine two or more resonant modes of the multimode resonator. Zhu and Menzel 2003 and Balalem *et al.* 2009 discusses high-frequency selectivity filters in triple mode. Makimoto and Yamashita 1980 discusses the rela-

tionship between harmonic frequency and impedance ratio in a stepped impedance resonator. Jiang *et al.* 2016 presents a dual-band open and short stub-loaded stepped impedance resonator that employs a two-fourth-order cross-coupling method in the transmission path to create the quasi-elliptic response. Yang *et al.* 2005 describes a resonator based on a compact microstrip resonant cell (CMRC). In Hagag *et al.* 2019, they introduced a resonator based on an evanescent-mode cavity, in which they integrated cavity resonator-based LNA co-design and obtained tunable filtering capabilities. Shen *et al.* 2009 presents a three-mode stepped impedance resonator with a sharp skirt and a broad stopband.

The Works reported in Lu *et al.* 2010, Arsalan and Wu 2019, Fouad 2003, Gonzalez 1997, Gray *et al.* 2008 and Fouad 2001 discuss on LNA design without a resonator for wireless applications, and the majority of these works achieved narrowband operation. For instance, Lu *et al.* 2010 describes a microstrip line-based LNA that achieves 2.2-2.6GHz. In Arsalan and Wu 2019, an S-band LNA is developed for satellite navigation systems using microstrip lines with a frequency range of 2.3-2.6GHz. Fouad 2003 discusses an RF cascode BJT-LNA with shunt series input matching. Aneja *et al.* 2021 presents a dual-band microwave integrated circuit (MIC)-based LNA working at 1.1GHz and 2.4GHz that achieves 24.4dB and 20.1dB with 2.6dB and 3dB NF. Bisht *et al.* 2020 discusses a CMOS-based dual-band LNA operating at 900MHz and 2.4GHz with a power gain of 9.3dB and 10.6dB and a noise figure of 3.7dB and 3.1dB.

The limitations of the work discussed above are that all of the resonators have extremely narrow bands and hence cannot be used for wideband applications. Typically, a resonator is built for filtering purposes in a receiver or transmitter; however, creating and testing a resonator on an individual basis is acceptable. However, compatibility concerns, such as impedance mismatch, arise when the resonator is integrated with a Low Noise Amplifier or a Power Amplifier. Except for Hagag *et al.* 2019, none of the works reported and discussed above designed anything other than the resonator.

As a result, this work proposes a novel resonator named Folded Butterfly-stub Stepped Impedance Resonator (FBSSIR) integrated with a core LNA circuit named FBSSIR integrated LNA. FBSSIR uses a Butterfly-open stub and a Folded T-type open stub in the Stepped Impedance resonator's central plane. As two stubs are introduced, two transmission zeros can be obtained simultaneously. The proposed FBSSIR is compact and suppresses the spurious passband compared to the one given in Shen *et al.* 2009. This also provides the required input and output matching to the

core LNA circuit.

5.3 Impedance Match Design Using FBSSIR

This section describes the impedance match design approach using folded butterfly stub stepped impedance resonator. Section 5.3.1 elaborates on the stepped impedance resonator structure's fundamentals, while the proposed FBSSIR structure and its analysis are discussed in Section 5.3.2.

5.3.1 Fundamentals of Stepped Impedance Resonator (SIR)

The basic geometry of SIR and its equivalent circuit diagram is shown in Figure 5.2(a) and (b). To understand about fundamentals of a stepped impedance resonator, a ($\lambda/2$) SIR consists of a low-impedance part (LIP) with characteristic impedance Z_1 and an electrical length of 2θ in the middle while two high-impedance parts (HIP) with characteristic impedance Z_2 and electrical length of θ at both sides is considered. The mathematical relationship between the resonant frequencies, characteristic impedance ratio, and the electrical length of SIR can be represented using equations 5.1 and 5.2 (Chu and Chen 2008).

$$\theta = \arctan\sqrt{R_Z} \tag{5.1}$$

$$\frac{f_{S1}}{f_0} = \frac{\pi}{2\arctan\sqrt{R_Z}} \tag{5.2}$$

Where f_0 is the resonant or central frequency of the SIR, f_{S1} is the first spurious resonant frequency of the SIR, θ is the electrical length of each part, and $R_Z = Z_2/Z_1$ is the characteristic impedance ratio of HIP and LIP. The characteristic impedance of each part with the microstrip as the fundamental structure is determined by the formula given in equations 5.3 and 5.4.

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{re}}} \frac{1}{W/h + 1.393 + 0.667\ln(W/h + 1.444)} \tag{5.3}$$

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{W}\right)^{-\frac{1}{2}} \tag{5.4}$$

Where W is the width of the conductor, h is the thickness of the grounded dielectric substrate and ε_r is the dielectric constant of the substrate. If f_0 and f_{S1} are provided,

the physical size of SIR can be calculated with Equations 5.1, 5.2, 5.3 and 5.4. The input impedance relation for each part of SIR can be calculated as in equations 5.5 and 5.6 (Hou *et al.* 2020).

$$|Z_{in}(l)| = \left| Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l} \right| \tag{5.5}$$

$$|Z_{in}| = \left| Z_0 \frac{Z_L + jZ_0}{Z_0 + jZ_L} \right| \tag{5.6}$$

Where Z_0 is the characteristic impedance, Z_L is the load impedance and $\theta = \beta l; \beta = \frac{2\pi}{\lambda_g}$ and $\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon_{re}}} = \frac{c}{f_0\sqrt{\varepsilon_{re}}}$. To make a folded structure with a gap using SIR, a folded open-loop SIR can be modeled as a coupling capacitor C_m in the equivalent circuit shown in Figure 5.2(c). Now the characteristic impedance Z_0 come along with the electric length of the series step impedance part, and the separated LIP are brief to θ' and $2\theta' + \theta'_s = 2\theta$.

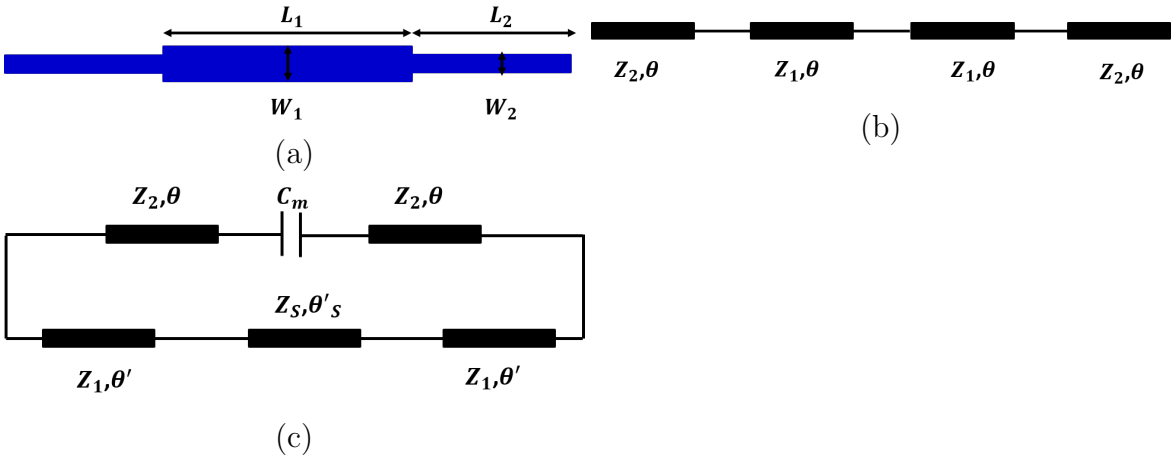


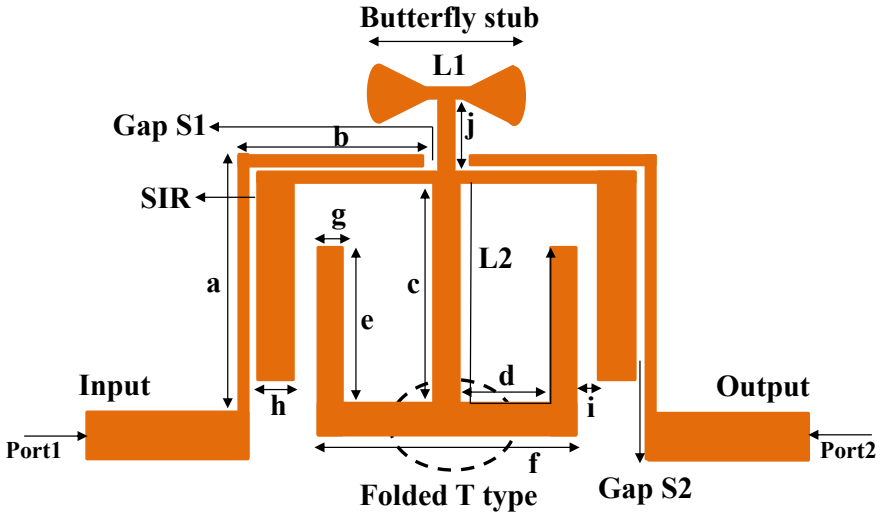
Figure 5.2: (a) Schematic diagram of SIR (b) The equivalent circuit diagram of the SIR and (c) The equivalent diagram of Folded SIR with a gap.

To increase transmission zero and compact size, SIR is bent and incorporated with the folded T-type open stub and butterfly open stub in the central plane with SIR to make a proposed FBSSIR which will be discussed in the next subsection.

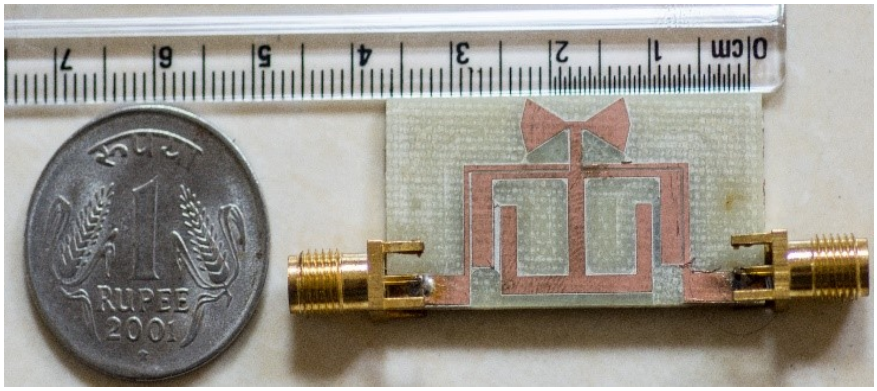
5.3.2 FBSSIR design and analysis

The geometry of the proposed FBSSIR is shown in Figure 5.3a. It consists of a half-wavelength ($\lambda/2$) SIR, a Butterfly type open Stub, and a folded T-type open stub on

its central plane. The physical dimension of the parameters shown in Figure 5.3a are: a=10mm; b=10.5mm; c=9mm; d=5.2mm; e=6.5mm; f=15mm; g=1.5mm; h=2mm; i=1mm; j=4mm and the gap S1=S2=0.2mm. The fabricated top view of the proposed FBSSIR is given in Figure 5.3b. The modeling and simulation of the FBSSIR structure are done using an advanced design system (ADS) v. 2019 RF simulator, while fabrication is done using basic fabricated methods of PCB packaging technology.



(a)



(b)

Figure 5.3: Proposed FBSSIR with is (a) Schematic view (b) Fabricated view

In order to calculate the transmission zeros and better return loss of FBSSIR, the proposed resonator coupling scheme is considered, which is shown in Figure 5.4. This coupling scheme can operate in three modes, two even and one odd mode. The coupling matrix K corresponding to the designed resonator is given in equation 5.7.

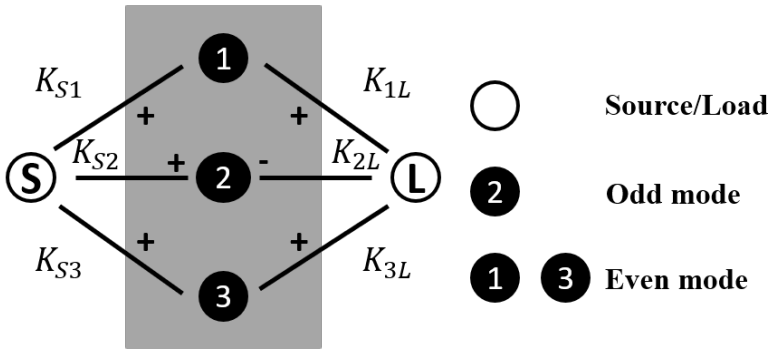


Figure 5.4: Coupling Scheme of the FBSSIR

$$K = \begin{bmatrix} 0 & K_{S1} & K_{S2} & K_{S3} & 0 \\ K_{S1} & K_{11} & 0 & 0 & K_{1L} \\ K_{S2} & 0 & K_{22} & 0 & K_{2L} \\ K_{S3} & 0 & 0 & K_{33} & K_{3L} \\ 0 & K_{1L} & K_{2L} & K_{3L} & 0 \end{bmatrix} \tag{5.7}$$

The above matrix K, $K_{S2} = K_{2L}$, $K_{S1} = K_{1L}$, and $K_{S3} = K_{3L}$ proves that the designed resonator is symmetrical. There is no coupling among the three modes because the split mode frequency and self-resonant frequency are equal. The generalized coupling matrix for the above with transmission zeros at ± 2j and return loss of 20dB is obtained by using the optimization technique from Shen *et al.* 2009 and given in equation 5.8.

$$K = \begin{bmatrix} 0 & 0.451 & 0.779 & 0.451 & 0 \\ 0.451 & 1.05 & 0 & 0 & 0.451 \\ 0.779 & 0 & 0 & 0 & -0.779 \\ 0.451 & 0 & 0 & -0.964 & 0.451 \\ 0 & 0.451 & -0.779 & 0.451 & 0 \end{bmatrix} \tag{5.8}$$

The diagonal elements in matrix K of equation 5.7 and 5.8 are found using equation 5.9

$$K_{i,i} = \frac{(f_0^2 - f_i^2)}{(\Delta f \cdot f_i)} \tag{5.9}$$

The parameters ($f_0 = 2GHz$) and ($\Delta f = 900MHz$) are considered for the central frequency and bandwidth of the resonator, respectively; f_i is the resonant frequency of the i^{th} resonator where the lower band ($f_1 = 1.6GHz$ and upper band $f_3 =$

2.58GHz). The open butterfly stub and the folded T-type stub are found to govern

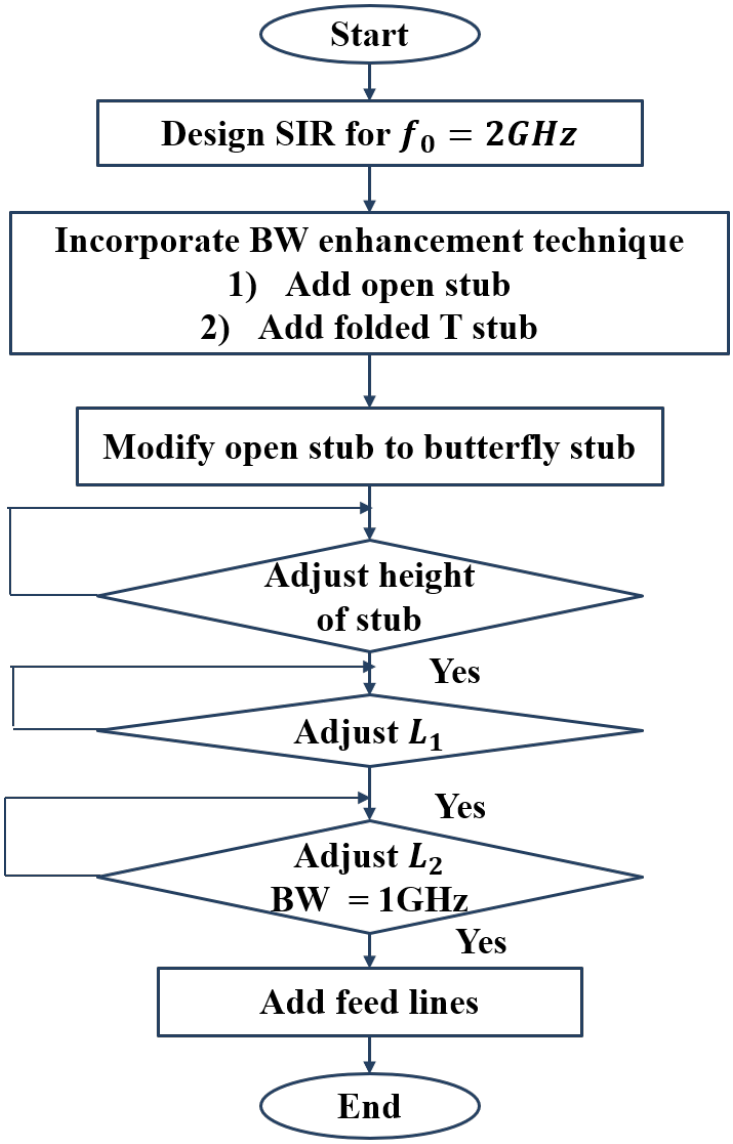
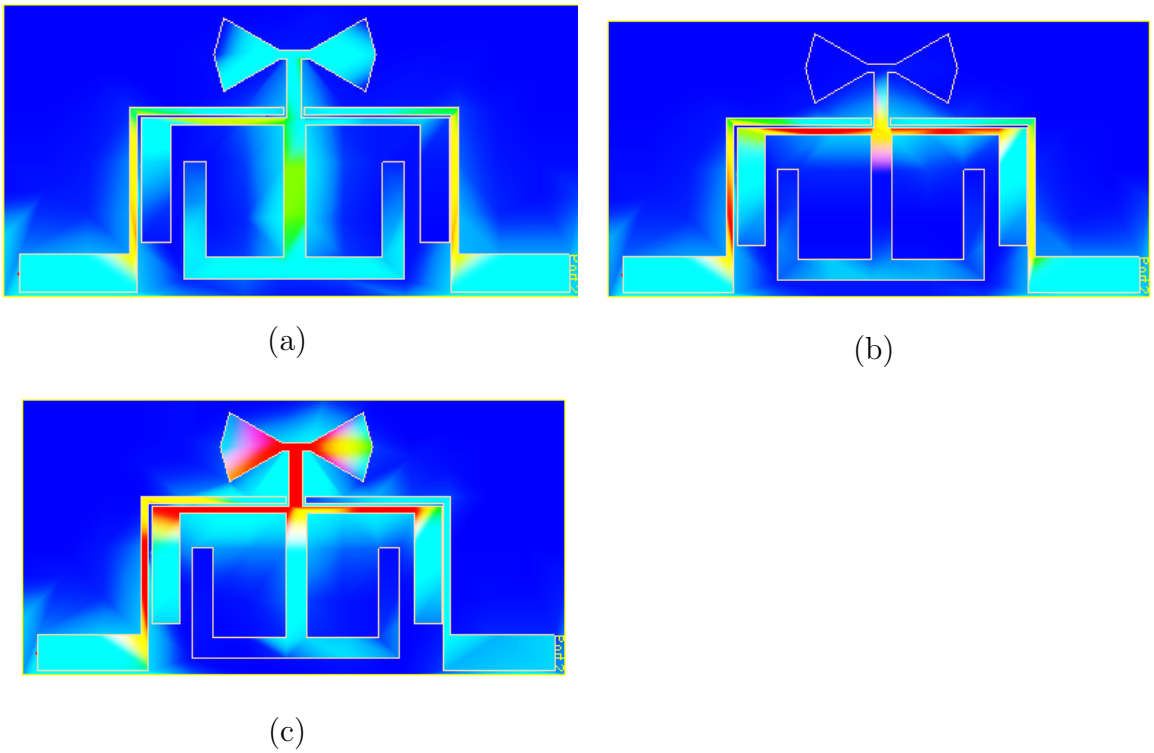


Figure 5.5: Flowchart of the design procedure for FBSSIR

the location of the transmission zeros in the upper and lower stopbands, respectively. The transmission zeros are affected by the width of the butterfly stub and T-type stub. The core frequency and the position of two transmission zeros that affect the bandwidth are primarily determined by the L_1 and L_2 lengths. As the butterfly stub is employed, L_1 consists of the angle suspended by the circular sector (60^0), the breadth (2mm), and the circular sector's outer radius (5mm). L_2 is 20.7mm in length. The variables mentioned here have been optimised, and the flow chart

depicted in Figure 5.5 illustrates the design approach. Figure 5.6 depicts the intended



(a) (b)

(c)

Figure 5.6: The surface current distribution at (a) 1.6GHz (b) 2GHz and (c) 2.58GHz

FBSSIR's simulated surface current distribution pattern for the three modes. The resonator's surface current density is approximated at 1.6GHz, where current begins to flow from input to output port, while at 2GHz, the signal flows exclusively through the SIR structure, as illustrated in Figure 5.6(a) and 5.6(b). While the maximal current density is on the Butterfly stub at 2.6GHz, this indicates that the signal is not reaching the output because it controls the transmission zeros, hence controlling the upper stopband, as illustrated in Figure 5.6(c).

The SIR is designed at a center frequency of 2GHz using the fundamentals and formula in the preceding subsections, and a folded T-stub and butterfly stub are embedded in the plane. The proposed FBSSIR's performance is evaluated using the insertion loss plot given in Figure 5.7. As shown in Figure 5.7, the stub height (j) is changed to obtain the optimal value. Below 4mm, there is a significant loss in signal transmission in the upper sideband, while there is no change above 4mm; thus, the optimal value for height (j) in FBSSIR is 4mm. Additionally, Figure 5.8 and Figure 5.9 exhibit plots of the S-parameters. After varying L_2 between 18.7mm and 21.7mm, it

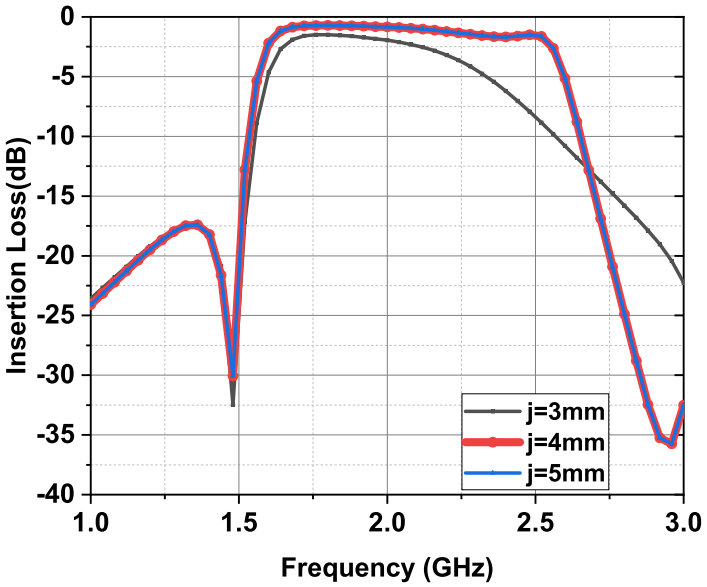


Figure 5.7: S-parameters analysis by varying the stub height (j)

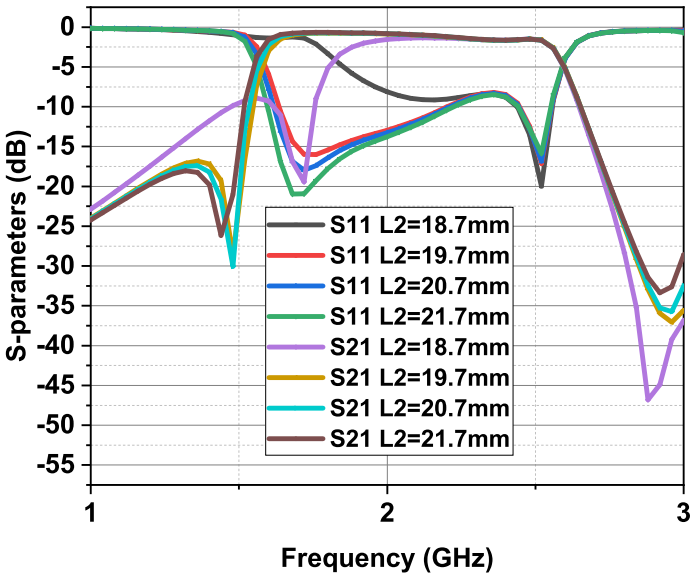


Figure 5.8: S-parameters analysis by varying the folded T-stub length (L2)

is obvious that the optimal value is 20.7mm, as L_2 less than the optimal value has less bandwidth, influencing both the lower and higher bands. And L_2 above the chosen

value produces a response that is close to the optimum value response. Similarly, L_1 is altered between 10 and 13 mm, and their S_{11} and S_{21} responses are illustrated in Figure 5.9.

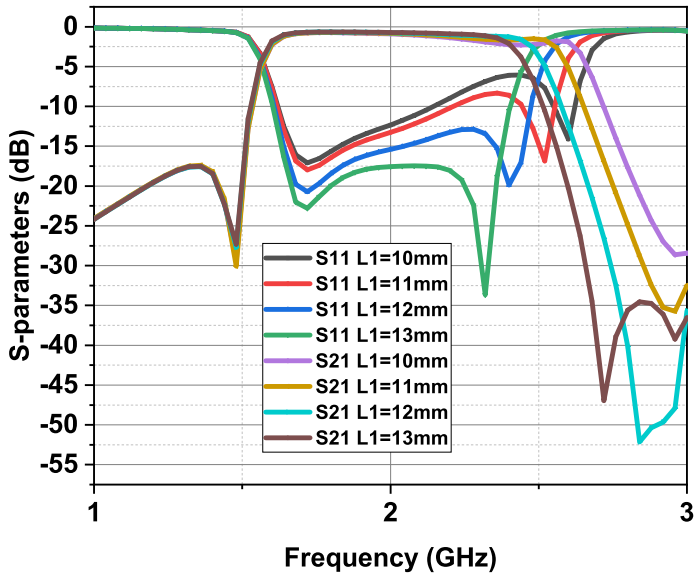


Figure 5.9: S-parameters analysis by Varying the butterfly stub length (L1)

Interestingly, 10mm produces the best S_{21} reaction and the worst S_{11} response, whereas 13mm produces the best S_{11} response and the worst S_{21} response. As a result, the optimal value of 11mm is chosen to meet our bandwidth need. The proposed FBSSIR is fabricated on a double-layer copper printed circuit board with a ϵ=4.6. The Smith chart is used to plot the resonator's input and output impedances, as seen in Figure 5.10. It is worth noting that the curve begins at the purely actual frequency of 1.64GHz and ends at another real frequency of 2GHz, which is the capacitive region's centre frequency. The curve then shifts to the inductive area between 2GHz and 2.5GHz. Figure 5.11 illustrates the measured and simulated values of the S-parameters. Due to the symmetry of the resonator, $S_{11} = S_{22}$ and $S_{21} = S_{12}$. From 1.6GHz to 2.55GHz, the return loss is substantially below -10dB, covering a nearly 1GHz wide bandwidth with a center frequency of 2GHz. The simulated and measured values agree well in terms of return loss, although there is a 3 to 4dB difference in S_{21} owing to manufacturing wear and tear. The constructed FBSSIR has a surface area of $37 \times 19mm^2$. The FBSSIR is compared to other published works in Table 5.1. This

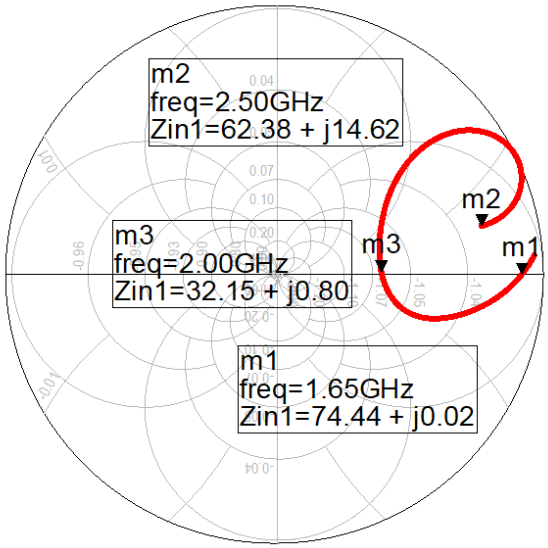


Figure 5.10: Smith chart plot of the FBSSIR

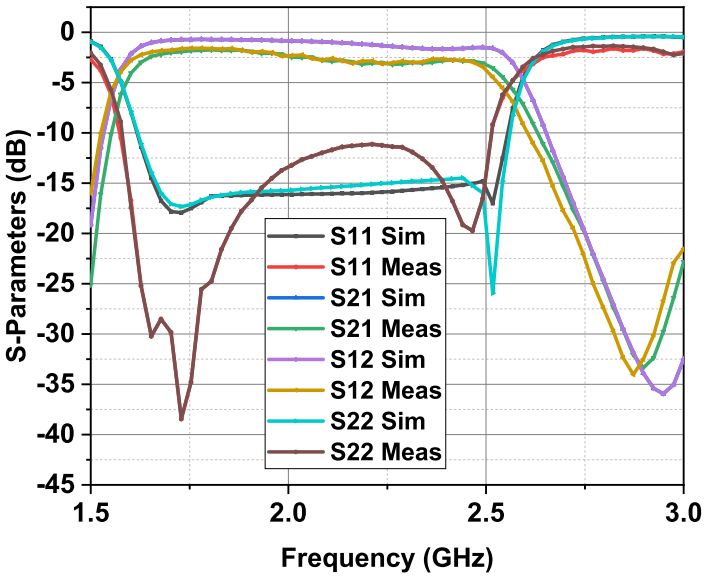


Figure 5.11: Simulated and Measured S-parameters of FBSSIR

work achieves the highest fractional bandwidth (FBW=50%). The equation 5.10 are used to compute the Fractional Bandwidth:

$$FBW\% = \frac{f_2 - f_1}{f_c} \times 100 \tag{5.10}$$

Where f_2 is the upper cutoff frequency, f_1 is the lower cutoff frequency and f_c is the center frequency. Here we have f_2 = 2.58GHz, f_1= 1.6GHz and f_c = 2GHz which results in FBW% of about to be 50 in our case.

Parameters	Central freq (GHz)	FBW%	Insertion loss(dB)	Return loss(dB)	Area (mm^2)
Chu and Chen 2008	2.13/4.87	14/11.2	0.73/0.9	32/33	23.1×23.1
Hou *et al.* 2020	2.38/4.87	6.7/8	2/1.4	–	–
Luo *et al.* 2010	1.84/2.9	8.1/6.8	1.7/1.6	> 10	–
Zhang *et al.* 2007	3.4/6.7	4.8/4	3.8/3.7	18.7/14.6	–
Hagag *et al.* 2019	2.4	16.6	2	> 10	–
This Work	2	50	2.5	> 15	37×19

Table 5.1: Comparison of state of art with resonators

5.4 Design and consideration of LNA integrated with FBSSIR

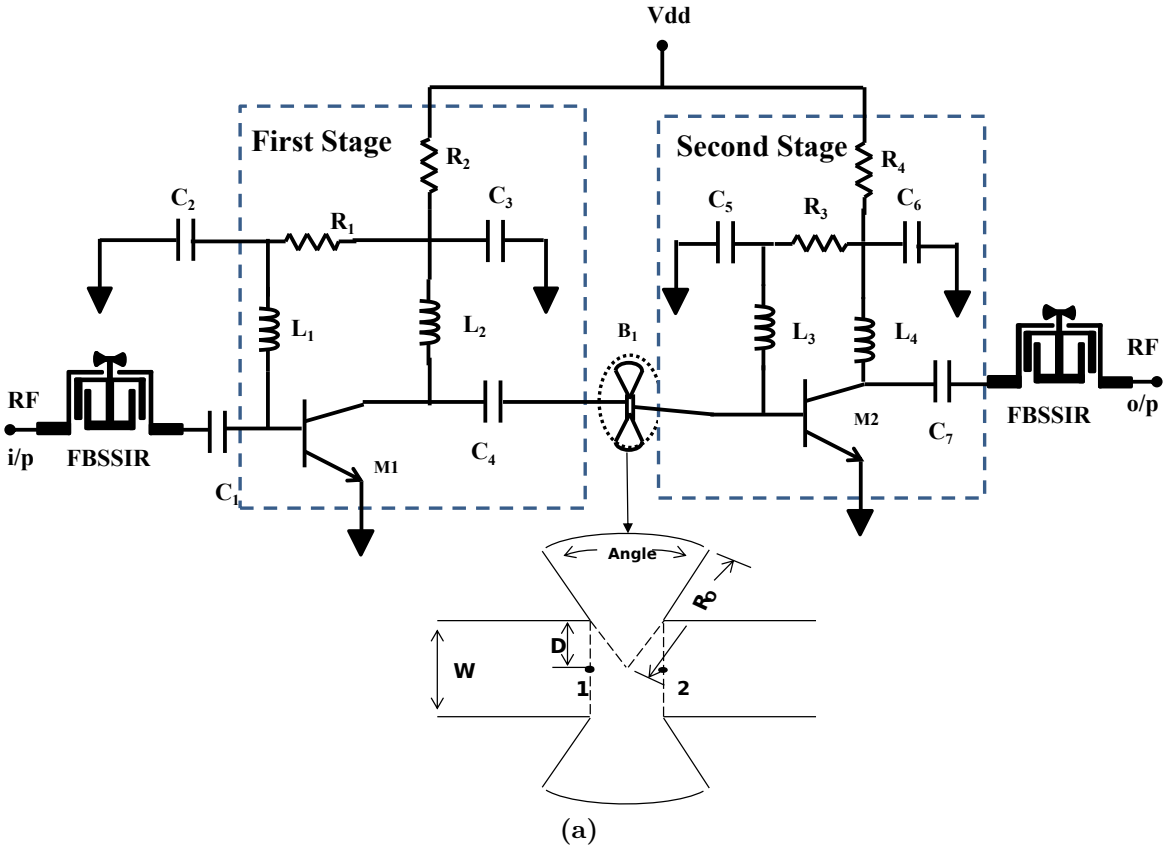
This section discusses the design and analysis of an integrated LNA based on FBSSIR. In general, the function of a resonator is to operate as a filter and to provide impedance matching, but the purpose of integrating FBSSIR into an LNA is to investigate a novel impedance matching design and to desensitise the LNA's passive components. The FBSSIR is a circuit that serves as an input and output matching network as well as a filter for this core LNA circuit. The transistor utilised in this application is the BFP420, which is a low-noise device based on a Siemens grounded emitter transistor (SIEGET). This device was chosen due to its 1.1dB minimum noise figure (NF_{min}), 21dB transconductance (G_m), and 25GHz transition frequency (f_T). The LNA is designed to operate at a normal V_{DD} of 3.3V and consumes very little power. The collector current (I_C) is limited to a maximum of 20mA. We employ a two-stage cascade LNA with an emitter grounding topology. Passive components

such as resistors R_1 to R_4 and inductors L_1 and L_3 are used to create the major bias networks for each stage. Both the input and output are capacitive coupled (i.e., C_1 and C_7) to prevent the adjacent circuitry from being affected by DC. Figure 5.12a illustrates the suggested schematic for the FBSSIR integrated LNA circuit. The initial stage is designed to have the lowest feasible noise figure because it establishes the circuit's sensitivity and noise figure. The base DC is supplied via the inductor L_1, which increases the LNA's Third order harmonics (IP_3) performance. Prior to cascading the first stage to the second, it is prudent to establish an interstage network to ensure maximum power transmission between the first and second stages. Rather than employing a conventional LC network as an interstage, this research proposes a novel interstage matching network based on stub matching. To improve stub matching, we employ butterfly stub B_1 with a width of feed line W=0.5mm, an outer radius of circular sector R_o=1.63mm, and an angle of 78^o. The $B_1 - C_4$ network is added to match the first and second stages' output and input impedances. The second stage optimises IP_3 and gain via R_4 and L_4. Additionally, it compensates for the gain loss caused by the inclusion of FBSSIR. The capacitors C_3 and C_2 in the first stage and C_5 and C_6 in the second stage give the AC grounding. The complete circuit is built and analysed

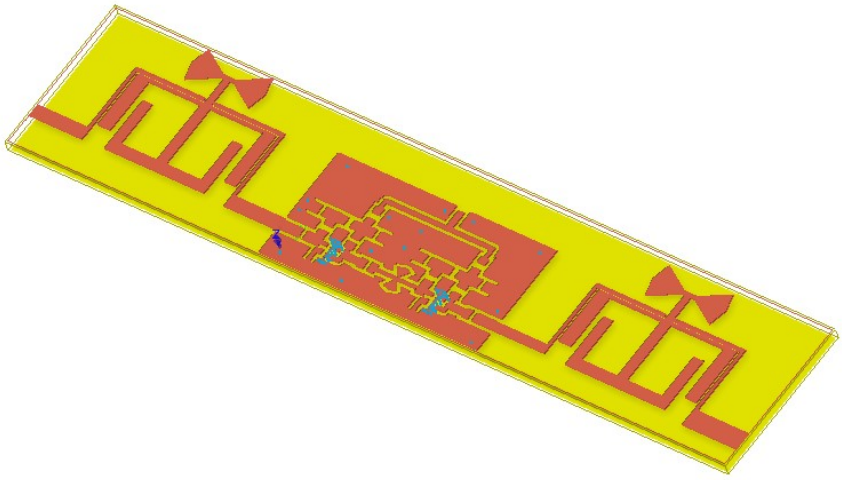
Comp	Value	Comp	Value	Comp	Value
R_1	5.6 KΩ	R_2	240 Ω	R_3	6.8 KΩ
R_4	190 Ω	L_1	33 nH	L_2	43 nH
L_3	24 nH	L_4	56 nH	C_{1-7}	100 pF

Table 5.2: Optimized component values of the proposed LNA circuit

for the sensitivity of the passive components utilised in the LNA design, and lastly, using DoE and statistical analysis, it is optimised for the optimal performance. Table 5.2 contains the optimal values for the LNA components. Figure 5.12b depicts the isometric representation of the three-dimensional layout. The layout is created with packaging components and assessed using the ADS and the Momentum microwave. v2019. The three-dimensional layout view reveals that the top and bottom layers are constructed of copper, and that vias connect the top and bottom layers throughout the circuit. The vias carry the surplus signal density to the ground bottom layer. Two types of vias are used: one with a drill diameter of 0.2mm and a pad diameter



(a)



(b)

Figure 5.12: Proposed FBSSIR based LNA (a) Schematic (b) 3D layout

of 0.3mm, and another with a drill diameter of 0.5mm and a pad diameter of 1mm. It's worth noting that the vias are more densely packed around the transistors to help

dissipate heat and offer a path for grounding. Due to the thinness of the signal path, 0.2mm diameter vias are used in and around the transistor. In other regions, vias with a diameter of 0.5mm are employed. The small-signal equivalent high-frequency

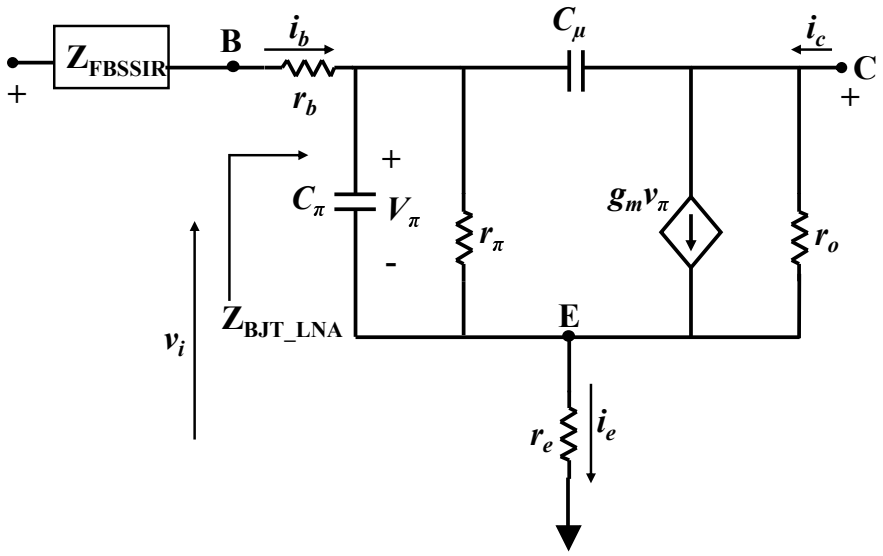


Figure 5.13: Small signal equivalent circuit of the proposed FBSSIR based LNA

model of the FBSSIR LNA is shown in Figure 5.13. The input impedance $Z_{in-Total}$ of the circuit can be calculated using equation 5.11.

$$Z_{in-Total} = Z_{FBSSIR} + Z_{BJT-LNA} \tag{5.11}$$

The input impedance of FBSSIR is similar to the SIR as the Folded butterfly stub only alters the location of zeros which is βl and is given by the equation 5.5.

Using the High-frequency small-signal model of BJT $Z_{BJT-LNA}$ is calculated. Here r_b is base spreading resistance and represents the resistance of the base-emitter junction. r_π represents the dynamic resistance for small signal analysis. r_e represents the parasitic emitter resistance. C_μ is the depletion capacitance of the collector base junction. C_π is the capacitance of the base emitter junction. $g_m v_\pi$ is the amplification factor.

$$Z_{BJT-LNA} = \frac{v_i}{i_b} \tag{5.12}$$

$$v_i = r_b.i_b + \left[\frac{1}{S.C_M} \| r_\pi\right].i_b + i_e.r_e \tag{5.13}$$

Where $C_M = C_\pi + C_\mu$ is the equivalent parasitic capacitance including the Miller

effect and $i_e = i_b \left[1 + g_m \left[\frac{1}{S.C_M} \| r_\pi\right]\right]$ By substituting this in equation 5.13

$$\frac{v_i}{i_b} = r_b + \left[\frac{1}{S.C_M} \| r_\pi\right] + \left[1 + g_m \left[\frac{1}{S.C_M} \| r_\pi\right]\right] \cdot r_e \tag{5.14}$$

Simplifying the equation 5.14

$$Z_{BJT-LNA} = r_e + r_b + \frac{r_\pi \cdot [1 + r_e g_m]}{1 + SC_M \cdot r_\pi} \tag{5.15}$$

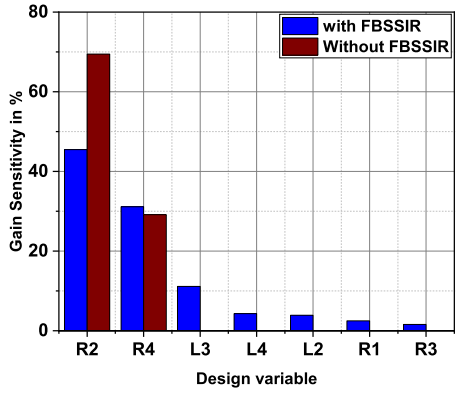
By substituting equation 5.5 and equation 5.15 in equation 5.11, we get the total input impedance of FBSSIR LNA given by the equation 5.16 below.

$$Z_{in-Total} = \left| Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l} \right| + r_e + r_b + \frac{r_\pi \cdot [1 + r_e g_m]}{1 + SC_M \cdot r_\pi} \tag{5.16}$$

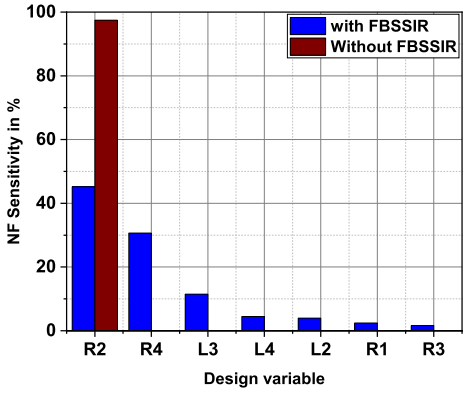
5.4.1 DoE Analysis

The Design of Experiments (DoE) is examined in order to produce a robust design and to comprehend the contribution of the design variable to accomplishing the final goal specifications as discussed in section 2.9. Only passive components are taken into account while determining the design variable. The DoE analysis is performed on the LNA core circuit with and without the FBSSIR to demonstrate the FBSSIR's potential. The results of the comparison of design variables versus contribution to the specific aim, such as NF, Gain, and return loss, are given in Figure 5.14(a), (b), and (c). It is worth noting that when there is no FBSSIR, R_2 and R_4 contribute virtually entirely to the gain. By integrating FBSSIR, the gain sensitivity is lowered by 30% from R_2. The gain sensitivity reduction caused by R_2 is shared by other passives such as L_2 to L_4, R_1, and R_3. Generally, sensitivity to a single component value is not recommended because it has a detrimental effect on the circuit's performance.

Similarly, it is noted that R_2 provides about 100% of NF in the absence of FBSSIR. However, when the FBSSIR is added, the NF's singular dependent on R_2 becomes desensitised and spreads to the other passives. The same holds true for the return loss depicted in Figure 5.14(c). The point of observation is that the FBSSIR is used for both input and output filtering; the sensitivity of the passive components is desensitised, resulting in consistent output results.



(a)



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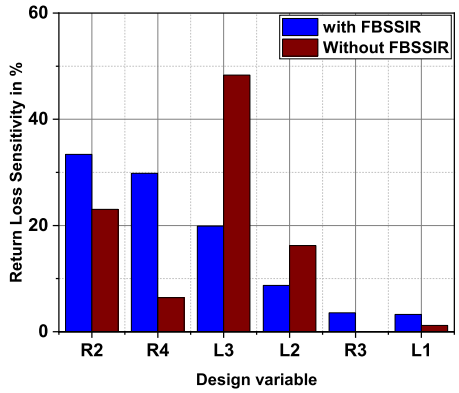


(c)

Figure 5.14: Design variable contribution to (a) Gain (b) NF (c) Return Loss

5.4.2 Statistical Analysis

Due to the fact that device parameters are vulnerable to fluctuation due to Process Voltage and Temperature (PVT), yield analysis is critical for calculating the real yield and confidence levels as discussed in section 2.8. The proposed FBSSIR integrated LNA is evaluated for error tolerance of 5% and 1% under Gaussian distribution. Gain, NF, and return loss values are depicted in Figure 5.15 (a), (b), and (c), respectively. The stable gain of 22dB, the NF of 2.8dB, and the return loss of 12dB are all achieved with a tolerance of 1%. It yields a yield estimate of 100% after 1000 iterations. However, for the 5% tolerance yield estimation, 32% of iterations failed to yield 68%. The parameters are limited to a minimum gain of 20dB, a maximum NF of 3.5dB, and a minimum return loss of 10dB. However, PVT changes are often less than 1%,

indicating that the planned FBSSIR-LNA is stable and robust.

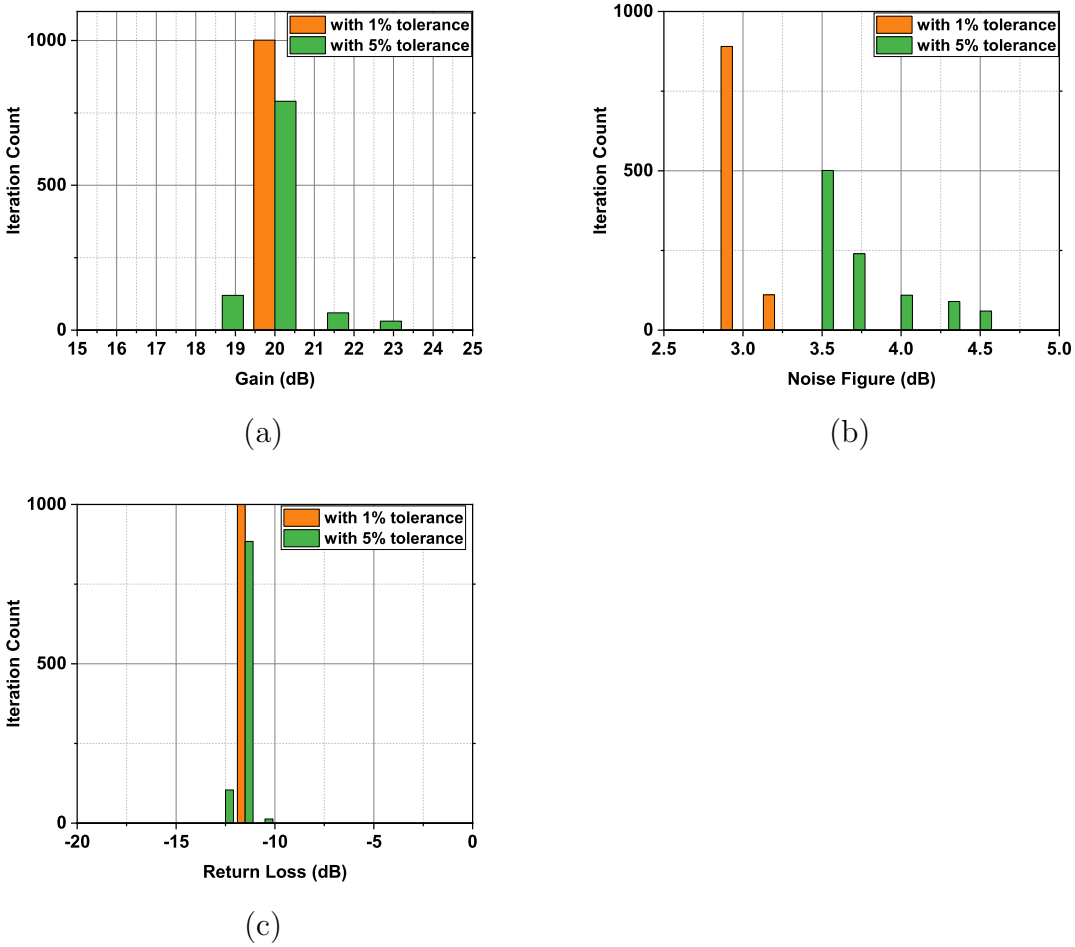
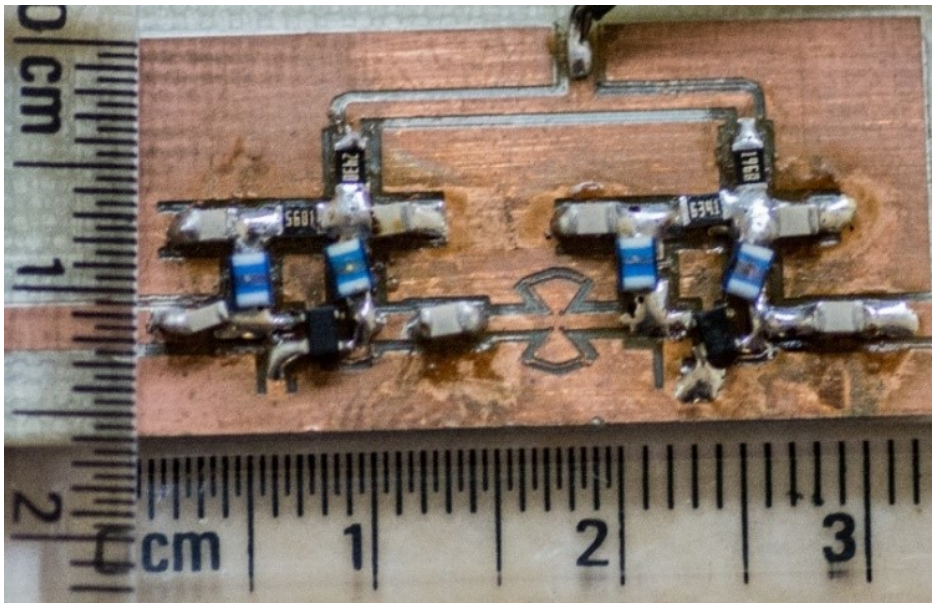


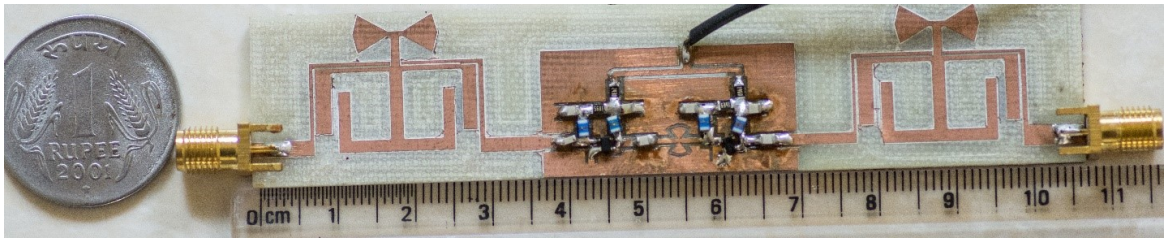
Figure 5.15: Yield estimation of FBSSIR-LNA (a) Gain (b) NF (c) Return Loss

5.5 Results and Discussion

This section discusses the performance of the FBSSIR integrated LNA by presenting simulation and measurement findings. The circuit is compared before and after the addition of the FBSSIR to demonstrate the potential and importance of the FBSSIR as a filtering step in the input and output to evaluate the LNA's performance. The LNA is implemented and constructed utilising PCB packaging techniques on a FR4 substrate. Figure 5.16a and figure 5.16b illustrate the top view of the manufactured LNA and FBSSIR integrated LNA, respectively. S-parameters for the FBSSIR integrated LNA



(a)



(b)

Figure 5.16: Fabricated photograph view with (a) LNA prototype (b) FBSSIR integrated LNA prototype

are determined using a PNA E8363 network analyzer connected to Agilent technologies RF probes up to 40GHz. Prior to performing measurements, the PNA and probes must be calibrated. For probe systems, the approach and method of short-open-load-through calibration have been used. Figure 5.17 shows the simulated and measured NF plots with and without FBSSIR. The NF of the LNA decreases by 7.5 dB in the FBSSIR passband, which ranges from 10.2dB to 2.7dB at 1.8GHz. Outside of the 1.6GHz to 2.5GHz frequency range, even the NF of the circuit with FBSSIR increases by 10dB. Due to the correct impedance matching of the components, the FBSSIR integrated LNA significantly reduces the NF from 10dB to 2.5dB. The antenna signal is routed through the FBSSIR and then to the LNA. By filtering, the FBSSIR eliminates noise and provides a pure signal to the first stage of the LNA. A modest decrease in

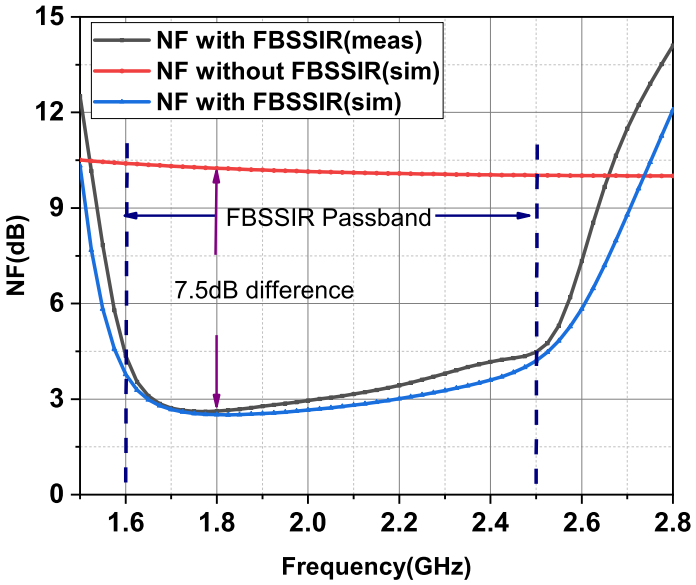


Figure 5.17: Noise Figure of the designed FBSSIR-LNA

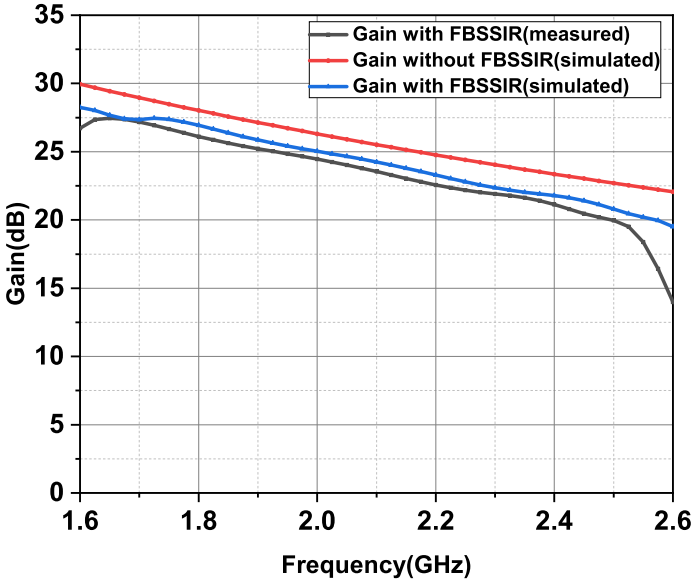


Figure 5.18: Gain of the designed FBSSIR-LNA

signal strength is detected, lowering the gain of the circuit by 4dB. However, the second stage LNA circuit may easily compensate for this increase. The output side

FBSSIR filters out noise generated by the device's passives and actives.

Figure 5.18 illustrates the gain comparison with and without FBSSIR. It is worth noting that, while the gain decreases slightly when FBSSIR is used, the slope of the gain decay from 1.8GHz to 2.5GHz is slightly reduced.

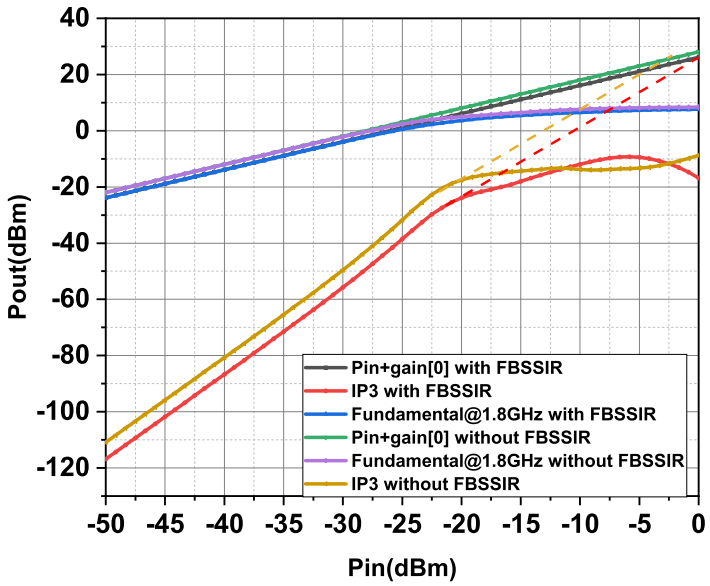
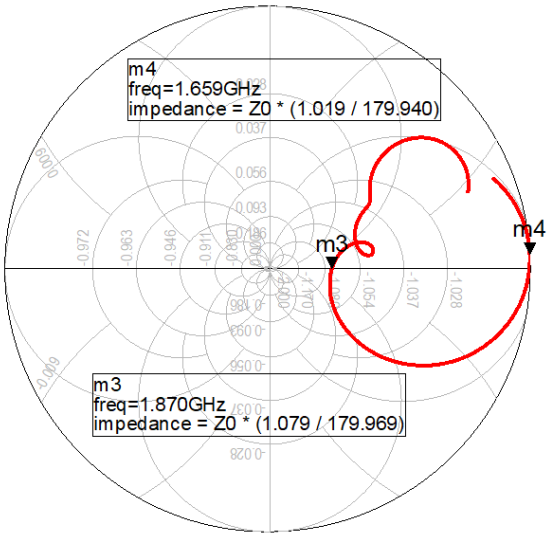


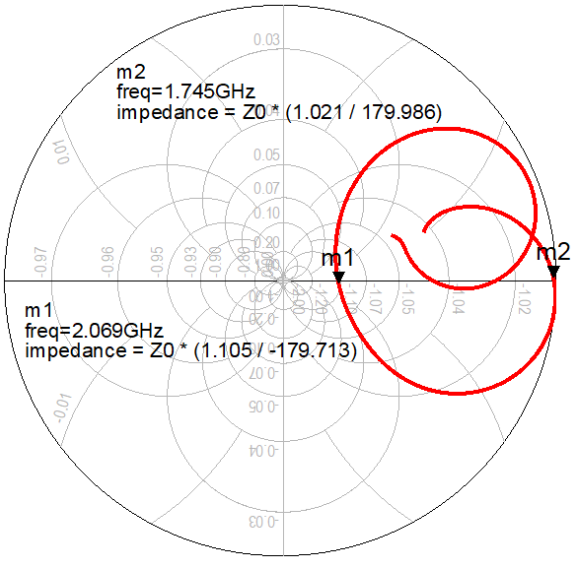
Figure 5.19: Simulated Comparison of Pin vs. IP3 and Pout (fundamental) of LNA with and without FBSSIR

Figure 5.19 plots the simulated input and output power (fundamental at 1.8 GHz) and input and output power (third-order harmonics) for the designed LNA with and without FBSSIR to determine the IIP_3 and IP_{1dB}. It is worth noting that for the circuit with FBSSIR, the Input 1 dB (IP_{1dB}) compression point is obtained at -23dBm. At 0dBm, the third-order input intercept point (IIP_3) is reached. Additionally, the plot demonstrates that the developed LNA achieves good OIP_3 and OP_{1dB} values of +25dBm and +2.3dBm, respectively. Third-order harmonics are decreased slightly when FBSSIR is used, resulting in a +5dBm improvement of IIP_3 from -5dBm when FBSSIR is not used to 0dBm when FBSSIR is used. This LNA's strong linearity results in an outstanding spur-free dynamic range, which is ideal for wireless receiver construction.

The input and output impedances of the FBSSIR integrated LNA are depicted in Figure 5.20a and Figure 5.20b , respectively, as a smith chart. Around the resonant



(a)



(b)

Figure 5.20: Simulated smith chart plot of FBSSIR integrated LNA (a) Input impedance (b) Output impedance

frequency of 2GHz, both the input and output impedances align with the real axis. They exhibit identical half capacitive and half inductance curves as a result of the FBSSIR's perfect impedance matching at the input and output. The measured stability factor K and the Δ described in equation 3.5 and equation 3.6 is plotted in the

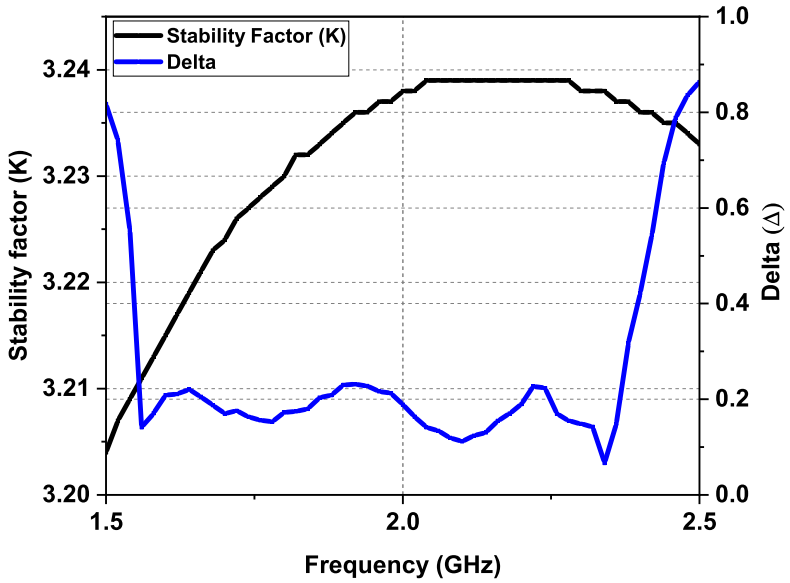


Figure 5.21: Measured Stability factor K and Δ of FBSSIR-LNA

figure 5.21. It is worth noting that the developed LNA is perfectly stable over the necessary frequency range of 1.6GHz to 2.5GHz.

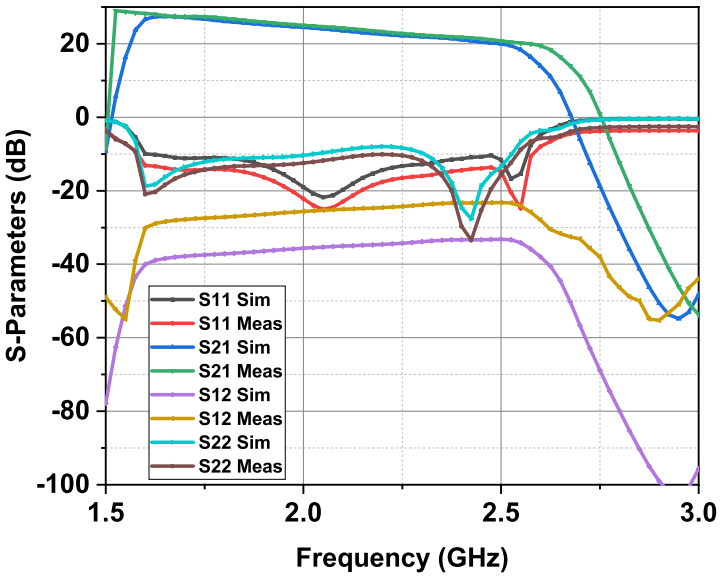


Figure 5.22: Simulated and measured S-parameters of FBSSIR-LNA

Figure 5.22 depicts the measured and simulated entire S-parameters of LNA. The gain is greater than 22dB over the whole frequency range of 1.6GHz to 2.5GHz. The disparity between measured and simulated values is primarily due to fabrication wear and tear, namely soldering. In the 1.6GHz to 2.5GHz frequency band, the return loss (S_{11}) is sufficiently low (far below 12dB) to avoid reflection. Other S-parameters, such as S_{12} and S_{22}, also gives satisfactory performance. The output of the LNA with and without FBSSIR is shown in Table 5.3. The state of art comparison with reported works is shown in Table 5.4.

Parameters	Without FBSSIR LNA	With FBSSIR LNA
Freq(GHz)	1.6-2.5	1.6-2.5
Gain(dB)	30	16
S_{11}(dB)	<-2	<-12
NF(dB)	10	2.7
IP_{1dB}(dBm)	-24	-23
IIP_3(dBm)	-5	0
OIP_3(dBm)	+25	+25
OP_{1dB}(dBm)	+2.9	+2.3
Area(cm^2)	3.3×1.6	10.7×2

Table 5.3: Results summary of FBSSIR-LNA

5.6 Summary

The FBSSIR integrated LNA in PCB technology with a two-stage cascaded topology is provided in this chapter. The statistical and DOE analyses are presented to evaluate the design's yield and resilience. To begin, the suggested FBSSIR is constructed and validated using full-wave electromagnetic simulations. It functioned as an excellent noise filter and desensitised the LNA passive settings. This FBSSIR integrated LNA

achieves gain in excess of 22dB throughout the 1.6-2.5GHz frequency range. It achieves a low NF of 2.7dB at 1.8GHz and fluctuates between 3-4.5dB between 1.6GHz and 2.5GHz. The FBSSIR integrated LNA is very linear, with an IP_{1dB} of -23dBm, an IIP_3 of 0dBm, an OP_{1dB} of +2.3dBm, and an OIP_3 of +25dBm, and a power dissipation of 26.5mW.

Table 5.4: Comparison of the FBSSIR-LNA performance with state of art.

Parameters	Frequency (GHz)	Gain (dB)	NF (dB)	IIP_3^*(dBm)	Area (cm^2)	P_{DC}(mW)	FoM
Yang *et al.* (2005)	2-2.5	12	1.7	–	2.4×1.8	30	0.28
Hagag *et al.* (2019)	2.8-4	14	4.6	11	8×3	90	0.05
Djoumessi and Wu (2009)	2.2-2.5	22	1.5	-10	3×3	7.5	1.7
Kumar and Pathak (2014)	2.3-2.5	12	0.7	–	6×5.5	42	0.1
Iyer and Pathak (2014)	2.3-2.5	7	4.4	–	8×6	35.1	0.01
Kumar and Pathak (2015)	2.4	11	4	–	12×3.4	56	0.01
Li *et al.* (2020)	0.3-6	16.5	3.1	-4	0.06×0.04	48	0.83
Chaghaei *et al.* (2020)	0.1-2	21	4.9	-9.4	0.02×0.02	1.8	5.8
This Work	1.6-2.5	27	2.7	0	10.7×2	26.5	0.4

– Not calculated * Simulated Results

Chapter 6

SWITCHLESS RECONFIGURABLE LNA BASED ON SSCL FOR K/KA BAND

6.1 Introduction

Applications in the K-Ka band (18-40GHz), including as 5th generation (5G) networking, radar, and astronomy detection, primarily rely on wideband mm-wave front-ends. Low noise amplifiers (LNAs), as one of the most crucial active components, are the primary block of mm-wave receiver front-ends. We intend to obtain a low noise figure, a high gain with flatness, good linearity, and low power consumption for LNAs in order to enhance the dynamic range and sensitivity of the receiver system, which complicates LNA design. This work aims on achieving the best trade-offs among the LNA performance parameters by comparing the reported works in the entire bandwidth of 22GHz.

6.2 Prior Works

Extensive research on wideband LNAs has been conducted in recent decades. A distributed amplifier (DA) is the most promising topology for realising an ultra-wideband

LNA (Liang *et al.* 2021) and (Fang and Buckwalter 2019). However, DA is not ideal in many cases because to its poor bandwidth at unity gain, high NF, and greater area. Other strategies for increasing bandwidth have been reported in (Hu *et al.* 2018), (Hu *et al.* 2019), (Nikandish and Medi 2015) and (Park *et al.* 2021) including shunt-resistive feedback, dual inductive peaking, enhancing dynamic load, a frequency-dependent feedback loop (FDFL), and a split common gate transistor (SCGT). These proposed strategies for increasing bandwidth decrease other RF factors such as noise performance. The primary disadvantage of wideband LNAs is that they amplify the unwanted signal while reducing the receiver's sensitivity. Another method is to use reconfigurable LNAs to construct wideband receivers with high interference rejection, and numerous multiband LNAs are described in the literature such as (Yu and Neihart 2013). A reconfigurable multimode LNA is proposed in (Shaheen *et al.* 2021), but it has a lower gain of around 12dB and a high NF of up to 5dB due to the inclusion of a switched multitap transformer in the input matching network and a tunable load based on electrical and magnetic tuning operating at three single bands (24/28/39 GHz).

(Nawaz *et al.* 2020) describes a 28/60 GHz reconfigurable LNA based on RF switches for mm-wave transceivers. Additionally, this LNA has a meager gain of 14dB and an NF of 4.6dB. They still have a 1dB ON-loss and a 0.7dB OFF-loss despite employing fine sophisticated RF switches. Although (Lee and Nguyen 2021) presents a 44/60 GHz reconfigurable LNA based on Q-enhanced metamaterial transmission lines, they have a high NF of 5.6dB and IIP_3 of -14dBm. The article's distinctive feature is that it achieves a 30dB rejection between two bands. Although it achieves a respectable NF of 2.8dB and low power consumption, a dual-band switchable LNA based on LC tunable tank and tunable stub based on Hetero-junction Bipolar Transistor (HBT) switch is published in (Nawaz *et al.* 2019). However, it suffers from low gain. (Liang *et al.* 2020) describes a tri-band reconfigurable LNA working at 24/33/50 GHz that utilises a triple coupling transformer (TCT) and extra gain boosting to reach gain of up to 32dB with a 6dB minimum noise figure. This LNA has a high NF value and low linearity. All of these published works operate at mm-wave frequencies and have their own design trade-offs.

(Wang and Zhang 2020) describes a two-stage LNA operating between 22GHz and 47GHz with a peak gain of 22.2dB and a noise figure of 4.3dB employing linked L-type interstage matching inductors. This LNA offers one of the best design trade-

offs available, with the drawback of a low IIP_3. (Lee and Nguyen 2018) describes a dual-band concurrent single-ended input to differential output LNA working at 18-25 GHz and 33-46 GHz with a gain of 16dB and a noise figure of 4.3dB. While this LNA has a low gain and a high NF, it also has the unique ability to manage stop band rejection and passband gain balancing concurrently. (Yu *et al.* 2021) describes a 21-41 GHz, 28.5dB gain, and 3.2dB NF LNA using the triple coupled transformer approach. Additionally, this LNA offers one of the best design trade-offs; nonetheless, no other LNA has achieved ultra-low NF while maintaining good linearity. (Li *et al.* 2018) describes an LNA with a gain of 12.8dB and an NF of 1.4dB working between 14GHz and 31GHz. Among the works presented, this is the only LNA with an NF less than 1.5dB yet a gain less than 13dB. (El-Aassar and Rebeiz 2020) presents a 19.5-28.5 GHz variable low power LNA with a gain of 7.8-23.2 dB and a 0.4-1.6 V supply; nevertheless, they have not achieved ultra-low NF. The literature reviewed above is suitable for wideband mm-wave receiver systems, but they all have limitations in terms of LNA design trade-offs in terms of gain, NF, linearity, power consumption, area, and sensitivity. All of the reported works except (Lee and Nguyen 2021) use one or more components such as tunable inductors, varactors, transformers, and RF switches, which require additional power supplies and are difficult to implement at high frequencies due to their associated loss and tradeoffs.

Considering the drawbacks of the bandwidth enhancement and other reconfigurable techniques for the ultra-wideband LNA, this research proposes a new switchless reconfigurable LNA based on the inter-stage and output-stage Suspended Substrate Coupled Line (SSCL) for the full K-Ka band (18-40) GHz. An 8-20 GHz switchless dual-band reconfigurable LNA and a 6-18 GHz switchless dual-band reconfigurable power amplifier (PA) are reported in (Xie *et al.* 2020) and (Choi *et al.* 2018) using a coupled line-based diplexer which is similar to the SSCL used in this research.

6.3 SSCL design and consideration

6.3.1 Coupled line Analysis

A coupled line (CL) is formed when a two-transmission line is placed in such proximity that energy from one line transfer to the other. This proximity will alter the electromagnetic fields (so the voltages and currents alter) of the propagating wave, thereby

altering the transmission line's characteristic impedance. When the two-transmission line is placed as coupled lines it forms a four-port network. Figure 6.1 illustrates the

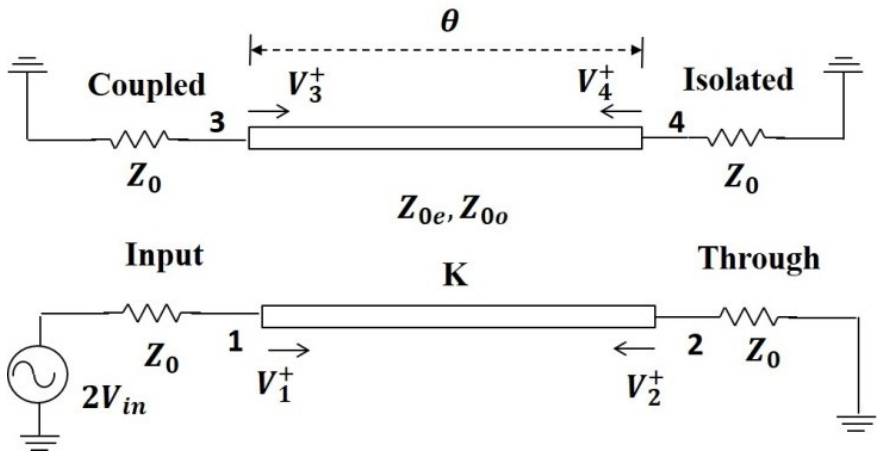


Figure 6.1: Conventional coupled line structure (A)

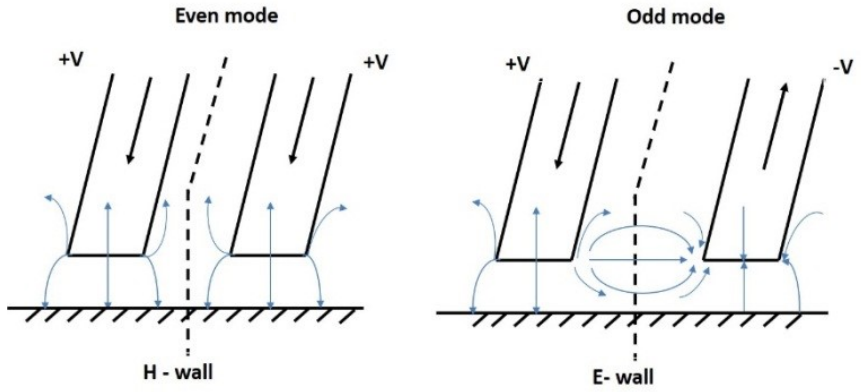


Figure 6.2: Even-Odd mode Excitation in CL

traditional microstrip coupled line. Coupled line working principles are the same even if we change the type of the transmission line used like suspended substrate line (SSL), strip-line, shielded microstrip line, Fin-line, and so on. So, the traditional microstrip coupled line analysis is discussed to better understand the proposed SSCL's dual-band activity mechanism. Port 1 is the input port, the output which comes directly from port 1 is through port or port 2. The output port where the coupled signal comes out is known as coupled port or port 3. The final port is known as the isolated port or port 4 where ideally no signal comes out from input. In a coupled line structure,

the load impedance Z_{load} is considered to be the same as the coupled line's characteristic impedance Z_0. In this case, the output voltage of the coupled port (port 3) and through port (port 2) can be determined as a function of the input voltage V_{in} denoted in equations 6.1 and 6.2 (Pozar 2011).

$$V_{\text{through}} = V_{\text{in}} \cdot \frac{\sqrt{1-K^2}}{\sqrt{1-K^2}\cos\theta + j\sin\theta} = T \cdot V_{\text{in}} \tag{6.1}$$

$$V_{\text{coupled}} = V_{\text{in}} \cdot \frac{jK\sin\theta}{\sqrt{1-K^2}\cos\theta + j\sin\theta} = C_F \cdot V_{\text{in}} \tag{6.2}$$

Where $T = \frac{\sqrt{1-K^2}}{\sqrt{1-K^2}\cos\theta + j\sin\theta}$ and $C_F = \frac{jK\sin\theta}{\sqrt{1-K^2}\cos\theta + j\sin\theta}$

Voltage coupling factor C_F of port 3 as a function of the coupling coefficient, K and electrical length θ can be given by:

$$20\log|C_F| = 20\log\left|\frac{jK\sin\theta}{\sqrt{1-K^2}\cos\theta + j\sin\theta}\right| \tag{6.3}$$

Here K is the coupled line's coupling coefficient, and θ is the coupled line's electrical length.

There are two modes for the coupled line depending on the current flow mechanism in an electromagnetic context. In the first mode, current flows downward on the conductor with a contra-flow current back up the other conductor due to displacement current coupling between the two conductors. This is referred to as the odd mode current, and it has an odd mode characteristic impedance Z_{0o} associated with it. In the other mode, the current flowing between each center conductor through displacement current has the same polarity and is connected to a common ground. As a result, this current is referred to as even mode current, and it is accompanied by an even mode characteristic impedance Z_{0e} (Pozar 2011) . The pictorial representation of the odd mode and even mode is depicted in Figure 6.2. The coupling coefficient K as a function of odd mode impedance Z_{0o} and even mode impedance Z_{0e} can be given by:

$$K = \frac{(Z_{0e} - Z_{0o})}{(Z_{0e} + Z_{0o})} \tag{6.4}$$

The relation between the characteristic impedance Z_0 and odd and even mode impedance is given as:

$$Z_0 = \sqrt{Z_{0e} Z_{0o}} \tag{6.5}$$

From equations 6.1 and 6.2, we can see that at very low frequencies or terse line length ($\theta \ll \pi/2$), nearly all input power is transmitted to port 2, with none being coupled to port 3. The maximum coupled power transmitted to port 3 is achieved at $\theta = \pi/2$ or $l = \lambda/4$, as shown in Figure 6.3.

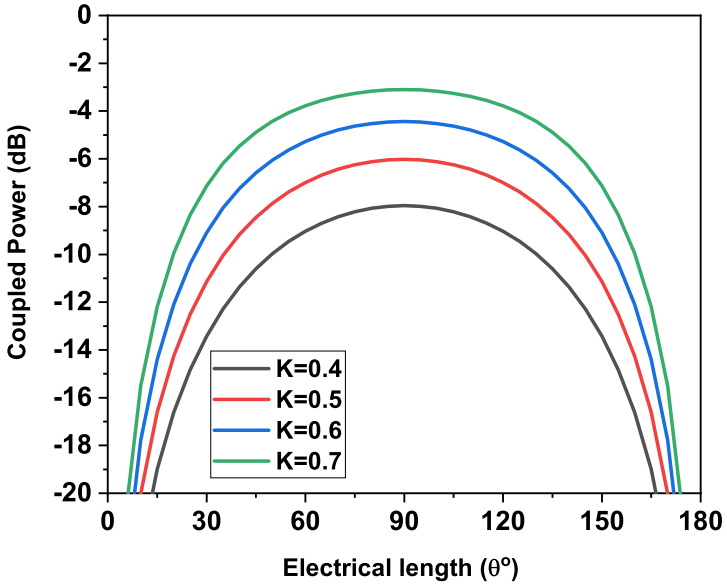


Figure 6.3: Coupled power of conventional coupled line A

From Figure 6.3, the maximum coupled power is approximately -3dB with a long-coupled line ($\theta = \pi/2$) for K = 0.7. For this reason, the traditional coupled line structure in Figure 6.1 may not be applicable in the proposed LNA. The scattering matrix [S] of a four-port coupled-line coupler can be written as:

$$[S]_{4\times4} = \begin{bmatrix} 0 & -j\sqrt{1-K^2} & K & 0 \\ -j\sqrt{1-K^2} & 0 & 0 & K \\ K & 0 & 0 & -j\sqrt{1-K^2} \\ 0 & K & -j\sqrt{1-K^2} & 0 \end{bmatrix} \tag{6.6}$$

The modified structure of the coupled line is shown in Figure 6.4. The isolated port (port 4) is grounded initially (without C_8). The shunt capacitance C_7 at port

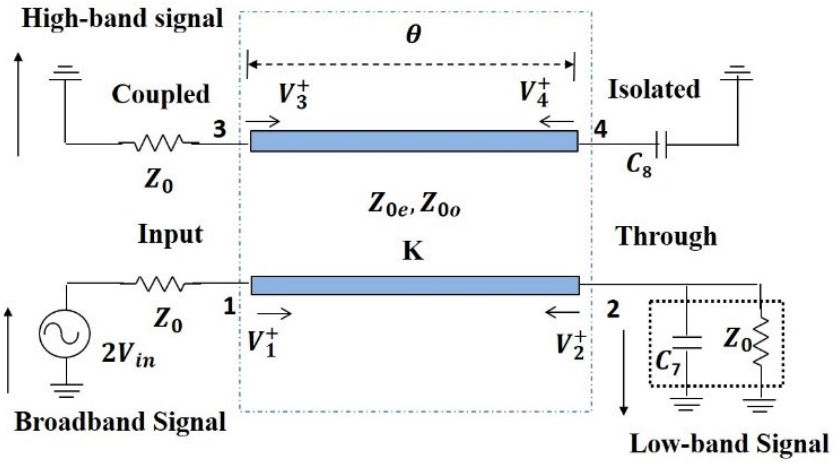


Figure 6.4: Proposed Coupled line structure B

2 (through port) behaves as a short circuit for ideal high-band frequencies operation. The input impedance matching network of the low-band LNA absorbs this C_7 during the low-band frequency operation. The through port output signal is mirrored with an 180^0 phase shift and re-enters the coupled line. The signal is then coupled to the isolated port, mirrored with an 180^0 phase shift, and finally emerges from the coupled port (port 3) with the initial coupled signal. The output voltage of the isolated port (port 4) and coupled port (port 3) as a function of the input voltage V_{in} can be expressed as:

$$V_4^- = C_F \cdot V_2^+ = C_F \cdot \Gamma \cdot V_2^- = C_F \cdot \Gamma \cdot T \cdot V_{\text{in}} \tag{6.7}$$

$$V_3^- = C_F \cdot V_{\text{in}} + T \cdot V_4^+ = C_F \cdot V_{\text{in}} + T \cdot \Gamma \cdot V_4^- \tag{6.8}$$

On simplifying the above equation

$$V_3^- = C_F \cdot V_{\text{in}} + C_F \cdot T^2 \cdot V_{\text{in}} \tag{6.9}$$

Coupled power of port 3 as a function of the coupling coefficient K and electrical length θ can be expressed as:

$$20 \log \left| \frac{V_3^-}{V_{in}} \right| = 20 \log \left| C_F + C_F \cdot T^2 \right| \tag{6.10}$$

It is noted that from equation 6.9, the coupled port output signal consists of two

parts: $C_F.V_{in}$ and $C_F.T^2.V_{in}$. The phase difference between the two parts is identical to the coupled line's double electrical length, as shown in Figure 6.5. When the

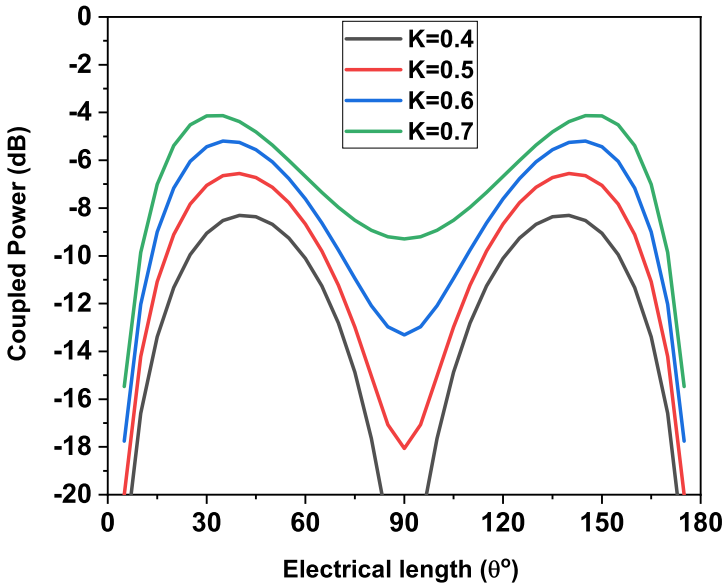


Figure 6.5: Coupled power of proposed coupled line B without capacitor C_8

coupled line's electrical length is $\lambda/4$, the phase difference between the two parts of the coupled power is 180^0; then, the minimum coupled power is obtained. Figure 6.5 and Figure 6.6 illustrate the coupled power in port 3 of the coupled line shown in Figure 6.4 according to different coupling coefficient K and electrical length (θ) of the coupled line. When the electrical length is $30^0 \sim 45^0$ or $135^0 \sim 150^0$, maximum coupled power can be obtained for a definite K. Here, a maximum coupled power of -4dB can only be achieved for K= 0.7, which is not sufficient to be used in the interstage of the LNA. The phase difference between the two parts of the coupled power $C_F.V_{in}$ and $C_F.T^2.V_{in}$ is the cause of inadequate coupled power, and it is shown in Figure 6.7.

To compensate for the phase difference between two parts of the coupled power, we added a shunt capacitance C_8 to the isolated port. The phase response after adding C_8 is shown in Figure 6.8. From Figure 6.7 and Figure 6.8, without the capacitor C_8, there is 180^0 phase difference when the electrical length is 90^0 or $\lambda/4$, causing minimum coupling, but after adding shunt capacitance C_8 to the isolated port, the phase difference becomes 0^0 at $\lambda/4$ electrical length which maximizes the coupling.

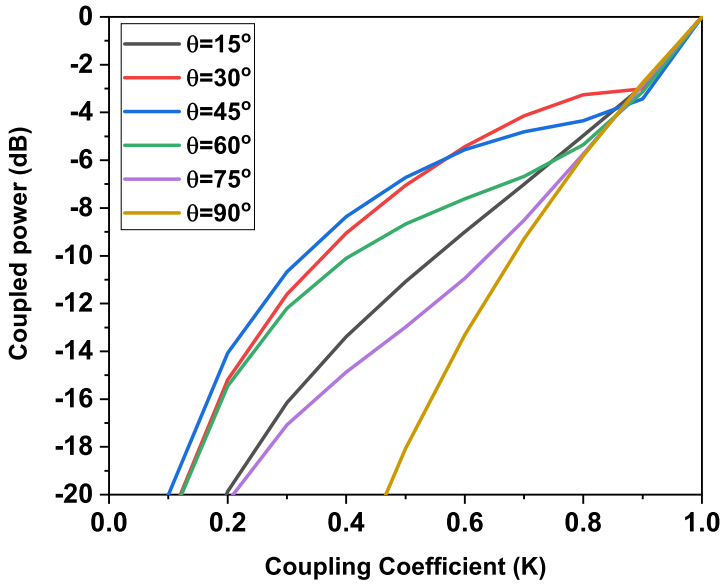


Figure 6.6: Coupled power of proposed coupled line B according to different coupling coefficients without capacitor C_8

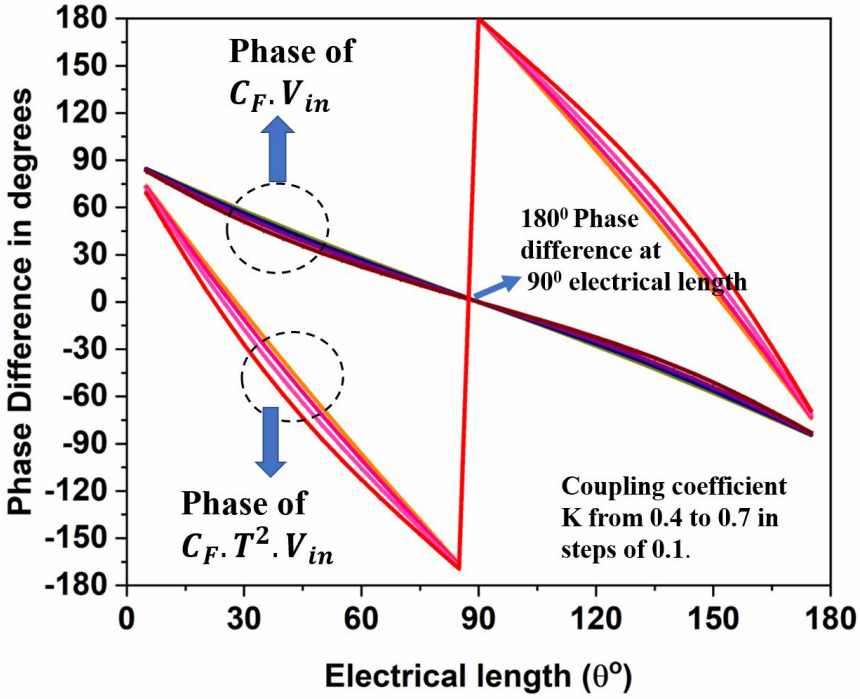


Figure 6.7: Phase difference of proposed coupled line B without capacitor C_8

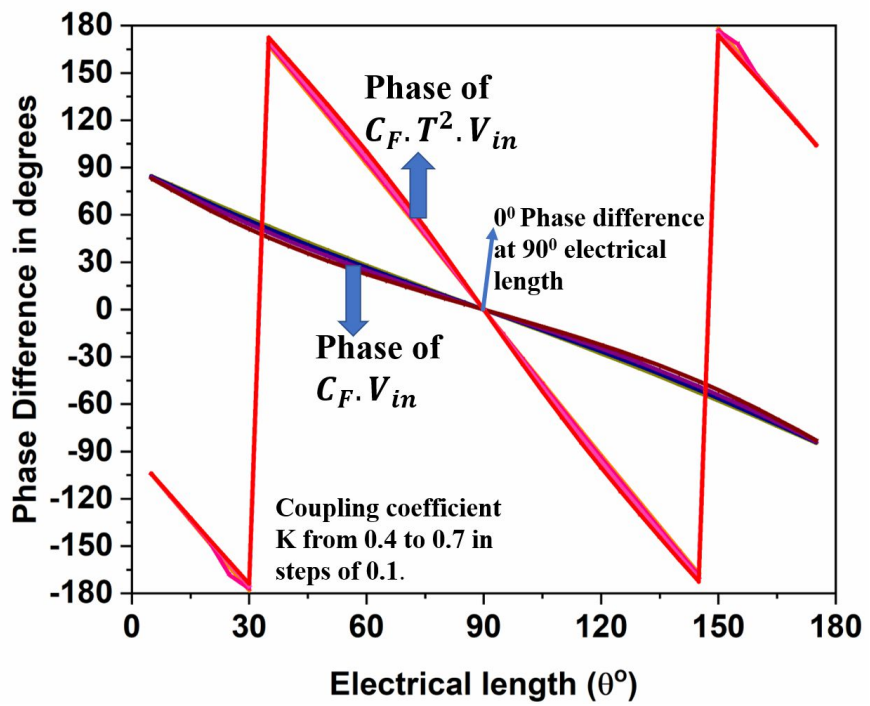


Figure 6.8: Phase difference of proposed coupled line B with capacitor C_8

6.3.2 Comparison of basic coupled line structure with proposed SSCL

The proposed coupled line is first tested with the traditional microstrip line (MCL) and Shielded microstrip line (SMCL) shown in Figure 6.9(a) as an inter-stage. The schematic of the proposed structure shown in Figure 6.10(a) is simulated, and the simulation results in Figure 6.11 show that the coupling power suffers a loss of around -4.8dB because of the described reason in the above subsection 6.3.1. The losses occur due to dispersion, fringing effects, and other EM losses due to mm-waves. In Chapter 3 section 3.3.1 a wafer-level integrated suspended substrate line (SSL) platform is developed to avoid these losses in our previous work. Based on the SSL developed the coupled lines is developed named as Suspended Substrate Coupled Lines (SSCL). The 1-D and 3-D schematics of the proposed SSCL are shown in Figure 6.9(b) and Figure 6.9(c). It consists of two substrates made of Silicon Nitride (SiN) with a thickness of 25μm separated by an air gap of 50μm. Each substrate has top and bottom metal layers with a thickness of 2.5μm marked as M1, M2, M3, and M4. The metal layers M1 and M4 act as the ground, while the metal layer M3 act as a signal trace.

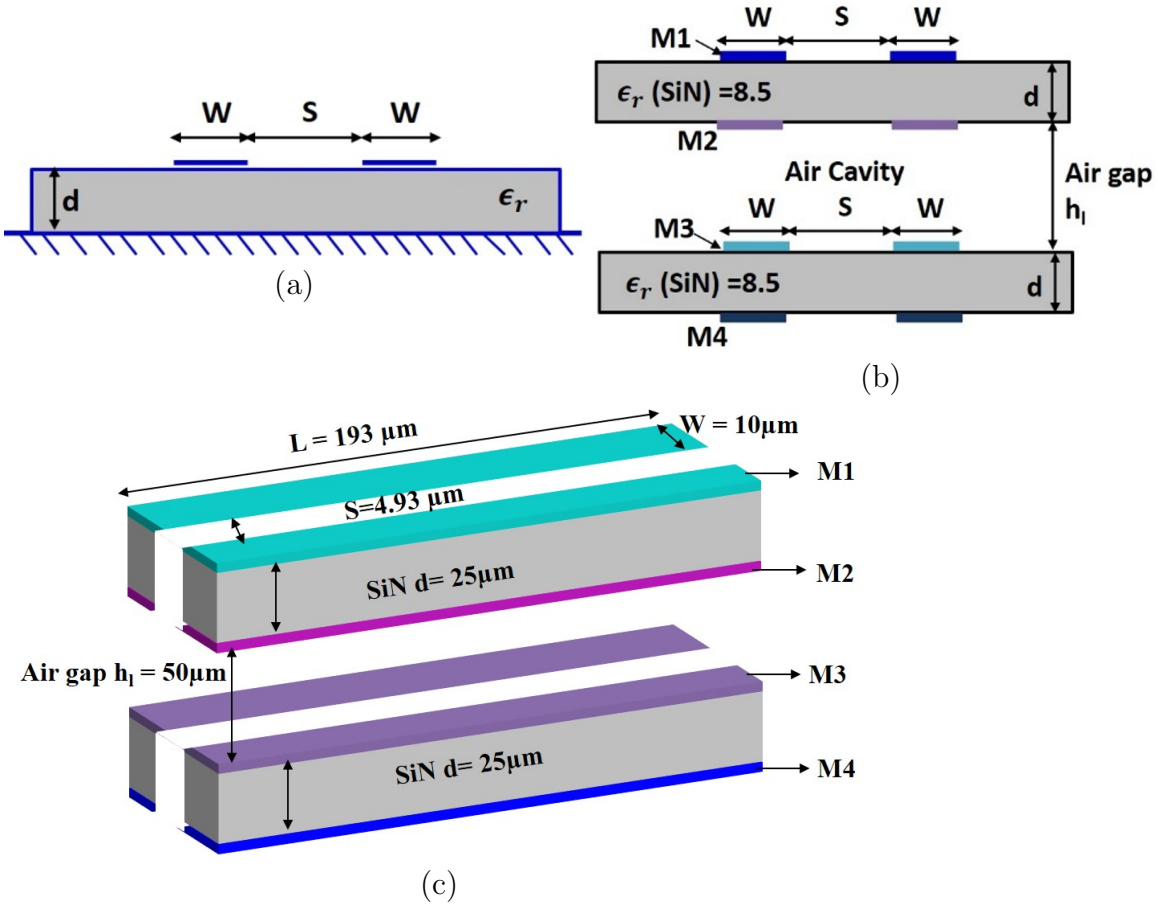


Figure 6.9: (a) 1-D Microstrip Coupled Line (MCL) (b) 1-D Suspended Substrate Coupled Line (SSCL) (c) 3-D geometry of SSCL

The metal layer M2 act as a signal reflection path. When the signal passes through the metal layer M3 at such high mm-wave bands, an EM field is developed, which causes a fringing effect around the M3 layer. Additional losses such as dispersion loss, dielectric loss also occur. But here, as the signal trace path has a reflection path (M2) and ground layers (M1, M4), the developed EM field is confined to the air cavity as discussed in chapter 3 section 3.3.1 . This allows us to have the minimum loss, and we receive high coupled power at the output.

The schematic of the proposed SSCL as interstage and output-stage are shown in Figure 6.10(a) and (b), respectively. The length (L) of the coupled line is 193μm with $30^0 \sim 40^0$ electrical lengths over 18-40 GHz. Width (W) and separation distance (S) is 10μm and 4.93μm, respectively. The coupling coefficient (K) is 0.72 approximately. Shunt capacitance of $C_7 = 0.01$pF is added to the through-port, and Shunt capacitance

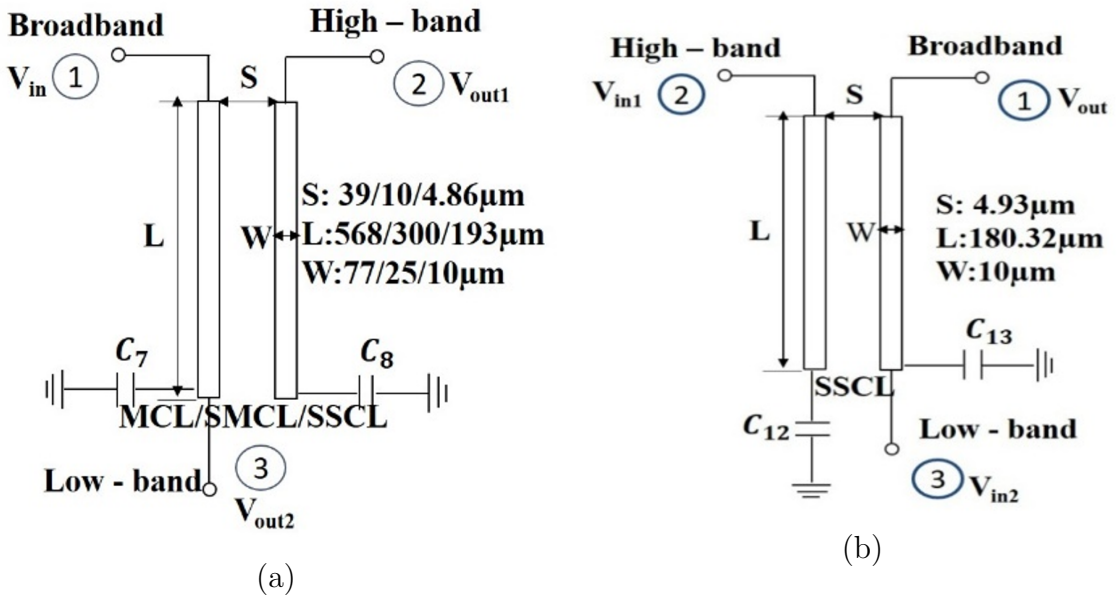


Figure 6.10: Schematic of (a) Inter-stage MCL/SMCL/SSCL (b) Output-stage SSCL

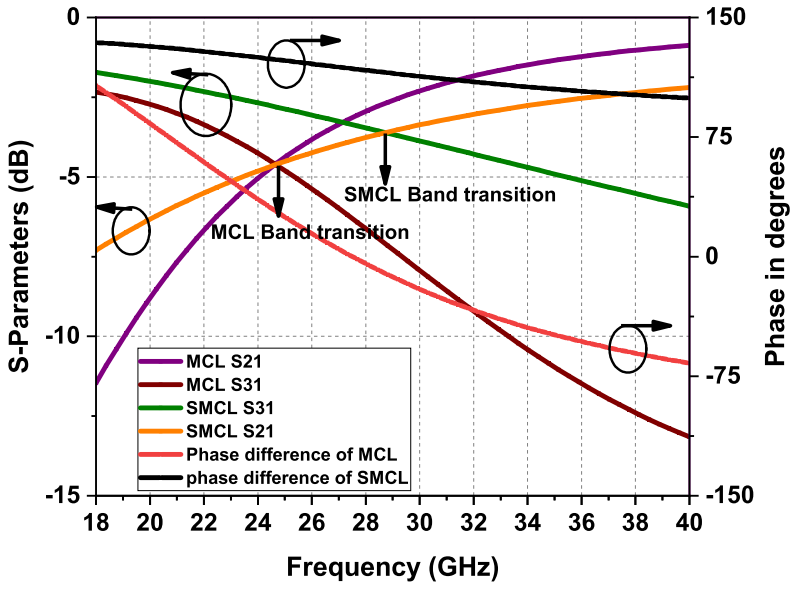


Figure 6.11: Simulated S-parameters and phase of MCL/SMCL as interstage

of $C_8 = 0.24$pF is added to the isolation port to increase coupled power. From the simulation results, as shown in Figure 6.12, over 25-40 GHz, the coupled power is approximately -1.5dB which is about 3dB higher than the traditional MCL as shown

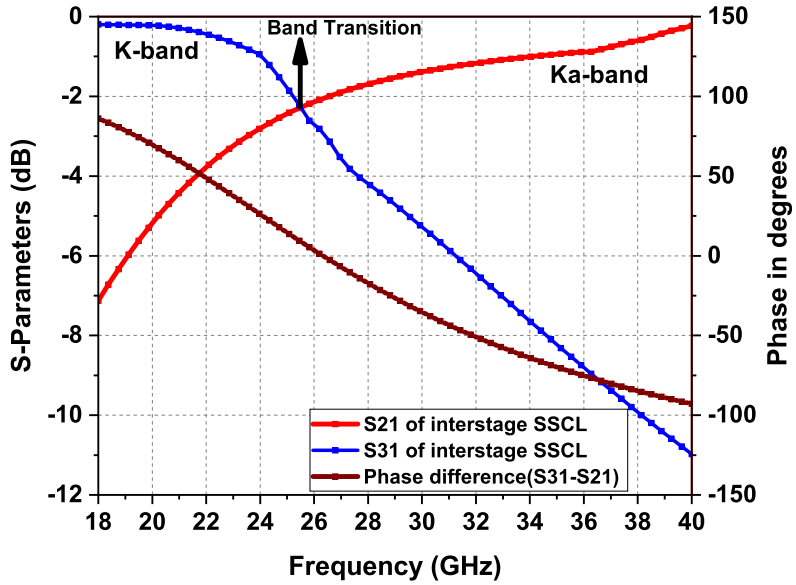


Figure 6.12: Simulated S-parameters and phase of SSCL as interstage

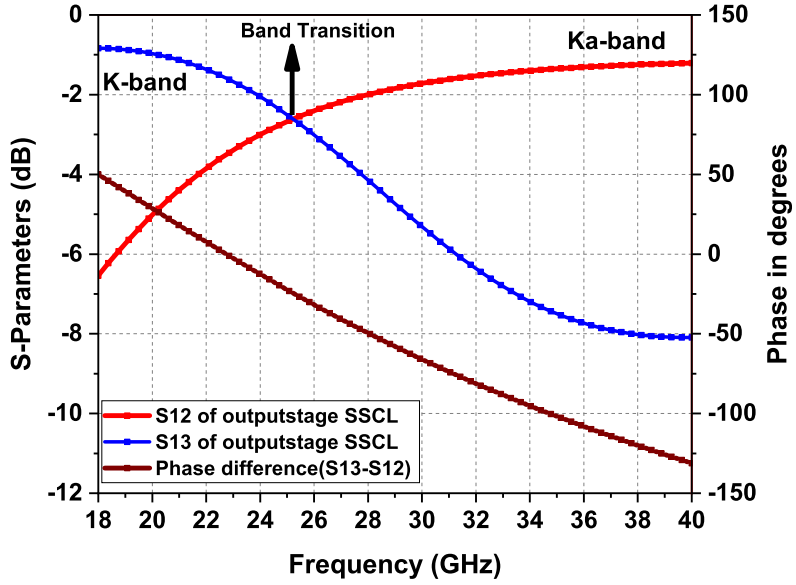


Figure 6.13: Simulated S-parameters and phase of SSCL as outputstage

in Figure 6.11. By this, the input broadband signal (18-40) GHz is successfully split into (18-24) GHz at the through-port and (25-40) GHz at the coupled port. The odd

mode characteristic impedance Z_{0o} and even mode characteristic impedance Z_{0e} are calculated to be 20.16Ω and 127.34Ω, respectively. Thus, the proposed SSCL can be applied in the reconfigurable LNA's interstage. Figure 6.10(b) is the schematic of the proposed output-stage SSCL, and the simulation result is shown in Figure 6.13. It is the symmetric structure of the interstage SSCL with optimized S, L, and Capacitors. Insertion loss is less than 3dB over 18-24 / 25-40 GHz. This stage combines the signal from the high-band and low-band stages and couples the power to the output as a broadband signal. The phase response of the couplers are also shown in the same Figure 6.11, 6.12 and 6.13 respectively.

6.4 Design and Analysis of CMOS Switchless LNA

The simplified block showing the proposed dual-band switchless reconfigurable LNA topology is shown in Figure 6.14. It consists of three amplifier stages: a broadband

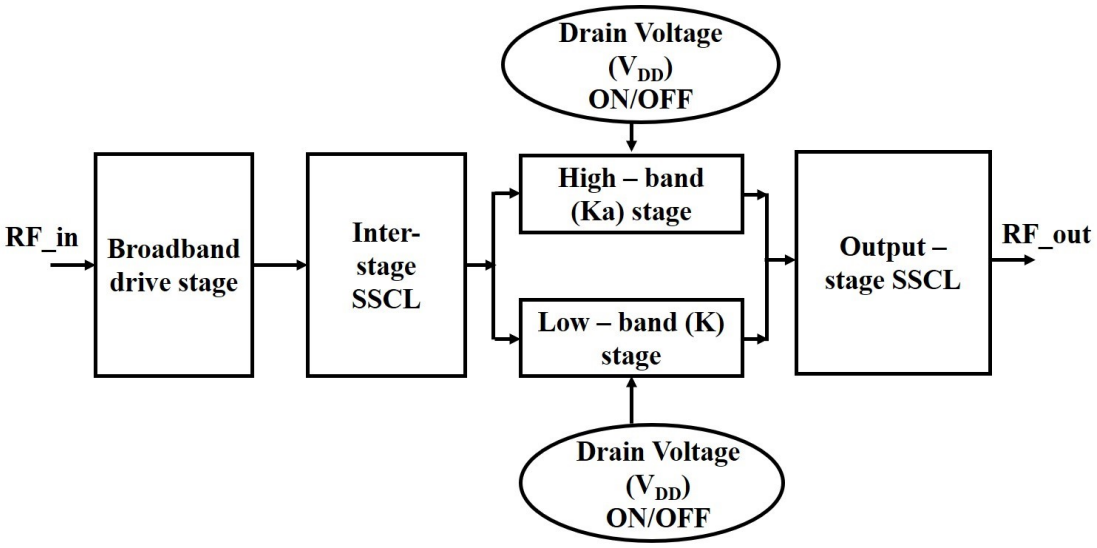


Figure 6.14: Proposed reconfigurable LNA topology

driving stage, a high-band (Ka) stage, and a low-band (K) stage, as well as two coupled stages based on SSCL, referred to as an inter-stage SSCL and an outer-stage SSCL. All three amplifier stages employ the common source (CS) topology. Transmission lines are utilised in place of spiral inductors in this design to conserve chip space and minimise other associated losses. To obtain a compact chip area, the lengthy transmission wires are bent. Instead of employing a normal quarter-wave long

transformer as the bias circuit for the proposed LNA, transmission lines and bypass capacitors are employed to behave like short circuits within the desired bandwidth and reduce chip size. Figure 6.15 depicts the proposed reconfigurable LNA in its

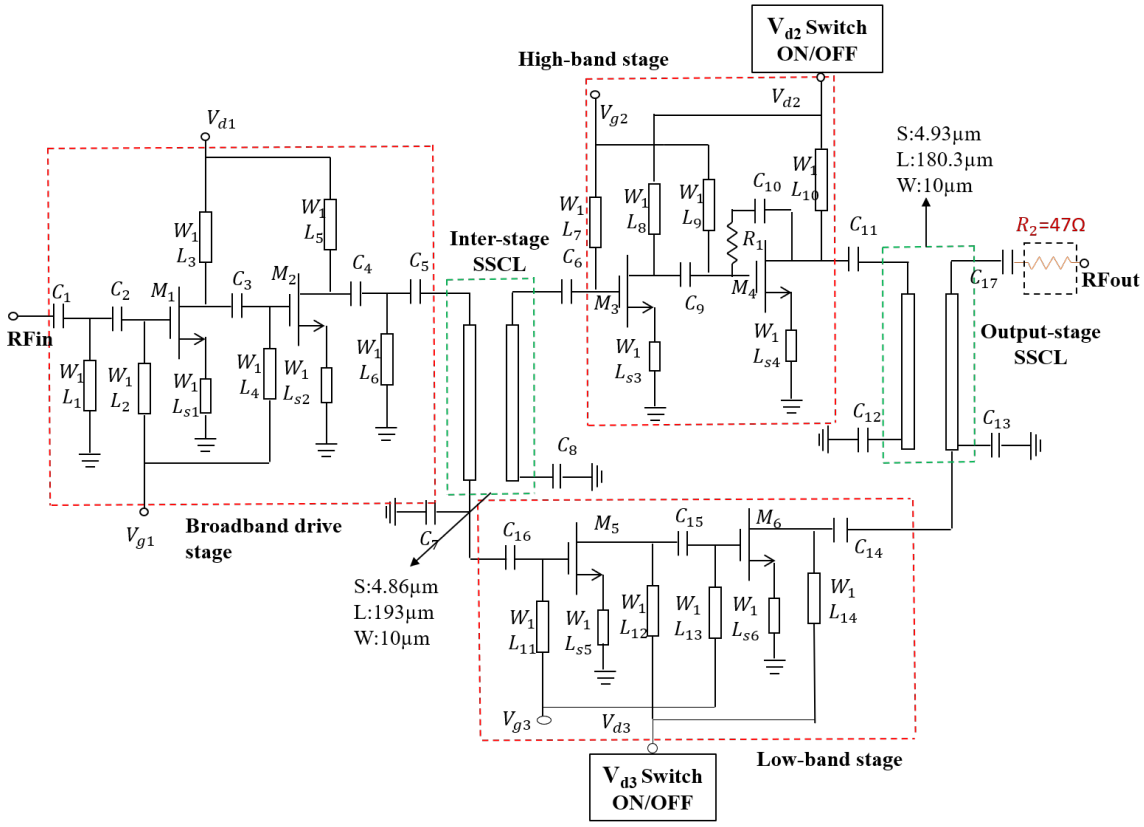


Figure 6.15: Schematic of the proposed reconfigurable LNA

whole. This reconfigurable Switchless LNA is capable of operating in three modes: dual-band, high-band (Ka), and low-band (K). V_{d3} is disabled for the Ka-band stage, V_{d2} is disabled for the K-band stage, and both are enabled for the dual-band stage. The following sections discuss the circuit architecture of the broadband drive stage and the high-band low-band stage.

6.4.1 Design of Broadband drive stage

As illustrated in Figure 6.15, the broadband drive stage is the first block in the proposed reconfigurable LNA topology. It is where the input RF signal is received. This stage is critical for the reconfigurable LNA's input matching and noise performance. It comprises of two cascaded CS stages with transistors M_1 and M_2 working at V_{g1}

= 0.43V. Capacitors (C_1, C_2) and a transmission line of length L_1 and width W_1 comprise the input matching network through which the signal flows and is sent to the transistor M_1's gate. M_1 and M_2 receive the drain and gate voltages through transmission lines of lengths L_3, L_2, and L_5, L_4. Source degeneration is incorporated through the use of the transmission lines L_{s1} and L_{s2} to M_1 and M_2 in order to get the ideal impedance for the lowest NF value near to the complex conjugate of the input impedance. This achieves both low NF and input impedance matching. The capacitor C_3 is employed to prevent direct current from flowing from the first to the second stage.

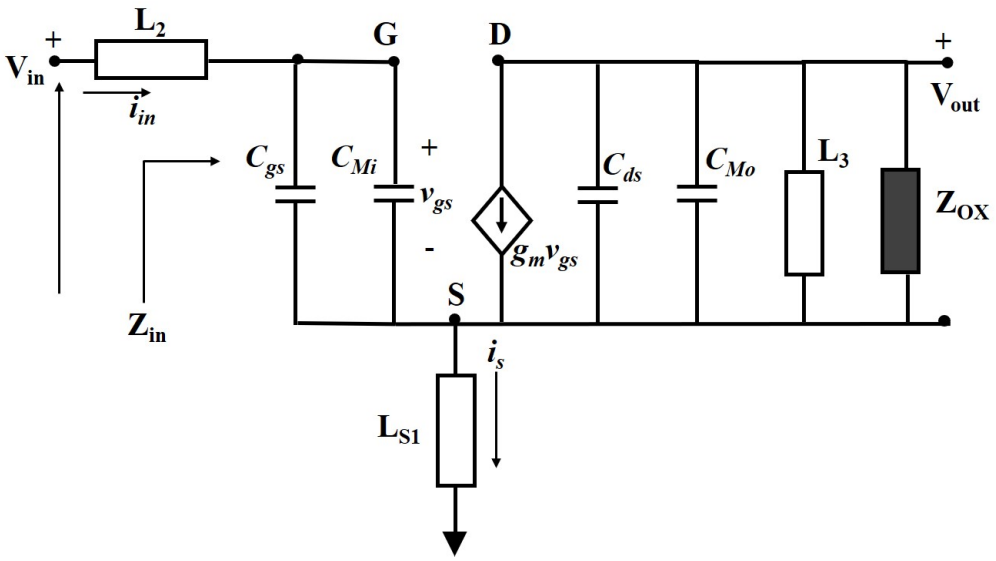


Figure 6.16: Simplified small-signal model of first CS stage for input impedance

The input impedance (Z_{in}) of the circuit, which depends mainly on this stage, can be calculated using the simplified small-signal model of the first CS stage is shown in Figure 6.16. Z_{OX} denotes the combined impedances of all the preceding stages. For simplicity, impedance in transmission lines such as L_2, L_1, and L_3 is considered inductance. In Figure 6.16 g_m denotes the transconductance of the transistor M_1, whose value is proportional to the width of the transistor, C_{gs} and C_{ds} denotes gate-source and drain-source capacitance, C_{Mi} and C_{Mo} denotes equivalent input and output Miller capacitance due to gate-drain capacitance C_{gd}.$C_{Mi} = C_{gd}\left(1 - A_v\right), C_{Mo} = C_{gd}\left(1 - \frac{1}{A_v}\right)$, A_v denotes the gain of the corresponding stage.

The input impedance of the circuit $\left(Z_{in} = \frac{V_{in}}{i_{in}}\right)$ is calculated as follows:

$$V_{in} = i_{in}\left[j\omega\left(L_2 + L_{S1}\right) + \frac{1}{j\omega C_{in}}\right] + g_m \cdot V_{gs} \cdot j\omega L_{S1} \tag{6.11}$$

Here $C_{in} = C_{gs} + C_{Mi}$ is the equivalent input capacitance at the gate terminal. Substituting $V_{gs} = i_{in}/j\omega \cdot C_{in}$ in equation 6.11 and simplifying gives

$$Z_{in} = \frac{V_{in}}{i_{in}} = \frac{g_m \cdot L_{S1}}{C_{in}} + j\left[\omega\left(L_2 + L_{S1}\right) - \frac{1}{\omega C_{in}}\right] \tag{6.12}$$

Similarly, the gain of the stage A_v can be calculated and shown in equation 6.13.

$$A_V = \frac{\frac{-g_m}{j\omega C_{in}} \cdot \left[j\omega L_3 \,\|Z_{ox}\|\, \frac{1}{j\omega C_{out}}\right]}{j\left[\omega\left(L_2 + L_{S1}\right) - \frac{1}{\omega C_{in}}\right] + \frac{g_m \cdot L_{S1}}{C_{in}}} \tag{6.13}$$

The simulated S-parameters of the broadband drive stage are shown in Figure 6.17. The gain (S_{21}) is above 20dB till 33GHz, and it falls to 16dB at 40GHz. The return loss (S_{11}) is well below -10dB from 18-40 GHz.

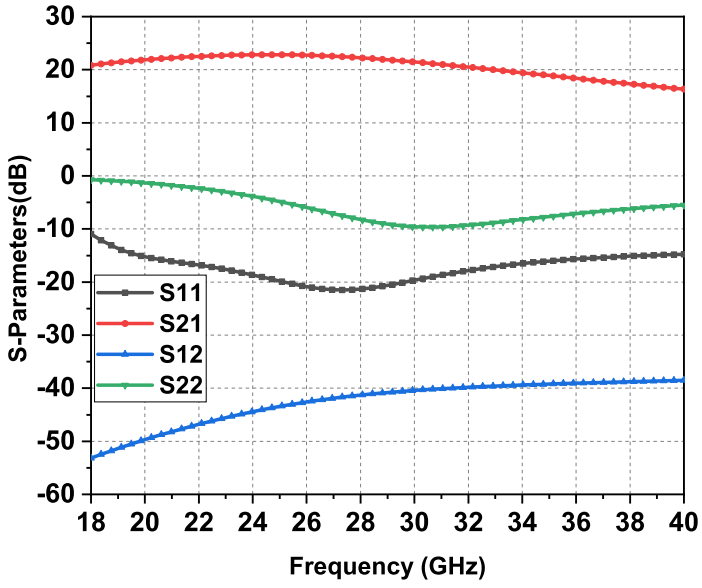


Figure 6.17: Simulated S-Parameters performance of the separate broadband drive stage.

6.4.2 Design of High band (Ka) and Low band (K) LNA stages

Simulated results for the broadband driving stage indicate a gain fluctuation of 7dB between 18-40 GHz. Though it is difficult to maintain almost constant gain across the whole bandwidth, the high-band and low-band stages, each of which consists of two transistors, are used to keep gain fluctuation below 2dB. The low-band stage is composed of transistors M_5 and M_6 in a two-stage cascaded configuration running at $V_{g3} = 0.4$V. This stage is intended to operate exclusively in the K band, between 18 and 24 GHz. Figure 6.18 illustrates the low-band driving stage's simulated S-parameters. The gain (S_{21}) is 10dB to 8dB in the 18-24GHz passband, but drops to 2dB at 40GHz. From 18-24 GHz, the return loss (S_{11}) is well below -10dB, while strong reflections are observed above this range. The high-band stage is composed of transistors M_3 and

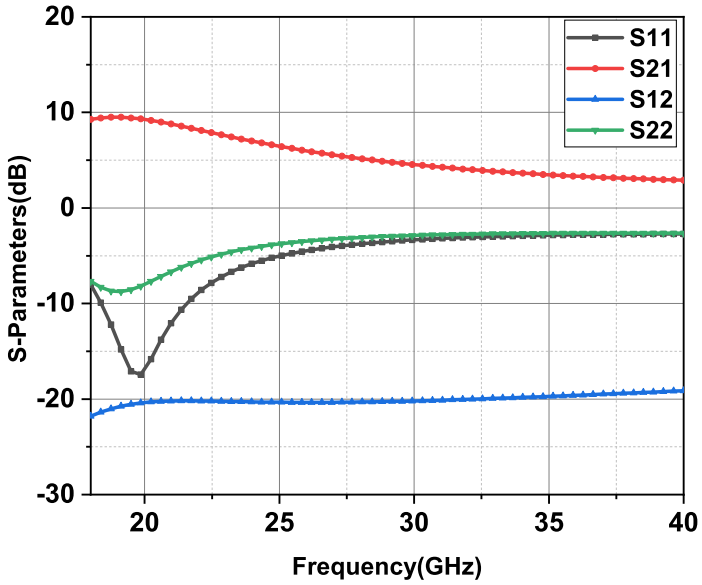


Figure 6.18: Simulated S-Parameters performance of the separate Low-band (K) stage.

M_4 in a two-stage cascaded configuration running at $V_{g2} = 0.47$V. This stage is meant to operate exclusively in the Ka-band, which covers the frequency range of 25-40 GHz. Figure 6.19 illustrates the simulated S-parameters of the high-band drive stage. Gain (S_{21}) is between 12dB and 10dB in the 25-40 GHz passband. From 25-40 GHz, the return loss (S_{11}) is significantly below -10dB, and high reflections are observed in

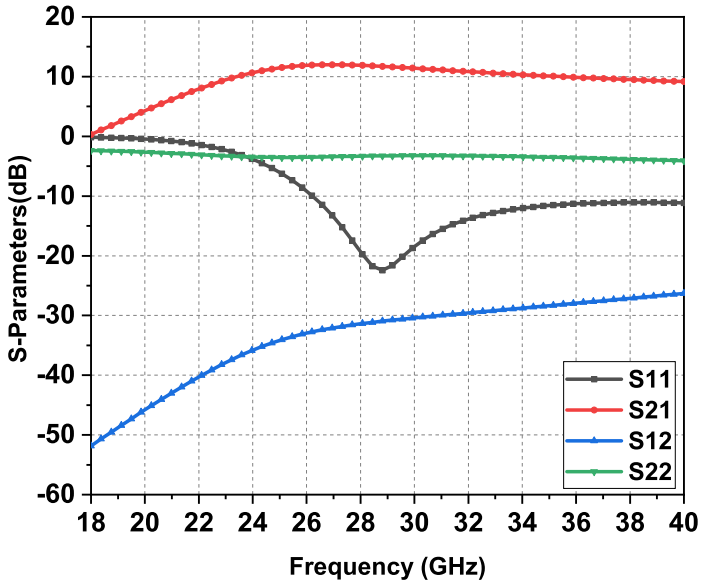


Figure 6.19: Simulated S-Parameters performance of the separate High-band (Ka) stage.

the 18-24 GHz range. To reduce instabilities caused by probable oscillation loops in the complicated structure of the multi-device amplifier or by the device's nonlinear nature, R-C resistive feedback is introduced at the transistor M_4's gate and drain using (R_1, C_{10}). It is not recommended to connect the coupled port (port 3) of the output stage SSCL directly to the 50Ω output load. This is because the SSCL is generated by stacking layer by layer on the substrate, making a direct connection to the output load difficult. Additionally, the impedance of SSCL varies with frequency, which is primarily inductive. In very extreme circumstances, the impedance may be completely inductive, resulting in circuit instability. To circumvent them, we have connected an R-C $(R_2 - C_{17})$ circuit between the output stage SSCL and the output load. In the worst-case scenario, the coupled R-C network cancels out any abrupt change in inductive impedance.

6.4.3 Consolidation of all Stages

After developing and testing each stage individually, such as the SSCL interstage, the SSCL output stage, the broadband stage, and the high and low band stages. As

illustrated in Figure 6.14, all stages are interconnected. The output of the broadband

Band	V_{d2}(V)	V_{d3}(V)	Total Current(mA)
K (18-24) GHz	0	1.2	13.8
Ka (25-40) GHz	1.2	0	14.5
K and Ka (18-40) GHz	1.2	1.2	21.4

Table 6.1: Drain Voltages states of single-band transistors.

drive stage is connected to port 1 of the SSCL interstage, where it is separated into two single bands designated as Ka-band and K-band. Based on the SSCL principle outlined in the preceding section. The Ka-band is coupled via SSCL's port 3, while the remaining K band is sent to the respective amplifier stages via port 2. Following amplification by the respective stages, the output stage SSCL is used to combine two single-band signals. As previously explained, SSCL at the output combines the signals from ports 2 and 3 and outputs the broadband signal from port 1. The total dc drain current and the drain voltage states of single-band transistors required to accomplish switch-free dual-band operation are shown in Table 6.1.

6.4.4 Noise Figure Analysis

To examine the whole LNA's noise figure, the following method is used to transform any noisy multi-port network into an equivalent noise-free network plus standard current and voltage noises at the input port. When all internal noise sources are represented as current noises, a general noisy multi-port can be explained as a hybrid of a noise-free multi-port and some current noises at the ports, as illustrated in appendix A-1

. The derivation of the noise factor F of the multi-port network is also depicted deeply in appendix A-1

Figure 6.20 illustrates the simulated NF of the various broadband, high band, and low band stages. The broadband stage NF has a U-shaped response curve with a maximum of 1.15dB at 40 GHz. This demonstrates that the technique outlined previously optimised the NF to a value of only 1.15dB. The low band stage's NF is around 1.6dB in the K band and grows above this band. The NF of the high band stage is

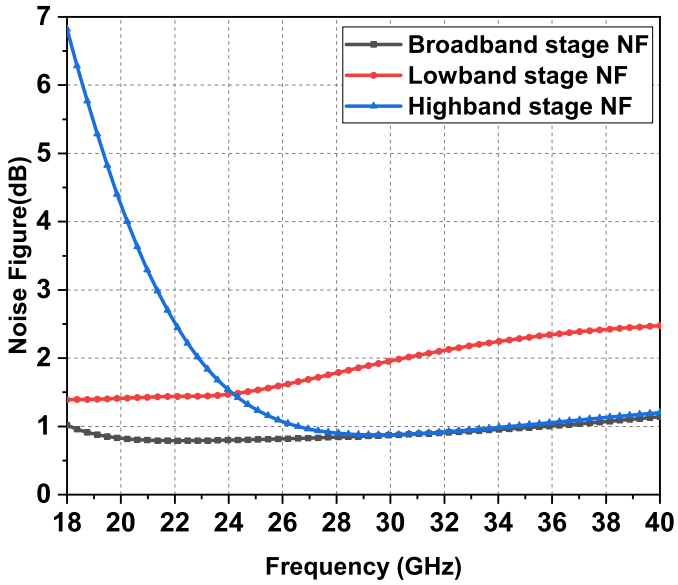


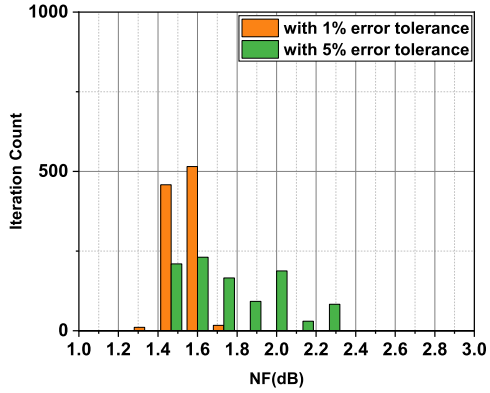
Figure 6.20: Simulated Noise Figure performance of the broadband, high band, and low band stages

around 1.2dB in the Ka band and up to 7dB in the K band. The reason for having high NF outside the desired frequency range in the single band operation lies in the design and optimization of SSCL.

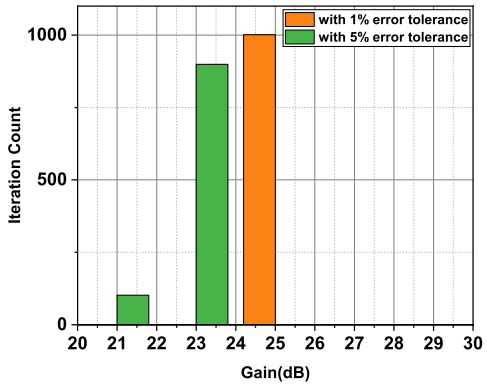
6.4.5 Statistical Analysis

Due to the fact that device parameters are vulnerable to fluctuation due to Process Voltage and Temperature (PVT), yield analysis is critical for calculating the real yield and confidence levels as discussed in section 2.8. The designed LNA is evaluated for 5% and 1% error tolerances under Gaussian distribution. NF, Gain, and return loss values are depicted in Figure 6.21 (a), (b), and (c), respectively. The stable gain of 25dB, the NF of 1.6dB, and the return loss of -11dB are all achieved with a tolerance of 1%.

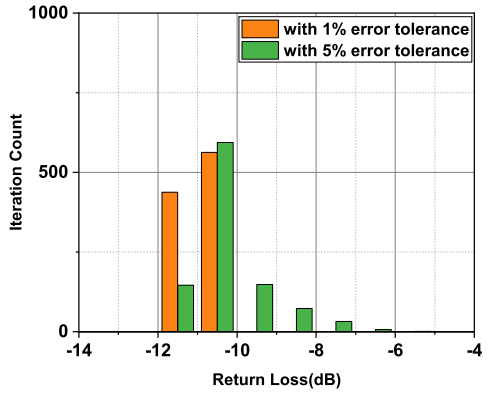
It resulted in a yield estimation of 100%, with a confidence level of 99.7% for 1000 iterations. However, with the 5% tolerance yield estimation, 10% of iterations failed to yield 90%. The parameters are limited to a minimum gain of 20dB, a maximum NF of 2dB, and a minimum return loss of -10dB. However, CMOS process PVT variations



(a)



(b)



(c)

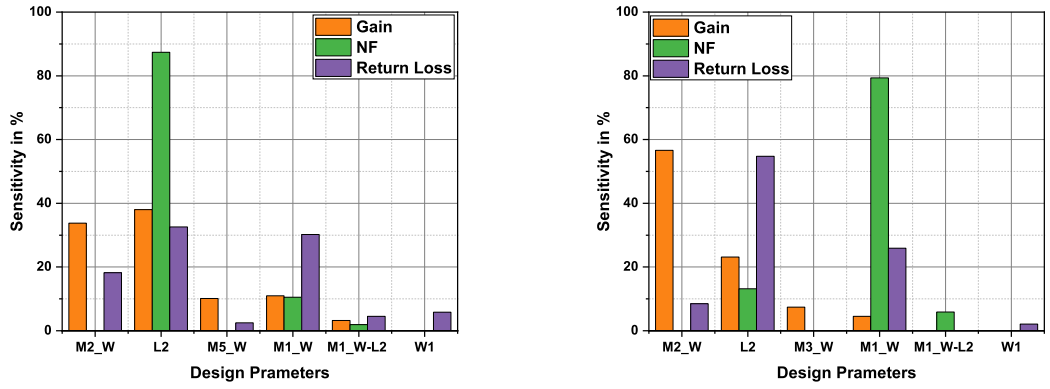
Figure 6.21: Yield estimation of LNA (a) Gain (b) NF. (c) Return Loss

are often less than 1%, indicating that the proposed reconfigurable switchless LNA is stable and accurate.

6.4.6 DoE Analysis

Design of Experiments (DOE) is a data-driven technique for a resilient design that elucidates the role of each design parameter in accomplishing a specific objective, such as a flat gain of 25dB, NF of 1.5dB with low return loss, and high linearity as discussed in section 2.9. The proportion contribution of each design parameter to the specified goal, such as NF, Gain, and return loss, is presented in Figure 6.22.

To validate the LNA at both the K and Ka bands, it is tested at 20GHz and 35GHz, as seen in Figure 6.22(a) and (b). With the exception of the percentage sensitivity,



(a) (b)

Figure 6.22: Design parameter contribution at (a) Low-band at 20GHz (b) High-band at 35GHz

the identical parameter from the broadband drive stage contributes to design goals. Additionally, it is noted that the low-band stage parameter M_{5W} contributes a small gain at 20GHz, whereas the high-band stage parameter M_{3W} contributes a small gain at 35GHz. For the sake of clarity, the design factors that contribute less than 1% are omitted from Figure 6.22. Extra attention has been taken during fabrication to ensure that these sensitive and contributing aspects produce trustworthy, precise measurement findings. The optimized parameters of the designed switchless LNA is depicted in Table 6.2.

Comp	Value	Comp	Value	Comp	Value	Comp	Value
M_{1W}	88 μm	M_{2W}	179 μm	M_{3W}	36 μm	M_{4W}	24 μm
M_{5W}	192 μm	M_{6W}	184 μm	W_1	10 μm	C_1	2.6 pF
C_2	0.14 pF	C_3	1.6 pF	C_4	0.24 pF	C_5	0.48 pF
C_6	0.44 pF	C_7	0.01 pF	C_8	0.24 pF	C_9	0.15 pF
C_{10}	0.5 pF	C_{11}	0.18 pF	C_{12}	1.6 pF	C_{13}	0.02 pF
C_{14}	0.6 pF	C_{15}	0.47 pF	C_{16}	0.8 pF	C_{17}	0.8 pF
R_1	1 KΩ	R_2	47 Ω	L_1	430 μm	L_2	157 μm
L_3	510 μm	L_4	520 μm	L_5	500 μm	L_6	94 μm
L_7	405 μm	L_8	438 μm	L_9	481 μm	L_{10}	462 μm
L_{11}	100 μm	L_{12}	384 μm	L_{13}	148 μm	L_{14}	362 μm
L_{S1}	35 μm	L_{S2}	2 μm	L_{S3}	36 μm	L_{S4}	23 μm
L_{S5}	305 μm	L_{S6}	452 μm				

Table 6.2: Optimized values of designed Switchless-LNA components

6.5 Performance Analysis

The LNA is designed and built utilising RF 65nm process technology by Magnachip Hynix Samsung. The chip is fabricated layer by layer with substrates and metal oxide metal (MoM) capacitors. Copper interconnects with six layers were fabricated using nanoclustering silica. These six layers, along with the other components of the LNA, are stacked on silicon wafers to give flexibility and thereby prevent parasitic losses caused by the CMOS mm-wave process. The procedure of stacking many layers is used to mount passive components on the silicon chip. Figure 6.23 shows a microchip die picture of the produced LNA. The chip's entire core area is $0.61 \times 0.92mm^2$. Full-wave simulations and measurements of LNA performance parameters have defined performance parameters with optimal dimensions to achieve high performance over a wideband of operation.

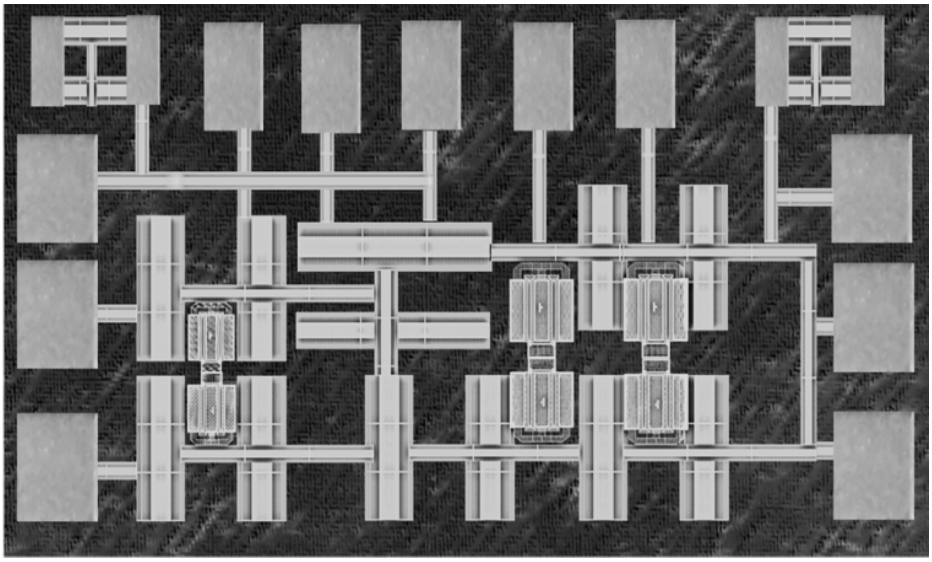


Figure 6.23: Microchip die photo of fabricated LNA

6.5.1 Experimental Verification

For on-wafer LNA, S-parameters and noise performance are measured using micro-probe sets such as Karl Suss (KSM) microprobe system, PNA-X (N5245B) Keysight's technologies up to 50GHz, and Cascade Microtech microprobe tips, with 100μm pitch. Prior to performing measurements, the PNA and micro-probes must be calibrated. Microprobe systems have been calibrated using the short-open-load-through technique.

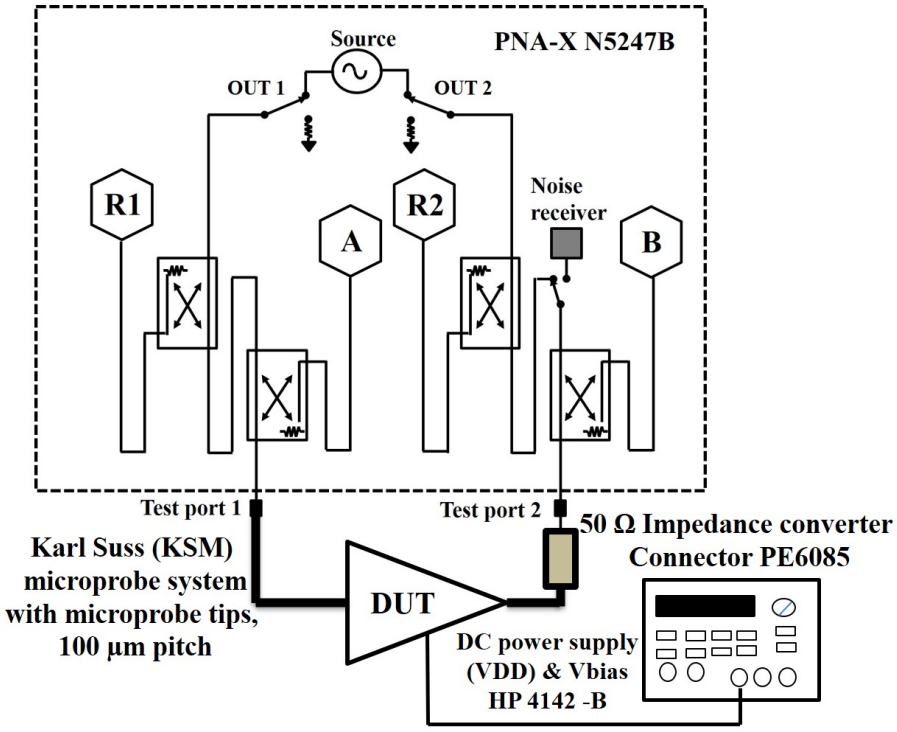


Figure 6.24: Measurement setup of the LNA

Gold short circuits (Short), gold open pads (Open), and gold plus thin film resistors (Load or Match) are included in the calibration sets. Figure 6.24 illustrates the complete measurement setup for the PNA-X. PNA-X employs a more precise cold source method than the conventional Y-factor method, in which the NF of the device under test (DUT) is determined from two independent measurements. The first measurement is the DUT's available gain. This is accomplished with extreme precision by measuring vector air corrected S-parameters. The second measurement is the noise power emanating from the DUT's output, with the input set at room temperature (25^0C). This noise figure option for the PNA-X has an integrated low noise receiver with three distinct gain levels. This enables the testing of a wide variety of devices with any combination of gain and NF without the need for additional hardware.

Vector Air corrected S-parameters compensate for the mismatch between the test system's unsatisfactory source match and the DUT's input impedance. When measuring the DUT's output noise power, mismatch correction is also implemented. The standard impedance tuner module is used to adjust the source mismatch created by the KSM probes and microprobe tips. Accurate 50Ω NF is estimated by adjusting the

source impedance applied to the DUT's input and measuring the resulting NF. The Pasternack PE6085 50Ω impedance convertor adapter connector is used to ensure that the output of S_{22} is properly matched. The comparison of state-of-art LNA with other reported ones is shown in Table 6.3 In Figure 6.25 and figure 6.26, the dual-band

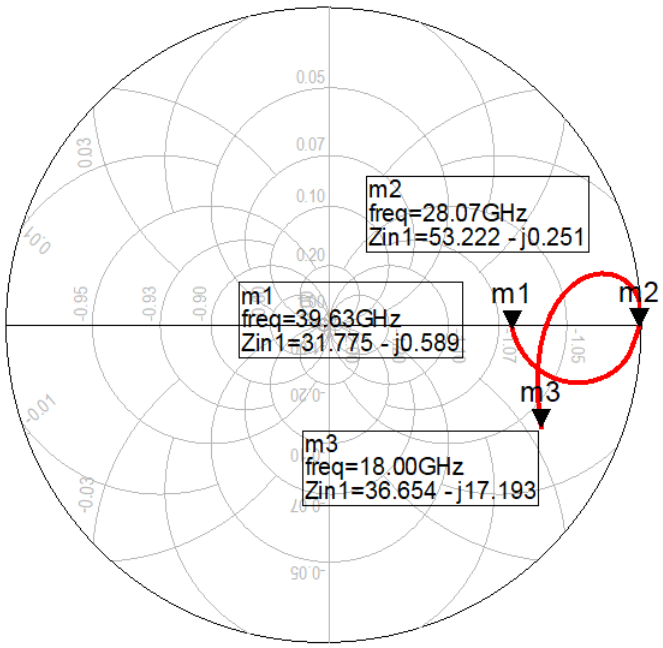


Figure 6.25: Simulated smith chart plot of proposed LNA Input Impedance

LNA's input and output impedances are shown as a smith chart respectively. It is worth noting that the input impedance begins in the capacitive region denoted as m3 at 18GHz and ends at the actual axis at 20GHz. It then follows the inductive zone and makes another contact with the real axis at 28 GHz and 31 GHz, shown by the symbol m2. It then passes through the capacitive zone again and comes to rest on the real axis at the final frequency 40GHz denoted by m1. The output impedance is capacitive dominant from the starting frequency of 18GHz, denoted by m6, to 25GHz, denoted by m4. As a result, the impedance in the K band (18-24 GHz) is capacitive, whereas the impedance in the Ka band (25-40 GHz) is inductive. LNA stability is measured and plotted in Figure 6.27. It is noted that the designed reconfigurable switchless LNA is unconditionally stable in the desired frequency range of 18 to 40 GHz. The proposed reconfigurable switchless LNA's measured and simulated NF and S-parameters in all three modes, dual-band mode, high-band mode, and low-band mode, are illustrated here. The NF fluctuates between 1.05dB at 18GHz and 1.2dB

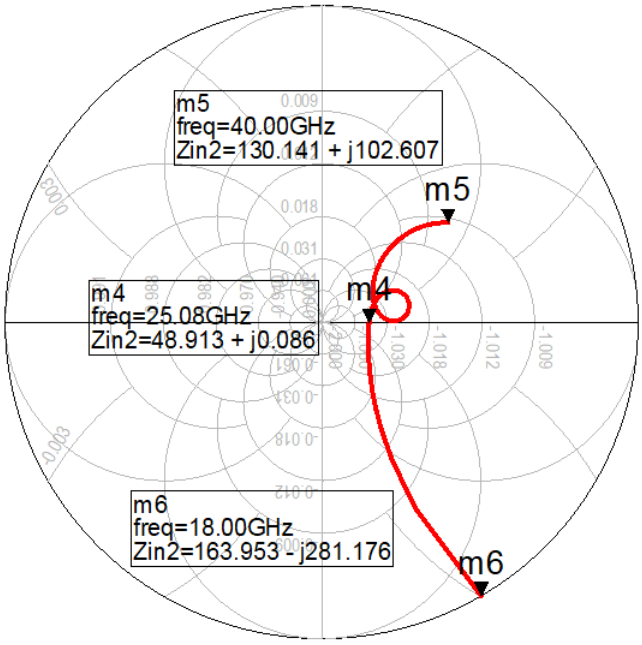


Figure 6.26: Simulated smith chart plot of proposed LNA Output Impedance

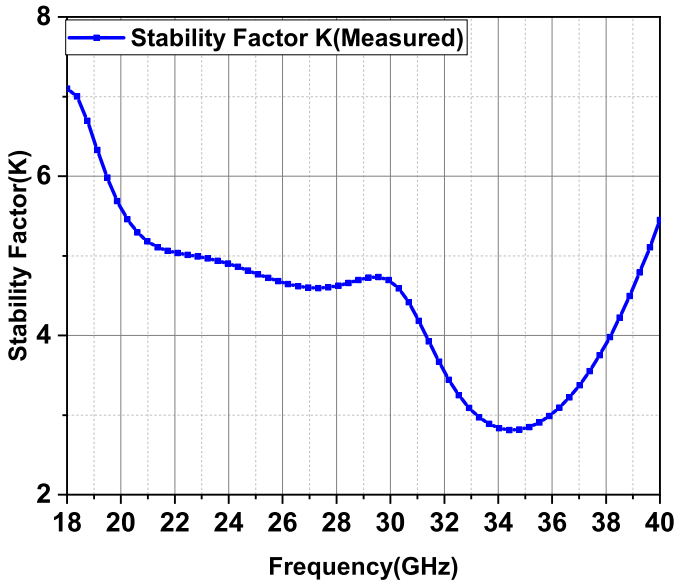


Figure 6.27: Stability factor K of LNA

at 40GHz in dual-band mode, with a minimum of roughly 0.9dB at 21GHz, as shown in Figure 6.28. As illustrated in Figure 6.29, the gain of 27dB is attained with only

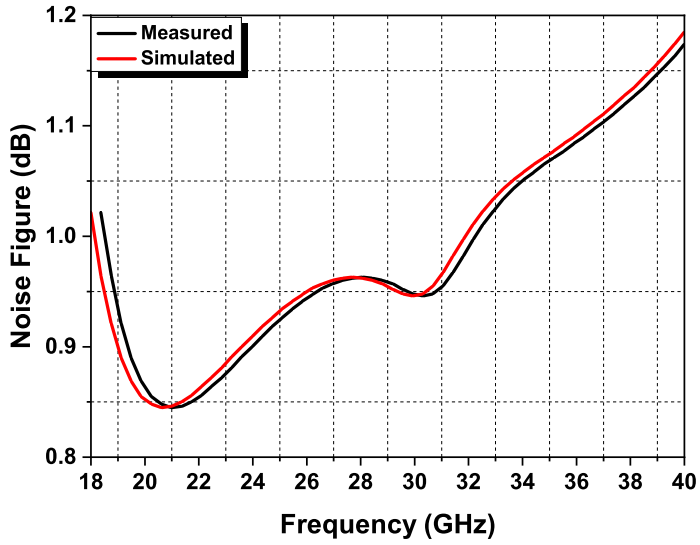


Figure 6.28: Noise Figure of the designed dual-band LNA

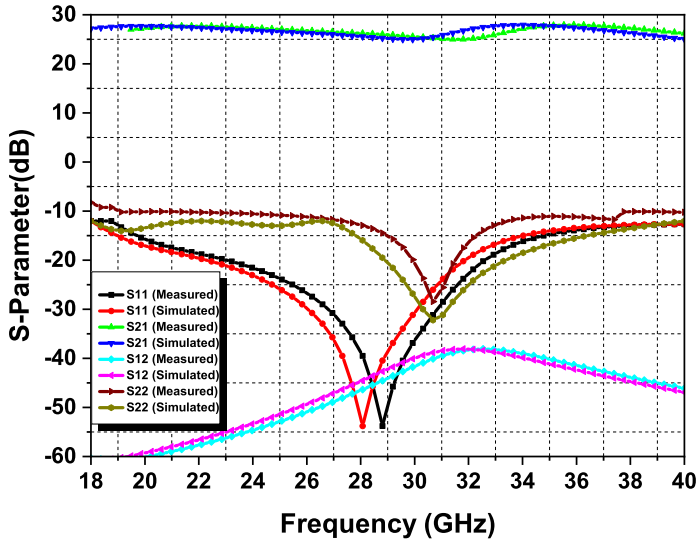


Figure 6.29: Simulated and measured S-parameters of the designed LNA in dual-band mode

a 0.2dB fluctuation and a 2dB variation across the entire frequency ranges of 18 to 24GHz and 24 to 40GHz. When compared to the previously reported works, this is phenomenal performance in terms of gain for having such a little fluctuation across

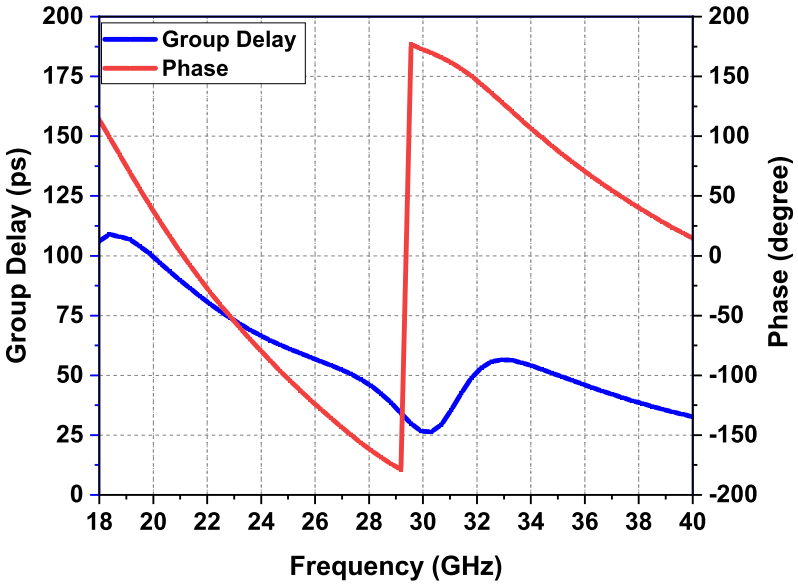


Figure 6.30: Simulated group delay and phase response of the designed LNA in dual-band mode

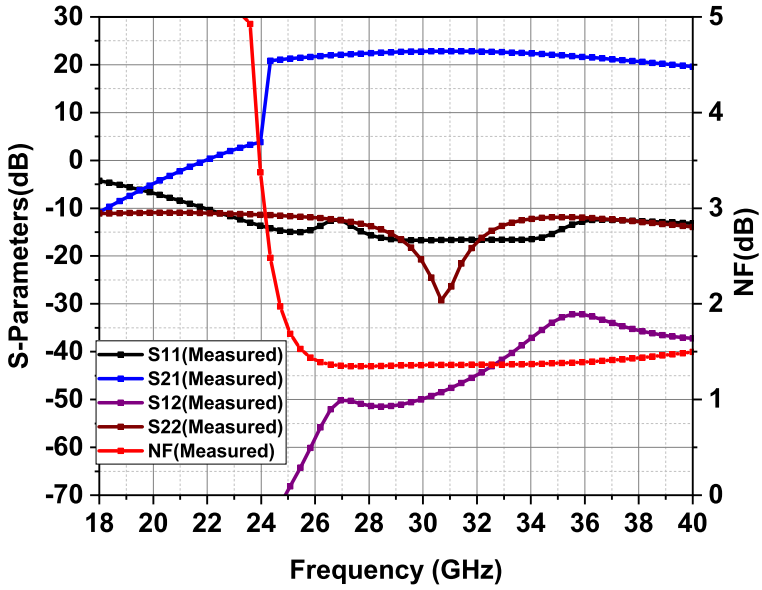


Figure 6.31: Measured S-parameters and NF of the designed LNA in high-band mode

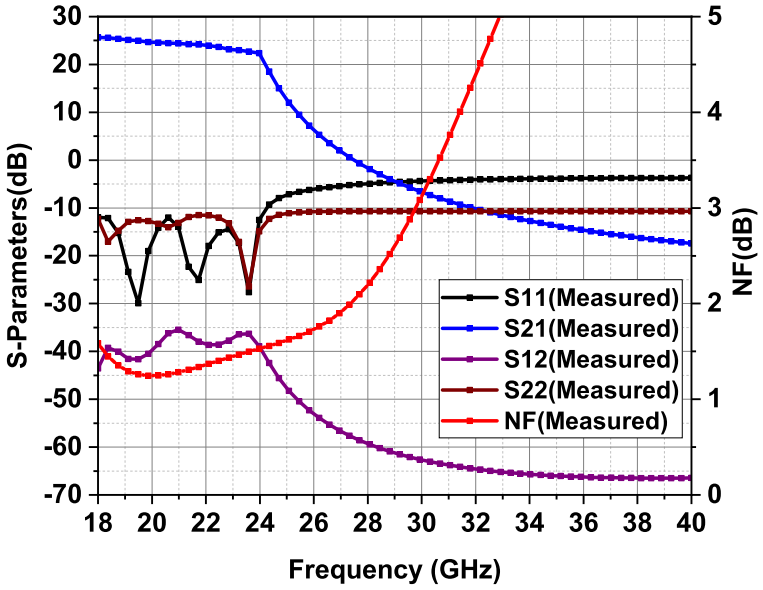


Figure 6.32: Measured S-parameters and NF of the designed LNA in low-band mode

the full 22GHz bandwidth. The return loss (S_{11}) is substantially below 10dB, preventing reflection. Other parameters, such as S_{12} and S_{22}, also perform satisfactorily. The simulated group delay and phase response of the designed LNA in dual-band mode is shown in Figure 6.30 also shows satisfactory performance. As illustrated in Figure 6.31, a consistent gain of 22dB with a 2dB variation is attained in high-band mode in Ka-band (25 to 40GHz). NF of around 1.5dB is attained with a return loss of less than 10dB. As illustrated in Figure 6.32, steady gain of 25dB with a variation of 1dB is attained in low-band mode (18 to 24GHz). A NF of around 1.5dB is attained with a return loss of less than 10dB.

The linearity analysis was used to determine the harmonics of the basic signal, such as third-order harmonics. Due to the fact that we are dealing with mm-wave bands up to 40GHz, we have included an analysis of second harmonics. Figure 6.33 and figure 6.34 show the measured values at 20GHz (K-band) and 35GHz (Ka-band). At 20GHz, the input 1dB compression point (IP_{1dB}) is -17dBm, the output 1dB compression point (OP_{1dB}) is +7.1dBm, the input intercept third-order point (IIP_3) is 0dBm, the output intercept third-order point (OIP_3) is +25dBm, and the input intercept second-order point (IIP_2) is +5dBm. As shown in Figure 6.34, at 35GHz, the input 1dB compression point (IP_{1dB}) is -16dBm, the output 1dB compression

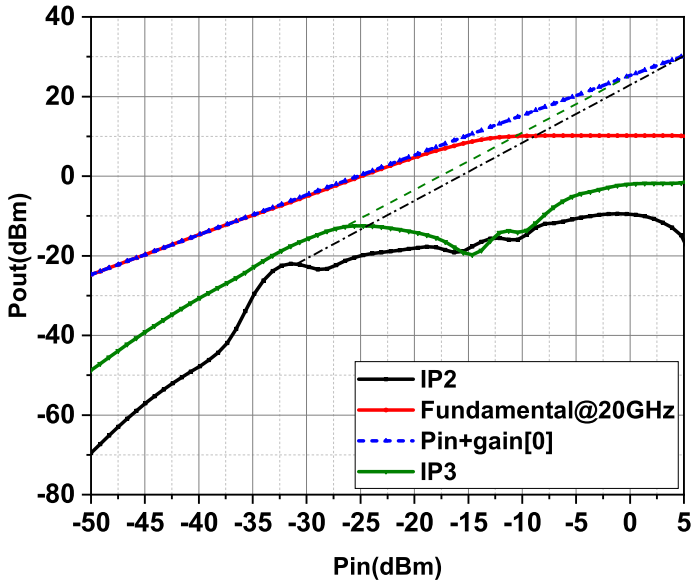


Figure 6.33: Measured K-band Linearity performance

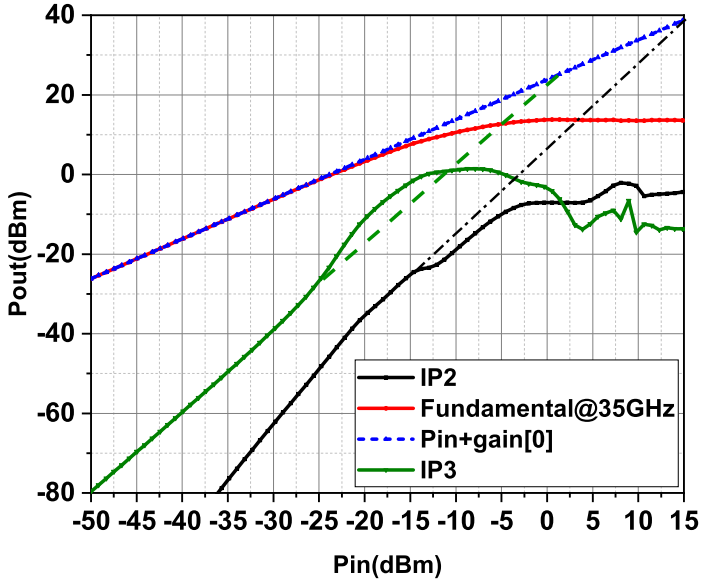


Figure 6.34: Measured Ka-band Linearity performance

point (OP_{1dB}) is +6.4dBm, the input intercept third-order point (IIP_3) is 0dBm, the output intercept third-order point (OIP_3) is +23dBm, and the input intercept

second-order point (IIP_2) is +5dBm. This value indicates that our reconfigurable switchless LNA architecture is more effective at suppressing harmonics and delivering good linearity to the input. This is accomplished by the use of optimised source degeneration with transmission lines at each CS stage to maintain a gain of less than 28dB and the suggested SSCL at the interstage and output to mitigate the impacts of intermodulation distortion (IMD). When the IMD decreases, the IIP_3 automatically increases, resulting in a more linear device.

6.6 Summary

This research describes the design and fabrication of a switch-free reconfigurable dual-band LNA working between 18GHz to 40GHz in 65nm CMOS technology. To achieve frequency reconfigurable capabilities, we theoretically investigated and built Suspended Substrate Coupled Lines (SSCL) in the interstage and output stage. The interstage SSCL divides the dual-band input signals into single-band amplifiers and then combines them in the output port via the output-stage SSCL. The projected LNA's unit transistor is designed in a Common-Source (CS) architecture and takes advantage of the inductive effect of transmission lines to degenerate the source while maintaining low noise and input matching. The fabricated $0.56mm^2$ LNA device has a measured small-signal gain of 27-27.2 dB with approximately 1dB NF in the 18-24 GHz band and a measured small-signal gain of 25-27dB with approximately 1.2dB NF in the 24-40 GHz band. The statistical and DoE analyses are presented to evaluate the design's yield and robustness. The LNA is highly linear, with an IP_{1dB} of -16dBm, an IIP_3 of 0dBm, an OP_{1dB} of +6.4dBm, and an OIP_3 of +25dBm. The proposed chip consumes 25.7mW only in the dual band. The comparison to the state of the art demonstrates that the developed LNA produces reasonably good mean values for all parameters, resulting in the highest FOM when used in modern receiver systems.

Table 6.3: Comparison of the proposed reconfigurable LNA performance with state of art.

Parameters	Technology	Freq(GHz)	Gain(dB)	NF(dB)	IP_{1dB}(dBm)	IIP_3(dBm)	OP_{1dB}(dBm)	OIP_3(dBm)	P_{DC}(mW)	Area (mm^2)	FoM	FoM_{IP3}
Shaheen *et al.* (2021)	45nm SOI	24 28 39	9.5 12 15.5	4.5 4.5	-12 -13 5.5	– -16.5	–	–	15.5	0.317	0.3	–
Nawaz *et al.* (2019)	130nm SiGe	28 60	16.2 15	2.8 3.4	-12 -7	–	–	–	8.2 21	0.1	0.3	–
Liang *et al.* (2020)	28nm CMOS	24 33 50	29.9 32.4 22.2	5.63 4.6	-40 -42 6	– -34	–	–	25.6	0.22	0.4	–
Wang and Zhang (2020)	130nm SiGe	22-47	22.2	4.3	–	-13.8	–	–	9.5	0.13	19.1	0.76
Lee and Nguyen (2018)	130nm SiGe BiCMOS	18-25 33-46	16 17	4.3 4.3	-24 -27	-15 -17	–	–	73.8	0.69	0.7	0.02
Yu *et al.* (2021)	65nm CMOS	22-40	28	3.2	-25	–	–	–	32	0.4	14	–
Li *et al.* (2018)	45nm CMOS	14-31	12.8	1.4	–	5	–	–	15	0.3	12	38.4
El-Aassar and Rebeiz (2020)	22nm FDSOI	23-27	28.5	2.4	-21	-10.4	–	1.95	20	0.19	7.6	0.76
Xie *et al.* (2020)	150nm GaAs	8-12 12-20	25-25.2 20-28	1.4 1.5	–	–	1.7 5	–	190 227.5	3.6	1.8 1.6	–
This Work	65nm CMOS	18-24 24-40	27-27.2 25-27	0.85-1.05 0.95-1.2	-17 -16	0 0	+7.1 +6.4	+25 +23	16.5 17.4	0.56	59.9	40.7 51.1

– Not calculated

Chapter 7

CONCLUSION AND FUTURE WORKS

7.1 Conclusion

Chapter 1 and chapter 2 presented the LNA basics with the design trade-offs, the basic LNA topology, and the performance metrics. The performance metrics such as Noise, Noise figures, S-parameters, linearity analysis, and so on have been discussed briefly. In addition to that, two new analyses, such as statistical analysis and DoE analysis, have been elaborated on in this chapter.

Chapter 3 presented a high gain with good linearity low noise amplifier is designed using a suspended substrate line for a 5G wireless cellular front-end receiver system operating at 28-32GHz. The proposed LNA design used optimization techniques and achieved high-performance SoC IC solutions with EM compatibility. The LNA is fabricated using 65nm CMOS technology which operates at 1.2V, and the chip area is $0.35 \times 0.22mm^2$.

Chapter 4 presented a Quasi Circulator integrated low noise amplifier is designed for the entire X band covering 8-12GHz for high survivability RF front end systems. The designed QC-LNA achieves an excellent flat gain of 30dB with ultra-low-noise figure 1dB in the entire 4GHz bandwidth and provides good linearity. The LNA is fabricated using 65nm CMOS technology which operates at 1.2V, and the chip area is $0.84 \times 0.52mm^2$.

Chapter 5 presented a folded butterfly stub stepped impedance resonator integrated LNA designed for satellite navigation systems operating at 1.6-2.5GHz. The

LNA is fabricated using PCB technology which operates at 3.3V, and the board area is $10.7 \times 2cm^2$. The LNA offers a decent gain of 22dB, a noise figure of 2.7dB, and good linearity. The FBSSIR is also fabricated separately and analyzed with the size of $3.3 \times 1.6cm^2$.

Chapter 6 presented a switchless reconfigurable low noise amplifier for full K/Ka-band using suspended substrate coupled lines operating at 18-40GHz is designed for modern wireless systems. The designed LNA achieves high-performance SoC solutions such as the highest flat gain of 27dB and an ultra-low noise figure of 1.2dB (Maximum) in the entire 22GHz bandwidth. It also offers excellent linearity performance, especially in suppressing the third and second-order harmonics. The band shifting is controlled by the drain voltage of the K band and Ka-band stages. The LNA is fabricated using 65nm CMOS technology and consumes 25.7mW (in dual-band mode), with the chip area of $0.61 \times 0.92mm^2$.

7.2 Future Works

The proposed CMOS LNAs considered all the essential parameters it should consider but to design a single SoC RF front-end system, the separate LNA is not sufficient. All the fabricated LNAs are single entity SoC. In the future, the work can be focused on integrating the designed LNAs with other RF front-end components such as antenna, mixer, oscillator, Phase-locked loop, and so on. In this way, it is possible to test the designed LNAs' functionality in real-time, and also, we can study the issues that arise during the integration.

We can incorporate other microwave techniques into the design. Also, we can do work on making the lower nm technologies such as 45nm, 22nm, 7nm, and so on. It can also focus on the sub-mm bands.

Appendix I
DERIVATION

A-1 Noise Figure Derivation

To examine the whole LNA's noise figure, the following method is used to transform any noisy multi-port network to an equivalent noise-free network plus standard current and voltage noises at the input port. When all internal noise sources are represented as current noises, a general noisy multi-port can be explained as a hybrid of a noise-free multi-port and some current noises at the ports, as illustrated in Figure A.1(a). Ports 1 and 2 denote the input and output ports, respectively, while Figure A.1(b) depicts the equivalent standard multi-port network. To find equivalent current and

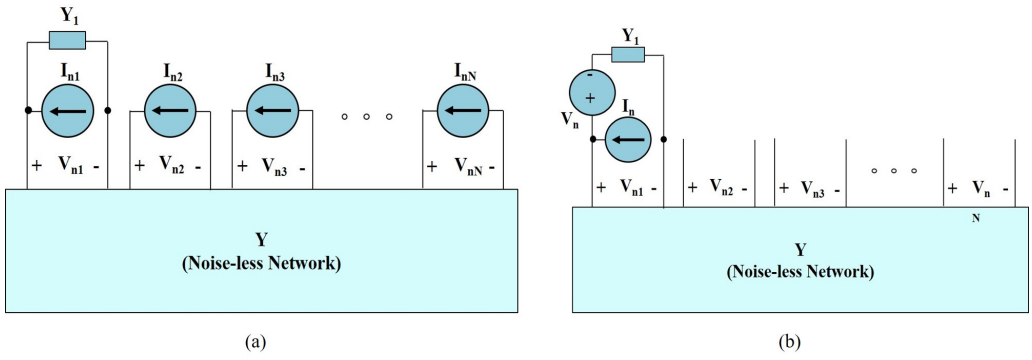


Figure A.1: Noisy multi-port (a) its equivalent noiseless multi-port network (b) with equivalent current and voltage noise sources at the input.

voltage source noises at the input port, we describe the network by Y matrix:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1N} \\ Y_{21} & Y_{22} & \cdots & Y_{2N} \\ \vdots & \vdots & \cdots & \vdots \\ Y_{N1} & Y_{N2} & \cdots & Y_{NN} \end{bmatrix} \tag{A.1}$$

Now we define a new matrix

$$Y'' = \begin{bmatrix} Y_{21} & Y_{23} & \cdots & Y_{2N} \\ Y_{31} & Y_{33} & \cdots & Y_{3N} \\ \vdots & \vdots & \cdots & \vdots \\ Y_{N1} & Y_{N3} & \cdots & Y_{NN} \end{bmatrix} \tag{A.2}$$

Equivalent current and voltage noises in Figure A.1(b) are depicted as

$$\begin{cases} I_n = \frac{\Delta_{12} I_{n1} + \Delta_{22} I_{n2} + \cdots \Delta_{N2} I_{nN}}{\Delta_{12}} \\ V_n = \frac{\Delta''_{11} I_{n2} + \Delta''_{21} I_{n3} + \cdots \Delta''_{N-1,1} I_{nN}}{\Delta_{12}} \end{cases} \tag{A.3}$$

Where Δ_{ij} and Δ''_{ij} are the determinant of the adjoint matrix of the ij the element of the Y and Y$''$ matrix respectively.

Using the correlation coefficient I_n and V_n is correlated.

$$c = \overline{I_n V_n{}^*} \tag{A.4}$$

I_n can be divided into two terms, one is correlated to V_n and the other is uncorrelated

$$I_n = I_{nc} + I_{nu} \tag{A.5}$$

$$\overline{I_n V_n{}^*} = \overline{(I_{nc} + I_{nu})\, V_n{}^*} = \overline{I_{nc} V_n{}^*} \tag{A.6}$$

The correlation admittance Y_c is defined as:

$$Y_c = G_c + jB_c = \frac{I_{nc}}{V_n} \tag{A.7}$$

$$Y_c = \frac{c}{\overline{V_n^2}} \tag{A.8}$$

Equivalent noise resistance R_n is defined as

$$R_n = \frac{\overline{V_n{}^2}}{4kTB} \tag{A.9}$$

Equivalent noise conductance G_u is defined as

$$G_u = \frac{\overline{I_{nu}{}^2}}{4kTB} = \frac{\overline{I_n{}^2} - \overline{I_{nu}{}^2}}{4kTB} = \frac{\overline{I_n{}^2} - |Y_c|^2 \overline{V_n{}^2}}{4kTB} \tag{A.10}$$

This expression is used in the above equation

$$\overline{I_{nu}{}^2} = \overline{I_n{}^2} - \frac{|c|^2}{\overline{V_n{}^2}} \tag{A.11}$$

The optimum source admittance Y_{S_opt} for minimum noise factor is calculated as:

$$Y_{S\_opt} = \sqrt{G_c^2 + \frac{G_u}{R_n}} - jB_c \tag{A.12}$$

$$Y_{S\_opt} = \sqrt{\frac{\overline{I_n^2}}{\overline{V_n^2}} - B_c^2} - jB_c \tag{A.13}$$

The minimum noise figure F_{min} is calculated as:

$$F_{\min} = 1 + \frac{G_u + R_n \left(G_{\text{Sopt}} + G_c\right)^2}{G_{\text{Sopt}}} \tag{A.14}$$

Finally, the noise factor F of the multi-port is calculated as:

$$F = 1 + \frac{G_u + R_n \left|Y_S + Y_c\right|^2}{G_S} \tag{A.15}$$

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2. **Vignesh R**; Pradeep Gorre ; Sandeep Kumar ; Hanjung Song "Highly Robust X-Band Quasi Circulator Integrated LNA for High Survivability of RF Front-end Systems" International Journal of Circuit, Theory and Applications, Wiley, vol 49, issue 7, July 2021, page no 2170-2182. DOI: 10.1002/cta.3001.

3. **Vignesh R**, Pradeep Gorre, Sandeep Kumar, "A novel wide bandwidth FB-SSIR integrated low noise amplifier for satellite navigational receiver system", Microelectronics Journal, Volume 117, 2021, 105288, ISSN 0026-2692.
   DOI: 10.1016/j.mejo.2021.105288.

4. **Vignesh R**; Pradeep Gorre ; Sandeep Kumar ; Hanjung Song "A K/Ka-band Switchless Reconfigurable 65nm CMOS LNA based on Suspended Substrate Coupled Line" in IEEE Access, vol. 10, pp. 33449-33464, 2022, DOI: 10.1109/ACCESS.2022.3162202.

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1. **Vignesh R**, P. Gorre, S. Kumar and H. Song, "A 28-32GHz CMOS LNA with Broadband Approach for 5G Mm-Wave Communication cells," 2019 IEEE Asia-Pacific Microwave Conference (APMC), 2019, pp. 485-487, doi: 10.1109/APMC46564.2019.9038463.

Book Chapters :

1. "Techniques to improve Gain-Bandwidth 5G ICs" in book title "CMOS Analog IC Design for 5G and Beyond" ISSN 1876-1100, ISBN 978-981-15-9864-7, 2021, Contributed by **Vignesh R** and Sandeep Kumar, doi:10.1007/978-981-15-9865-4.

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